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Optical and interface properties of direct InP/Si heterojunction formed by corrugated epitaxial lateral overgrowth

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Abstract: We fabricate and study direct InP/Si heterojunction by corrugated epitaxial lateral overgrowth (CELOG). The crystalline quality and depth-dependent charge carrier dynamics of InP/Si heterojunction are assessed by characterizing the cross-section of grown layer by low-temperature cathodoluminescence, time-resolved photoluminescence and transmission electron microscopy. Compared to the defective seed InP layer on Si, higher intensity band edge emission in cathodoluminescence spectra and enhanced carrier lifetime of InP are observed above the CELOG InP/Si interface despite large lattice mismatch, which are attributed to the reduced threading dislocation density realized by the CELOG method.

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1. Introduction

Integration of III-V semiconductors on silicon is a major challenge in realizing efficient electronics-photonics integrated devices and systems. Several III–V compounds are direct bandgap materials and hence have favorable optical and electronic properties, such as efficient light emission and high carrier mobility. In particular, InP and related materials are important III-V semiconductors, used in long wavelength lasers, high performance photodetectors, high electron mobility transistors, etc [1,2]. High crystalline quality InP/Si are desired for Si based photonic integrated circuits and tandem solar cell applications. The three main approaches to integrate III-V and Si are: flip-chip integration [3], bonding technologies [4], and hetero-epitaxial growth [5]. Among them, heteroepitaxy would be the most desirable approach for integration because of better thermal dissipation, self-alignment (which provides high integration density), fewer processing steps, and device cost effectiveness [6]. However, the large lattice mismatch between InP and Si, the difference in the thermal expansion coefficients, and the polar/non-polar interfaces usually result in heteroepitaxial layers with high density of crystal defects. It is not uncommon to find misfit and threading dislocations, stacking faults, microtwins, and antiphase domains in those InP/Si layers. All these defects are detrimental to the optical devices made out of InP/Si, since they create deep electronic levels in the band gap, which can act as carrier traps, and non-radiative recombination centers (NRRCs) [7].

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Various approaches for defect reduction have been considered to achieve high crystalline quality III-V/Si substrates by epitaxial growth techniques [5,8]. The corrugated epitaxial lateral overgrowth (CELOG) method, a modified form of epitaxial lateral overgrowth (ELOG) [9], has been shown to be a potential solution for III-V/Si integration by hydride vapor phase epitaxy (HVPE) [10]. HVPE is an ideal method for III-V based solar cell fabrication since it uses cheap precursors [11], yields high growth rate and gives the growth selectivity necessary for CELOG [12]. Recently an n-InP/p-Si heterojunction photodiode was realized by the CELOG method in a HVPE reactor [13].

Understanding the minority carrier dynamics in InP/Si heterojunction is essential for achieving high performance devices, such as high efficiency solar cells. In InP/Si layers with high dislocation density, dislocations act as recombination centers which reduce the minority-carrier lifetime and diffusion length [14]. In heterojunction solar cells, where dislocation density is normally high, the predominant loss mechanism is recombination loss at dislocations which reduces the open-circuit voltage and increases the leakage current [15]. An enhanced carrier lifetime of InP on Si is desired for high performance photonic devices.

Here, we report on the investigation of depth resolved carrier dynamics in CELOG InP/Si direct heterojunction. By conducting low temperature cathodoluminescence (LT-CL) and time resolved photoluminescence (TRPL) line scanning on the cross-section of CELOG InP/Si, we study the impurity and defect related radiative recombination and non-radiative recombination through surface and interface states. The advantage of CELOG InP/Si for dislocation reduction and carrier lifetime enhancement is demonstrated. High crystalline quality InP/Si interface without threading dislocations and comparable to that of wafer bonded interface was revealed in transmission electron microscopy (TEM) studies. This study shows that the CELOG method to fabricate direct InP/Si heterojunction is promising for realizing III-V multi-junction solar cells and optical light sources on silicon.

2. Experiment details

A heterojunction of n-InP layer on p-Si substrate (n-InP/p-Si) realized via the CELOG method in an HVPE reactor is studied in this report. The n-InP layer was grown on a p-Si substrate patterned with InP-seed layers. The substrate processing included metalorganic vapor phase epitaxy (MOVPE) for the growth of the InP-seed on a (001) Si substrate (off-cut 4° toward [111]), plasma enhanced chemical vapor deposition (PECVD) for SiO_2 mask and Si_3N_4 spacers, photolithography, and inductively coupled plasma (ICP) etching of the InP layer to form the InP-seed mesa. Process flow of InP-seed mesa fabrication is shown Figs. 1(a)-1(d). A schematic of the InP-seed mesa pattern on Si processed for CELOG is shown in Fig. 1(e). The pattern consists of InP mesa (height = 2 µm) with Si_3N_4 spacer (sidewalls), where the silicon surface is exposed through the circular holes, of diameter 30 µm, arranged in a triangular lattice with center-to-center distance of 35 µm. Circular pattern is chosen to enhance the coalescence. CELOG on stripe openings were investigated [10,16]. We found that coalescence was hindered if the spacing between the stripes is too large and the lateral overgrowth rate is determined by the angle between stripe openings and [110] direction. By using symmetric circular opening, high rate lateral overgrowth front can be formed without intentional alignment of openings with respect to [110] direction.

The n-InP/p-Si CELOG growth in a HVPE reactor consisted of a semi-insulating InP:Fe (SI-InP, resisitivity ~10^8 ohm.cm) growth followed by n-InP (n = 7×10^{16} cm^{-3} quantified by Hall measurements), for 5 min. and 25 min., respectively. The CELOG growth was conducted at 590°C at the reactor pressure of 20 mbar; the InCl and PH_3 flows were 12 sccm and 120 sccm, respectively. A schematic of the CELOG InP/Si cross-section is shown in Fig. 1(f). The dislocations in InP seed mesas can propogate to the surface of growth but will not bend downward to the surface of Si substrate in the lateral overgrowth region. This heterojunction has been processed to build up a photodiode. N-type contact pads (150 µm × 150 µm) consisting of 90 nm AuGe/50 nm Ni/150 nm Au were formed on the n-InP surface

by e-beam evaporation and lift-off process. A 600 nm thick p-type Al contact layer was sputtering deposited on the back of Si, and then was annealed at 380°C for 5 min to make ohmic contacts. The growth details and preliminary electrical characterization results were discussed elsewhere [13].

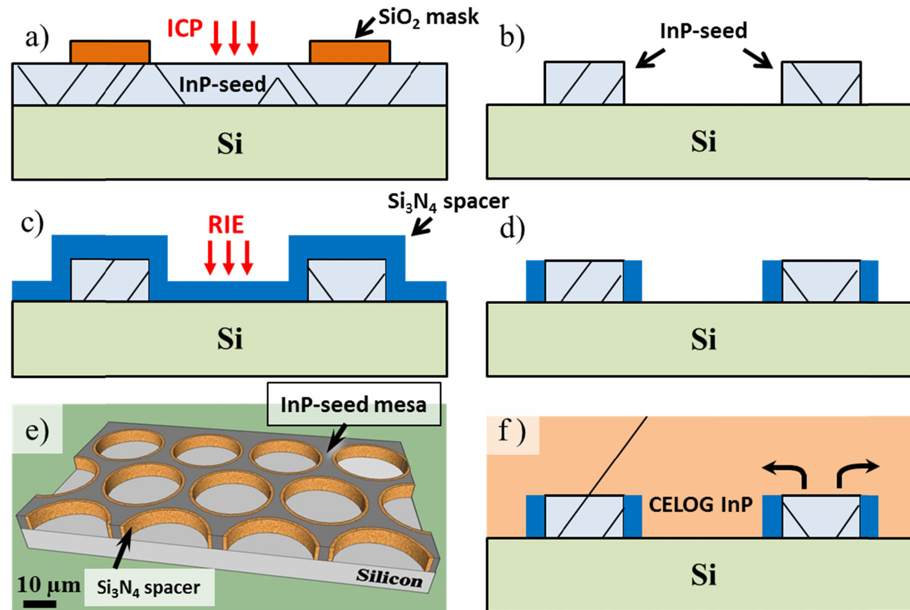

Fig. 1. (a)-(d) Process flow of InP-seed mesa fabrication for CELOG. (e) Schematic of the InP-seed mesa pattern on Si before CELOG. The thickness of InP-seed layer is 2 µm and the distance between the two adjacent circular rings, of diameter 30 µm, is 5µm. (f) Schematic of the CELOG InP/Si cross-section.

The surface roughness of CELOG InP/Si was characterized by atomic force microscopy (AFM). Here we focus on the characterization of the CELOG n-InP/p-Si heterojunction. The cross-section of the CELOG InP/Si was studied by spectrally resolved cathodoluminescence (CL) measurements using a MonoCL2 system (Gatan UK) attached to a LEO 1530 (Carl-Zeiss) field emission scanning electron microscope (FESEM). The CL signal was recorded with either an InGaAs photodetector (panchromatic images), or a liquid nitrogen cooled InGaAs array (CL spectra). The measurements were carried out at 80 K with the SEM operated at 10 keV. The CL probe depth in InP at 10 keV is ≈200 nm. In the hyperspectral mode the full spectrum of each pixel of a selected region of interest is acquired, which allows the construction of images for the different luminescence bands and their spectral parameters.

Recombination processes in CELOG InP/Si heterojunction were studied using time-resolved photoluminescence (TRPL) at room temperature. The measurements were performed using a femtosecond Ti:sapphire laser (100 fs pulse duration, 800 nm central wavelength, 76 MHz pulse repetition frequency) and a spectrometer-streak camera system. The time resolution of the experiments was 5 ps. The CELOG samples were mounted on a manual translation stage with 0.2 µm sensitivity, and the excitation beam was focused to a spot of 2.0 µm in diameter with a 40 × microscope objective. The average photoexcitation power was 0.5 mW, which, taking into account the reflection from the sample surface and averaging over two absorption lengths corresponds to a photoexcited carrier density of 4 × 10^{18} cm^{-3}. The crystallinity of the InP layer at the InP/Si heterojunction was characterized by a high-resolution transmission electron microscope (HRTEM). The TEM sample was prepared by mechanical polishing, dimple grinding and Ar ion milling. An ion energy of 4 keV was used for ion milling which was reduced to 2 keV when the perforation is reached.

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An FEI tecnai-F30ST with 300 keV electron emission was used to acquire the bright field (BF) images and selected area diffraction (SAD) patterns from the substrate, the film and the interface regions. The TEM sample was oriented to [011] zone axis to acquire the SAD patterns. The SAD pattern from the substrate was used to calibrate the camera length for precise measurements of lattice constant of the constituent materials at interface. A FEI Tecnai G2 Sphera TEM operated at 200 kV was used to acquire HRTEM images from the samples prepared by focused ion beam (FIB).

3. Results and discussion

The CELOG starts with selective growth of InP on the top surface of the InP-seed mesas. The growth then proceeds vertically and laterally and eventually downward to the Si surface to form a coherent InP/Si heterojunction. A uniform InP CELOG layer is formed on the Si substrate. Root-mean-square (RMS) roughness of the coalesced CELOG surface measured with AFM gave an average roughness of 39 nm for 20µm x 20µm scan windows. Although the rougness of CELOG InP/Si is rather high, it can be improved by subsequent chemical-mechanical polishing (CMP) conducted prior to the device fabrication.

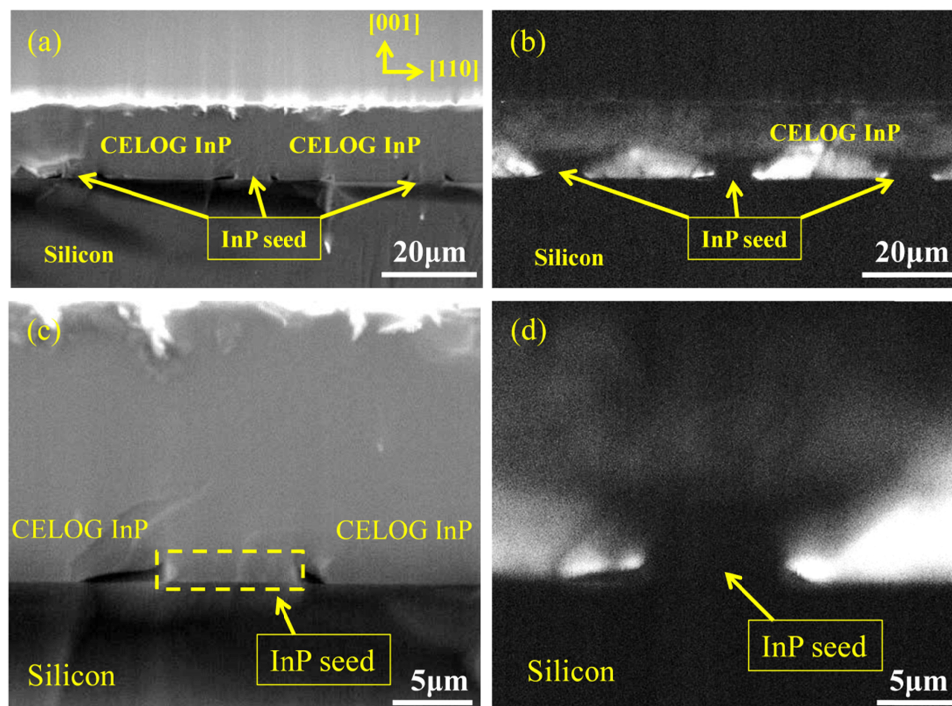

Fig. 2. SEM images (a, c) and the corresponding panchromatic CL images (b, d) of CELOG InP /Si cross section. Voids can be seen next to the seed in SEM images (a & c). The PanCL images were taken at 80 K.

Figure 2 shows the SEM images (a, c) and the corresponding panchromatic CL (PanCL) images (b, d) of the CELOG InP/Si cross section. From the SEM cross section images, Figs. 2(a) and 2(c), one can observe that a large CELOG region is formed with the exception of voids only close to the bottom of the InP-seed mesa covered by the Si_3N_4 mask. Void formation is understood to be caused by the CELOG growth fronts with low growth rate towards the seed but with faster growth rate away from the seed, which can cause materials reliability issues requiring further investigation. The voids have been present for the parameters studied in this work. By optimizing the V/III ratio and growth temperature, facet formation can be controlled and the void formation can be minimized, but this remains to be

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investigated. In the cross-section panCL images shown in Figs. 2(b) and 2(d) the bright CL regions correspond to the regions with reduced NRRC density, as compared to the dark contrast seen on the seeds, where a high concentration of NRRCs quenches the luminescence. This supports the arguments for a substantial reduction of dislocations in the CELOG layers in general. This reduction would account for the improvement of the crystalline quality of the CELOG layers with respect to the as-grown InP/Si heteroepitaxial layers, which present a high defect density resulting in an almost full quenching of the luminescence emission [17]. In particular, the InP/Si heterojunction region in the CELOG layer presents the highest CL intensity, supporting a substantial reduction of defects. There is no luminescence in the region of InP-seed, due to the high dislocation density. However, in the region above the seed, the luminescence starts to appear at around 5 μm away from the InP-seed/Si interface, and the intensity increases as the layer becomes thicker due to dislocation annihilation. The threading dislocations present in the InP-seed propagate during CELOG growth, but they escape upwards to the lateral regions of the seed. Since the dislocations cannot bend downwards to the Si surface, the CELOG regions close to the InP/Si interface are of good optical quality, as can be inferred from the brightest emission observed in the CL images.

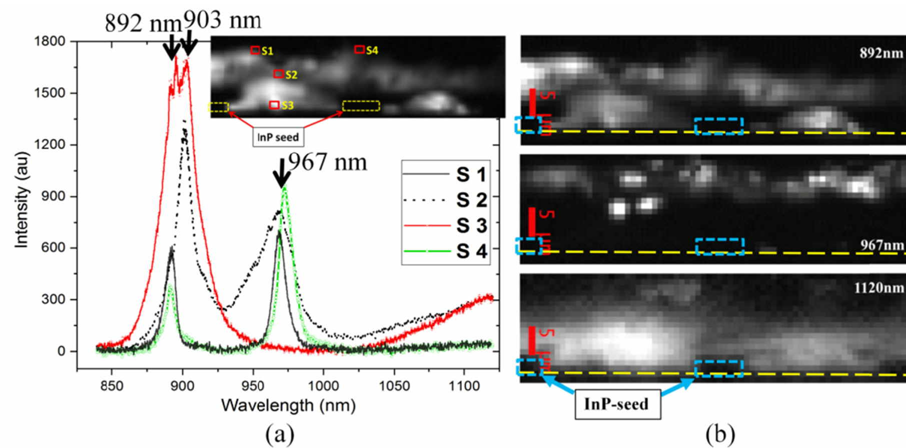

Fig. 3. (a) CL spectra measured at different sites (S1-S4) in the CELOG InP/Si cross section indicated in the panCL image in the inset. (b) Monochromatic CL images at wavelengths 892 nm, 967 nm and 1120 nm extracted from the spectral image. The yellow line markings in the CL image are the approximate position of InP/Si interface.

The hyperspectral image mode was used to collect spectral information at 80 K over a selected region of the CELOG samples. Electron-beam excitation causes the emission by all the luminescence mechanisms present in the semiconductor. Figure 3(a) shows the local CL spectra acquired at different positions in the CELOG InP/Si cross section indicated in the inset, the pan-CL image. The CL spectra present emissions at 892 nm (1.39 eV), 903 nm (1.37 eV), 967 nm (1.28 eV) and a broad tail at 1120 nm (1.107 eV). The spatial distribution of the different spectral parameters was extracted from the hyperspectral images. In particular, monochromatic CL images (peak intensity maps) taken from the CELOG cross section at wavelengths of 892 nm, 967 nm, and 1120 nm are shown in Fig. 3(b).

The images reveal a non-uniform distribution of different bands, which can be associated with the spatial distribution of the different defects involved related to the growth and processing steps. The CL emission at 892 nm (1.39 eV) is close to the band edge transition (BE) of InP at 80 K, which is 1.41 eV [18]. Note that this band can be shifted in the different regions of the CELOG layer, which can be associated with the presence of different levels of donors and acceptors. The 903 nm (1.37 eV) peak, along with 892 nm peak, was observed in the CELOG InP close to the InP/Si interface (S3, in Fig. 3(a)) but the former vanishes above

4 μm away from the interface. This suggests that 903 nm peak can be attributed to Si diffusion from the substrate into the CELOG layer [19,20]. Si incorporation into the CELOG region can also occur during growth, due to Si gas phase transport from the unmasked areas of the Si substrate [21]. As one approaches the top of the CELOG layer (S1 and S4 in Fig. 3(a)), a CL band peaking at 967 nm becomes dominant. As shown in the monoCL image in Fig. 3(b), the emission at 967 nm is relatively non uniform; it is mainly observed in the top part of the CELOG layer and even spatially anticorrelated with the distribution of the 892 nm band. The emission at 967 nm could be due to a donor level created by an oxygen atom replacing a P atom [22,23] during the metallization process of the PIN diode fabrication (which is not presented here). In fact, the samples were annealed at 380°C for 5 min to make the ohmic contacts after metallisation. Phosphorous out-diffusion and oxygen in-diffusion from the native InP oxide layer can happen during the annealing step. Such oxygen complexes are expected to be at higher concentrations close to the top of the CELOG InP/Si layer where the contacts were formed, and indeed it is so as observed in Fig. 3(b) (967 nm map). Finally, a broad band emission at about 1120 nm is also observed, as shown in the low energy tail of the CL spectra of Fig. 3(a). This band is often referred as C-band in InP and is attributed to a complex or pair defect involving species such as a donor like phosphorus vacancy (V_P) and an acceptor like indium vacancy (V_{In}) [24,25]. The intensity of the C-band emission is affected by the crystalline quality of InP, as observed in the mono-CL image. Its peak intensity in Fig. 3(a) in general is lower than the intensity of the other two peaks previously mentioned, but it is more conspicuous at the CELOG InP/Si interface region with respect to the other regions of the CELOG layer. The monochromatic CL images clearly establish the distribution of this band, which appears mainly localized at the CELOG region as Fig. 3(b) reveals.

To characterize the carrier dynamics and lifetime in the CELOG InP layers, TRPL measurements were carried out on the cross-section of CELOG InP/Si samples. Nonradiative recombination and trapping of carriers depend on the concentration of surface and interface defects, as well as point and extended defects in the bulk [26]. The PL decay time is determined by both radiative (τ_R) and nonradiative (τ_{NR}) recombination times via. $1/\tau_{PL} = 1/\tau_R + 1/\tau_{NR}$. Assuming that the radiative recombination time in bulk InP is spatially uniform, a longer PL lifetime is an indication of a reduced nonradiative recombination. For the same type of the prevailing nonradiative recombination centers, longer PL decay times indicate lower NRRCs density.

TRPL were measured on the (110) cross section surface along [001] growth direction above the CELOG InP/Si heterojunction (CELOG-scan) with a step size of 1 μm and above InP-seed region (seed-scan) with a step size of 2 μm. Position dependent PL decays are observed in both CELOG-scan and seed-scan as shown in Figs. 4(a) and 4(c). The TRPL decay curves in CELOG-scan measured close to the top of the growth surface and adjacent to the InP/Si interface show double exponential PL decay, as indicated by the decay curves measured at 3 μm and 21 μm from the InP surface as shown in Fig. 4(a). On the other hand, the TRPL spectra measured in the middle of the grown InP layer show single exponential PL decay. Such position dependent PL decay is also observed in seed-scan shown in Fig. 4(c). The single exponential PL decay process is dominated by bulk recombination with carrier lifetime τ, whilst PL transients yielding double exponential indicate two recombination mechanisms with a fast (τ_1) and a slow (τ_2) decay processes. The carrier lifetimes, τ_1 and τ_2, for double exponential decay and τ for single exponential decay extracted from the TRPL decay curves in CELOG-scan and the seed-scan are plotted as a function of the distance from the top of the growth surface in Figs. 4(b) and 4(d), respectively. The depth dependent carrier lifetimes in Fig. 4(b) and 4(d) can be divided in to three regions in both CELOG and seed-scans. In region I, within 7 μm below the top surface, the TRPL decay curves of both seed-scan and CELOG-scan show double exponential decays and both lifetimes, τ_1 and τ_2 increase with the distance from the top surface, which indicates that a similar decay mechanism

dominates in both regions. For region II in both the CELOG and seed-scans, i.e., the middle of the grown InP layers, a single exponential decay is observed. For CELOG-scan the carrier lifetime, τ, increases in this region with the distance from the surface, reaching its maximum of 700 ps at 15 μm from the surface and remains relatively constant until 19 μm. In seed-scan, the carrier lifetime τ increases with the distance from the surface and then decreases after a maximum at 600 ps at a distance of 10 μm. In region III close to the InP/Si interface, double exponential decay processes are observed in both CELOG and seed-scans. The width of region III in seed-scan is wider than that in CELOG-scan.

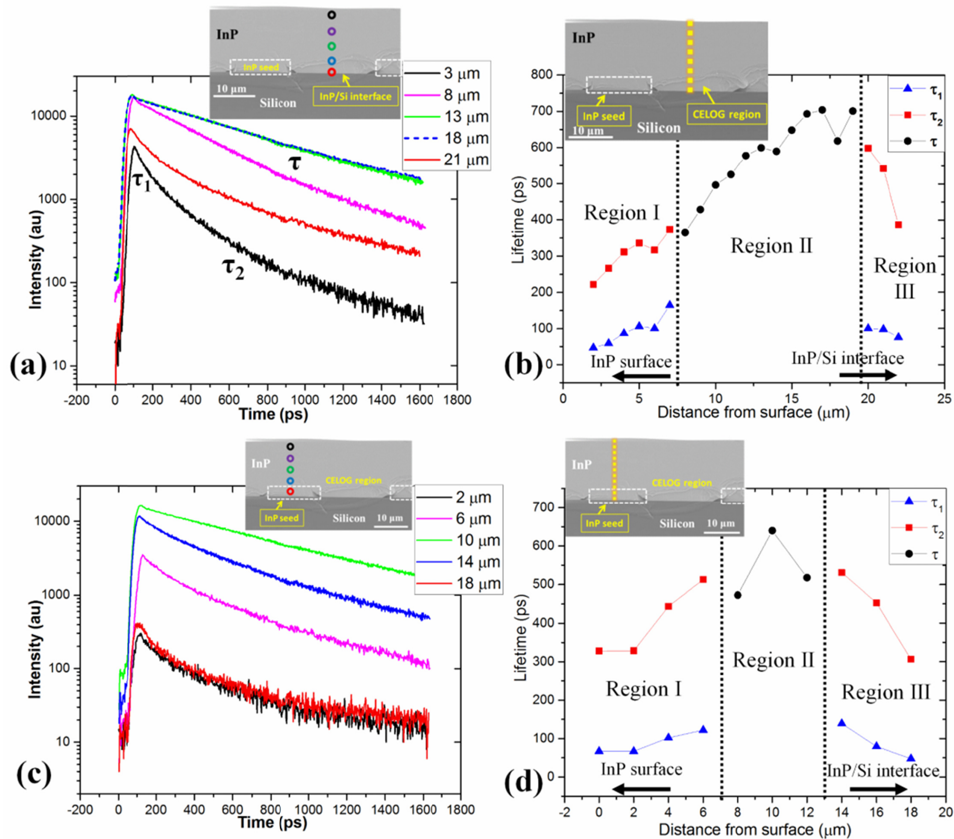

Fig. 4. Room temperature time resolved PL decay curves measured on the (110) plane of CELOG cross section vertically along (a) CELOG region (CELOG-scan) and (c) seed region (seed-scan). The measured points from where the TRPL were acquired are shown in the inset SEM image of CELOG InP/Si cross-section. The numbers in decay curves denote the distances of the measured points from the CELOG surface. Carrier life times extracted from the line scannings are shown in (b) and (d), respectively. The scanning lines are marked in the inset SEM image. The highest intensity and PL lifetimes are observed near the InP/Si interface of the CELOG region.

Similar depth dependent carrier lifetime variation has been observed in carrier dynamic studies of CdTe by 2-photon excited (2PE) TRPL with excitation spot smaller than the minority carrier diffusion length; which was attributed to photocarrier diffusion and surface recombination [27]. In the double exponential decays observed in region I in both CELOG and seed-scans, the faster decay part (τ_1) could be attributed to the carrier diffusion and surface/interface recombination [28]. This recombination mechanism becomes viable when the excitation spot is within the diffusion distance to the adjacent (001) surface containing surface recombination centers. With the excitation spot approaching the surface, a larger

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fraction of photoexcited carriers reach the surface and τ_1 decreases accordingly. The longer decay time component may also be affected by the carrier diffusion since the non-radiative recombination at (001) surface acts as a sink and increases the gradient in photo-excited-carrier concentration, which speeds up the diffusion process and thereby the PL decay.

The TRPL measured in region II shows single exponential decay and the carrier lifetime decreases toward the InP surface in both seed- and CELOG-scans (Figs. 4(b) and 4(d)). As shown in the CL characterization, Fig. 3, the progressive increase of the 967 nm band emission at 80 K towards the top surface suggests that the higher contribution of this recombination channel weakens the near band edge (NBE) emission, reducing the minority carrier lifetime in this region. The surface recombination at the (001) surface might also be affecting the PL decay in this region as deduced in the 2-D simulation of carrier dynamics in (2PE) TRPL experiments in semiconductors: it leads to an increase of the single exponential carrier lifetime, τ, when increasing the distance from the surface, reaching the maximum value once the surface recombination on (001) plane has negligible impact on the PL decay [27]. Such saturated carrier lifetime is only observed in region II in the CELOG-scan, while in the seed-scan it shows premature declination after reaching a maximum value of 640 ps. In region II of seed-scan, the higher lifetimes (~640 ps) observed away from the interface (around 10 μm) indicates better quality InP, which could be due to the annihilation process of dislocations propagating from the seed layer [29]. The InP growth starts on the defective InP-seed; as the growth proceeds, the threading dislocations propagating from the seed can get eliminated by creating dislocation loops for increasing InP layer thickness. In region II of CELOG-scan, the lifetime increases as the excitation laser spot approaches the InP/Si interface. The longest lifetimes (~700 ps) were observed from 5 μm to 2 μm close to the InP/Si interface. It indicates that the material near the interface has a low concentration of dislocations, which is consistent with the high CL intensity observed in that region of the CELOG layer (see Fig. 2). In this region, the original dislocations in the InP-seed layer were filtered away since the dislocations propagate only towards the top surface and cannot bend downwards to the surface of Si. Lifetimes near the CELOG interface are longer than the highest value in the seed-scan (~640 ps), which suggests that CELOG is more efficient in reducing dislocation density than the mere increasing of the layer thickness in InP/Si heteroepitaxy. In the seed-scan, the reduced carrier lifetimes in region III are due to the high density of dislocations (~10^9cm^{-2}) in the seed, which could cause nonradiative recombination. In CELOG-scan, as the excitation laser spot reaches further close to the interface (~2 μm from interface) or at the interface in region III, the lifetime drops, and the decay follows a double exponential. Misfit dislocations could be confined to the CELOG interface. Therefore, the faster decay near CELOG InP/Si interface might be due to non-radiative recombination at the InP/Si interface where dangling bonds associated with misfit dislocations are present. The CELOG InP/Si interface partially neutralizes the dangling bonds, thereby reducing the surface recombination velocity (SRV) as compared to the top surface, which will be shown in the TEM inspection of the InP/Si interface revealing a coherent InP layer epitaxially fused to Si. Therefore, the depth dependent carrier lifetime distribution can only be seen in a narrow region close to the InP/Si interface in CELOG-scan. This difference in the SRV of the InP/Si interface and the InP top surface is the reason for the lifetime differences observed in the top and the interface regions in the CELOG-scan.

In Fig. 5, the carrier lifetimes of CELOG InP/Si layers are compared with that of direct heteroepitaxial InP/Si by MOVPE (InP-seed/Si). The carrier lifetime on the (001) surface of CELOG InP/Si (denoted as *CELOG top* in the figure) extracted from a single exponential decay is 745 ps. The decay curve measured close to this site but on the (110) cross-section (denoted as *CELOG CS_2 μm*) is double exponential and the lifetime of the lower decay rate is 220 ps. Because of the proximity of the measurement sites the lifetimes are expected to be the same in contrast to what is being observed. This suggests that the active contribution of carrier diffusion to the (001) surface and surface recombination could reduce the carrier

lifetimes measured at the (110) cross section near the InP top surface. As expected, the TRPL spectrum measured on the surface of InP-seed/Si grown by MOVPE has a significantly shorter carrier lifetime of ~150 ps due to the high density of threading dislocations. The carrier lifetimes in heteroepitaxial InP measured on CELOG (001) surface and near the InP/Si interface in (110) cross-section (*CELOG CS_19 μm*) have shown improved values, 710-745 ps accounting for the reduced dislocation density. These values are still less than what we obtained for homoepitaxial InP grown on planar substrates (2-6 ns depending on the doping concentration) but are comparable to heteroepitaxial InP on Si with an estimated dislocation density of 10^7/cm^2 according to a model [15]. Photo-carrier diffusion and surface recombination can affect the accuracy of the carrier lifetime measured by TRPL technique. Double heterostructures have been used in GaAs TRPL measurement for accurate carrier lifetime measurement [30]. Carrier diffusion to InP/Si interface and recombination with interface states could affect the accuracy of the estimated carrier lifetime in this region and a higher carrier lifetime value could be expected if an appropriate carrier confinement can be realized at InP/Si interface to eliminate diffusion effects.

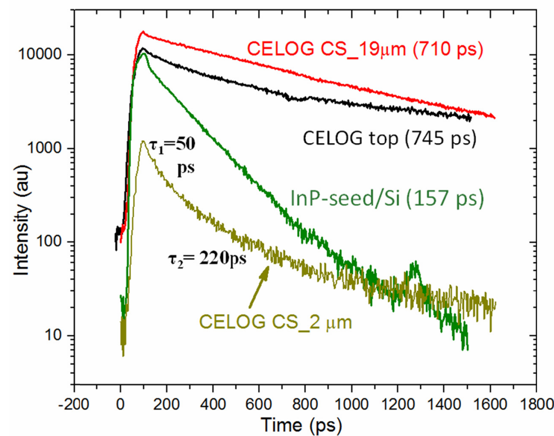

Fig. 5. Time resolved PL decay curves of CELOG InP/Si and InP-seed/Si. *CELOG top* refers to the measurement on top (001) surface of 20 µm thick CELOG surface; *CELOG CS-19µm* and *CELOG CS-2µm* refer to the measurements on the (110) cross sectional surface at 19 µm and 2 µm from the top surface, respectively.

The crystalline quality of the CELOG InP/Si interface was inspected by cross-sectional TEM. In earlier studies, on uncoalesced CELOG InP/Si realized on linear seed patterns, stacking faults were observed in the CELOG interface region [10,16]. On the contrary, neither stacking faults nor threading dislocations are observed in the InP CELOG regions in this sample (Fig. 6(a)). The contrast variation in the image is due to the changing thickness of the TEM sample. The InP-seed layer grown by MOVPE presents a high dislocation density (~10^9cm^{-2}) due to ~8% lattice mismatch [31]. A network of threading dislocations and stacking faults (SFs) has been observed in the InP-seed layer. The CELOG InP growth initiates by nucleating on the surface of InP-seed and the growth proceeds laterally from the growing InP facet planes, which eventually grows downward to reach the Si substrate. The growing InP crystal gets bonded with the Si surface at high temperatures which facilitates the formation of atomic bonds between InP and the Si substrate, in a similar way to the wafer bonding process.

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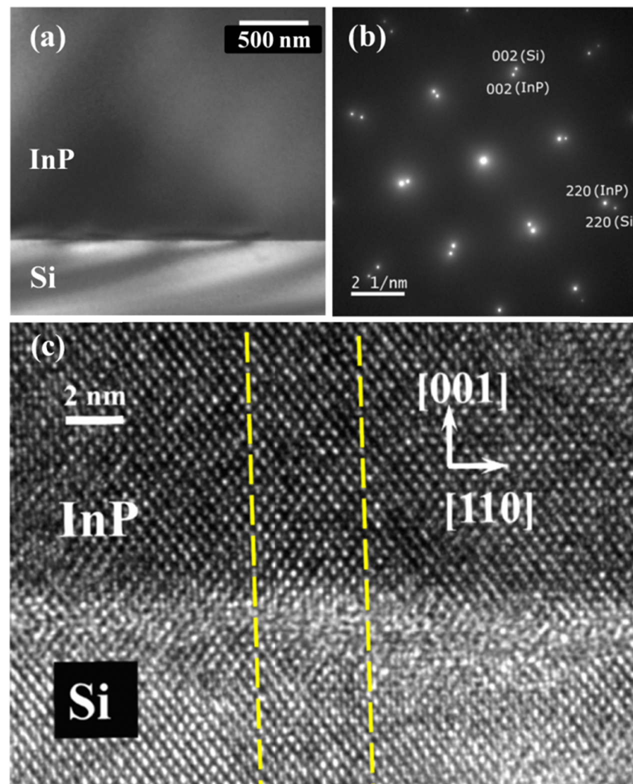

Fig. 6. (a) Bright field TEM image showing the smooth interface between InP and Si in the CELOG region. No threading dislocations contrast is observed in the InP film. (b) Selected area electron diffraction pattern acquired at the film-substrate interfacial region. (c) HRTEM cross section of CELOG InP/Si interface. The yellow lines marked in the HRTEM are parallel to (110) atomic planes. By counting the number of (110) planes between the lines in both layers, one missing plane in the InP layer can be inferred.

Taking the dimensions of the bright field TEM image shown in Fig. 6(a) and a sample thickness of 200 nm, a maximum threading dislocations density of ~3×10^8 cm^{-2} can be expected in the CELOG region. Figure 6(b) shows a selected area diffraction (SAD) pattern taken from the film-substrate interface in the CELOG region. In the SAD pattern, the reflections originating from both the Si substrate and the InP film are clearly separated from each other, which indicates a coherent InP/Si interface without amorphous layer. The InP reflections follow the expected cubic symmetry which shows that the film is highly crystalline. The atomic arrangement in the InP layer corresponding to the arrangement of Si atoms in the substrate is characterized by cross-sectional high resolution TEM (Fig. 6(c)). The number of (110) atomic planes in both silicon and InP layers are counted, as indicated between the parallel lines in the Fig. 6(c). A period of 14 (110) InP planes is matched to a period of 15 (110) Si planes at the interface, which corresponds to the ratio of lattice constants of InP (5.8687 Å) and Si (5.431 Å). Misfit dislocations should exist at the interface of InP/Si, but are not visible in the HRTEM image. The 8% lattice mismatch between InP and Si was accommodated by these misfit dislocations where there is one less {110} InP atomic plane in the CELOG layer, with respect to the Si atomic planes, every 5 nm distance at the InP/Si interface. In contrast to direct heteroepitaxial growth, where each misfit dislocation leads to two threading dislocations which thread toward the top surface, these misfit dislocations are edge dislocations confined only to the InP/Si interface. Misfit dislocations created at the interface in CELOG process do not generate threading

dislocations. They are confined to the interface as in wafer-bonding technology [32]. The CELOG process appears as a bonding process taking place during the growth, as if the growing InP layer is fused to the Si surface at high temperatures. The results of Matsumoto et al. indicate that subsequent epitaxial growth on bonded wafer can cause dark line defects due to thermal mismatch [33]. In our case the heterointerface is already formed at high temperature and hence low risk for threading dislocation during subsequent growth of e.g. laser devices. Off-cut Si substrate was used to avoid APDs (antiphase domains) in the InP-seed grown with MOVPE. No APDs were observed in the CELOG region by TEM and CL.

4. Conclusions

We studied monolithically integrated InP/Si heterojunction with high crystalline quality InP and coherent InP/Si interface realized by self-aligned corrugated epitaxial lateral overgrowth (CELOG) method in HVPE. CL spectra acquired at 80 K in different regions of the CELOG cross-section present following transitions: 1) near-BE band at 892 nm (1.39 eV); 2) a band at 903 nm (1.37 eV) related to Si diffusion from the Si substrate; 3) a band peaking at 967 nm (1.28 eV) associated with an oxygen donor level due to replacement of P site; 4) a broad band around 1120 nm (1.11 eV) attributed to a complex defect pair, due to donor like V_P and acceptor like V_{In}. The intensity distribution of these emissions has been studied by hyperspectral CL images. The monochromatic CL images of 892nm and 1120 nm emissions taken on the cross-sections showed strong contrast between CELOG regions (bright) and defective seed regions (dark), suggesting high crystalline quality InP/Si heterojunction in the CELOG region. The depth dependence of InP carrier lifetime in CELOG InP/Si cross-section was measured at room temperature by time resolved photoluminescence. Depending on the positions, single and double exponential decays were observed, and the related recombination mechanisms have been discussed. An enhancement of carrier lifetime was observed near the CELOG InP/Si interface with respect to seed layer accounting for its better crystalline quality. We notice that the value of carrier lifetime measured by TRPL at the cross-section of CELOG InP/Si is affected by photo-carrier diffusion and associated non-radiative recombination through surface states on (001) InP plane and interface states in the misfit dislocation network at InP/Si direct heterojunction. Appropriate carrier confinement structure would be essential for enhancing carrier lifetime in CELOG InP/Si heterojunction. TEM characterization also revealed high crystalline quality of InP at the CELOG InP/Si interface without threading dislocations in the InP layer, but misfit dislocations presumably exist at the interface as shown in cross-sectional HRTEM in a manner observed in wafer bonding heterointerface. The selected area electron diffraction pattern acquired at the film-substrate interfacial region has revealed a coherent CELOG InP/Si interface free of amorphous layer. This work has demonstrated that CELOG is an efficient method for dislocation reduction and carrier lifetime enhancement in heteroepitaxial InP growth on Si. Location-dependent multiple bands and dislocation densities in this approach cause challenges to the devices grown on CELOG. Chemical mechanical polishing (CMP) will be used to remove the top layer of InP to expose the high quality CELOG region. Devices will be fabricated on the CELOG region by isolating the seed regions from electrically active regions. Ideally the seed site and its pattern density should be small to achieve large area CELOG region for planar photonic devices. But these have not been investigated in detail in this work. As shown in this work, the regrown materials in CELOG region have high crystalline quality but they will be isolated islands after CMP to expose the CELOG layer, which are separated by defective InP seeds. Large area and uniform low dislocation InP layer on Si are desired for in-plane photonic integrated circuit (PIC) applications. By conducting InP planarization growth after removing the original InP seeds between CELOG InP islands, a uniform high crystalline quality InP/Si layer can be expected. The CELOG approach is generic and can be extended to the formation of other III-V/Si heterostructures. Thus III-V material with long carrier lifetime on silicon fabricated by CELOG method will facilitate the

realization of cost effective integrated photonic devices and III-V multi-junction solar cells on silicon with bandgap combinations desirable for high efficiency.

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Disclosures

The authors declare that there are no conflicts of interest related to this article.

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