Budapest University of Technology and Economics
Faculty of Electrical Engineering and Informatics
Department of Electron Devices

MSc THESIS

MSc degree in Electric Engineering

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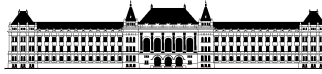
BUDAPEST, 2015



MSc THESIS TASK DESCRIPTION

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candidate for MSc degree in Electrical Engineering

Preliminary investigations on Thermal Electric Devices

Until now, the continuous development of electronics has been characterized by Moore's law. The scale down resulted in the nanosized CMOS integrated circuits, pushing the "red brick wall" towards the lower dimensions.

Although the current CMOS integrated circuit development is driven by a lot of innovations, there are still some limits determined by unavoidable physical effects such as tunneling of charge carriers through thin insulating regions and statistical irregularities in the number of dopant atoms.

There are many new ideas for building atomic or molecular scale devices for the information technology. However, there is still a gap between the up-to-date "top-down" CMOS technology and the "bottom-up" devices, i.e. molecular electronics, nanotubes, single electron transistors. The new thermal-electric device (phonsistor) and the CMOS compatible thermal-electric logic circuit (TELC) may help to fill this gap. The device is based on the semiconductor-metal transition (SMT) effect shown by certain materials. This effect allows an electric resistance change in three-four orders of magnitude induced by thermal or electrical excitation.

Tasks of the student:

- Present a comprehensive review on thermal electric devices and circuits
- Study and analyze some experimental thermal electric devices (VO_2) structures
- Evaluate results, give suggestions for extension of investigation.

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Budapest, 7 March 2014

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PRELIMINARY INVESTIGATIONS ON THERMAL ELECTRONIC DEVICES

SUPERVISOR

Dr. Mizsei János

BUDAPEST, 2015

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STUDENT DECLARATION

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Jesús Antonio Méndez Puertas

Summary

A study of the possibilities and developments of the electronic thermal devices is presented. Mainly, it is focused on the review of the principles and previous investigations on the thermal integrated switches based on the novel vanadium dioxide material, that presents a semiconductor to metal state phase transition around 68ºC.

In order to prove the viability of the thermal integrated logic circuits, basically consisting on thermal logic gates made of phonsistors, it has been experimentally tested, using a heating plate and a source meter, a single SMT (Semiconductor to Metal Transition) switch and a thermal logic gate structure, based on a platinum contacts geometry deposited on a VO_2 thin film over a silicon substrate.

The experiments revealed the correct operation of the VO_2 switch, proving the previous studied theories, as the resistance change and the reason that produce the transition activation. Also, the NOR logic function was proved on the thermal logic structure, using current driven inputs and a pull-up resistor in the output. The results acquired present the possibility of creating thermal logic gates and electronic circuits based on the phonsistor scheme. Further investigations building nanoscale structures, which would improve the performance, could be done to test the minimum switching times and the power consumption that would have the thermal logic technology.

Keywords: thermal logic circuits, vanadium dioxide (VO_2) switches, thermal logic gates, VO_2 thin films, phononic computing

Resumen

Se muestra un estudio acerca de las posibilidades de desarrollo de los dispositivos electrónicos térmicos. Principalmente, centrado en los principios y las investigaciones previamente realizadas en los conmutadores integrados térmicos, basados en el novedoso material Dióxido de Vanadio, que presenta una transición de fase del estado de semiconducción al metálico en torno a los 68ºC.

Para probar la posibilidad de realizar los circuitos integrados lógicos térmicos, consistentes principalmente en puertas lógicas hechas con “phonsistors”, ha sido probado experimentalmente un conmutador SMT (Transición de Metal a Semiconductor) y una estructura de puerta lógica térmica, basada en una estructura de contactos de platino depositada en una capa fina de VO_2 sobre un sustrato de silicio.

Los experimentos realizados, mostraron la correcta operación del conmutador VO_2, probando las teorías presentadas con anterioridad, como el cambio de la resistencia y las causas que provocan la activación. Además, la función de la puerta lógica NOR es probada en una estructura de lógica térmica, usando entradas activadas por corriente y una salida con una resistencia de pull-up. Los resultados obtenidos presentan la posibilidad de crear puertas lógicas térmicas y circuitos basados en el esquema de los “phonsistors”. Posteriores investigaciones para construir estructuras a tamaño nano, que podrían mejorar las prestaciones del sistema, podrían ser llevadas a cabo para probar los tiempos mínimos de switch de las puertas y el consumo de potencia que tendría la tecnología de lógica térmica.

Palabras clave: Circuitos Lógicos Térmicos, Conmutadores de Dióxido de Vanadio (VO_2), Puertas Lógicas Térmicas, VO_2 Thin Films, Computación de Phonones

1 Introduction

Although the CMOS technology is the most extended nowadays on the integrated electronic circuits, some new technologies are been investigated to fight the impossibilities in the size reduction and improving aspects as the operation frequency and the power consumption of the CMOS technology.

The thermal logic circuits could solve the developing problems of the CMOS technology, which is built mainly out of phonsistor devices based on the SMT materials, such as the vanadium dioxide. The vanadium dioxide presents a resistance change of several orders of magnitude at a temperature of approximately 67ºC. Some new technologies are carbon nanotubes, molecular electronics and nanowire FET.

The purpose of this thesis is to present the principles and previous investigations on the thermal circuits, and to show afterwards the experimental tests on a VO_2 thin film with platinum contacts structure, trying to prove the possibility of building thermal logic integrated circuits based on the phonsistor device.

Firstly, it is discussed the previous investigations on phononic computing, introducing the necessary building blocks to achieve it, which are the thermal diodes or thermal rectifiers, the thermal transistors (based on the Negative Thermal Differential Resistance (NDTR)), the thermal gates and finally the thermal memories.

Secondly, it is showed the Mott transition principles and the characteristics of the MIT/SMT transition in the Vanadium dioxide (VO_2), which is basically a Mott transition. The third chapter deals with the design of the VO_2 based switches, starting with the possible deposition techniques for creating the VO_2 thin films and the metallic contacts, and ends presenting some previous investigations of several thermally, electrical and optical driven VO_2 switches. Also, the two main theories of the switching mechanism that induces the MIT in the electrical switching (the Joule heating and field effects), are reviewed.

Finally, it is examined the thermal logic circuit (TELC) proposal, in which the thermal gates and thermal switch tested are founded. The measurements made on a

VO_2 thin film with platinum contacts and the results achieved are exposed in the last chapter.

2 Basic devices for managing heat conduction

2.1 Introduction

In the last decade there has been some investigations in the field of the thermal conduction, trying to demonstrate the possibility of building thermal logic gates and devices, which are able to control the heat flow, as their electronic counterparts [4]. The reason why electronic devices have been early developed it is because is much harder to control de flow of heat than the flow of electrons, since phonons (the carriers of heat) are not defined particles but bundles of energy unaffected by electromagnetic fields without mass or charge [5].

Some thermal rectifiers have been proposed and built, by using the property of temperature-dependent power spectra in nonlinear lattices [4], as well as molecular thermal devices that pump heat from a cold to a hot tank.

Moreover, researches based on the new phenomenon of negative differential thermal resistance, have recently built and create models for thermal diodes, thermal transistors, thermal logic gates and thermal and thermal memories, which are the basic components of functional thermal devices [4]. These components add a new physical dimension to information processing in addition to electronics and photonics, eliminating the long regarded view as useless of the heat in electronic circuits [5].

These introduced elements and concepts will be explained in detail below, starting from the thermal diode and finishing with the thermal memories.

2.2 Thermal diode

A primary building block for phononics is a device that rectifies the heat flow, i.e., a thermal rectifier or diode [5]. This device conducts heat in only one direction. The directional thermal effect was firstly observed by the physicist Chauncey Starr in a copper-cuprous-oxide interface. The device models at that time had not any rigorous theoretical foundation such as nonlinear dynamics or computing simulate process [5].

2.2.1 Three segment thermal diode 2002

In 2002 a more serious model for a thermal diode based on resonance was proposed by Terraneo, Peyrard and Casati, based on the possibility to control the energy transport inside a non-linear material one dimensional chain, with a resonant frequency that depends strongly on temperature, connecting two nearly linear segments (thermostats) at different temperatures, which resonant frequencies hardly varies with temperature [1][5].

In the research was observed that the heat flux increased by raising the temperatures of the thermostats and keeping constant the temperature difference, or acting on the properties of the chain. Consequently it allows the system to behave as a common conductor down to an almost perfect insulator [1].

The principle of the thermal rectifier was that when the resonant frequencies or phonon bands of the three regions matched, the heat flux was possible.

When the power spectrum in one part of the device matches that in the neighbouring part, it is found that heat energy is exchanged efficiently. In the absence of such overlapping of the spectral properties, the flux of energy becomes strongly weakened [6].

2.2.2 Two segment thermal diode 2004

Then Casati and other Scientifics in 2004, proposed a model for a thermal diode, which was demonstrated via computer simulation. The system was formed by two segments of nonlinear lattices connected by a harmonic spring with constant strength k_{int} [2]. Each segment is composed of a chain of particles, joined each other by linear springs [6], this segments are described by Hamiltonian of the Frenckel-Kontorova (FK) model which is supposed to have heat conduction [2].

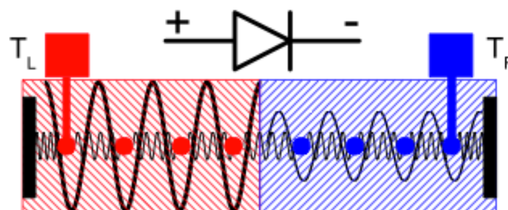

Figure 2.1: Scheme of the thermal diode [6]

After the numerical simulations, fixing the parameters to simplify, using Langevin heat baths, and integrating the differential equations of motion by using the 5th-order Runge-Kutta algorithm [2]; it was shown that the local heat flux varies with the temperature gradient Δ ($T_L - T_D$) and the temperature T_o, this is depicted in Figure 2.2.

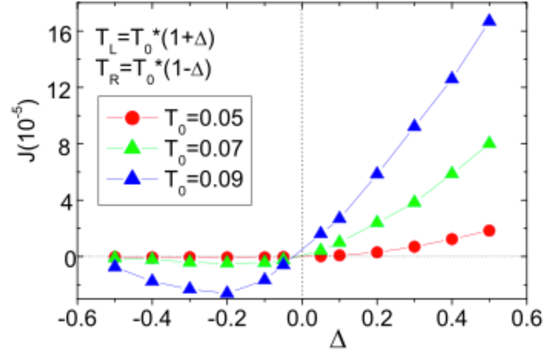

Figure 2.2: Heat current J vs. Δ, for different values of T0 [2]

As it is shown in the plot, when $\Delta > 0$ the heat current increases proportionally with Δ, while in the case of $\Delta < 0$ the heat currents is approximately zero. Thus, when $T_L > T_R$ (heat flow J_+), the thermal diode conducts properly, and in the case of $T_R > T_L$ (heat flow J_-), the heat flux is very poor, so it exists a rectification in the conduction between both heat current directions, $|J_+/ J_-| > 0$.

For setting up the rectifier efficiency of the diode it must be observed some parameters, such as the temperature T_o, the interface elastic constant k_{int} and the effect of the lattice parameter λ, which refers to the strength of the on site potential.

K_{int} controls the heat flux and consequently the rectifier efficiency $|J_+/ J_-|$, in the simulations it was proved the variation of the rectification from 2 with k_{int}=0.5 up to 100 for k_{int}=0.01. Varying λ also was clearly shown that in a wide range of parameters the model had a quite good rectifying efficiency of almost 100 [2].

To understand the rectifying mechanism of this model, it must be taking in account the phonon spectra of the left and right interface particles at the different temperatures, in which the thermal diode works. On one hand, at low temperatures the particles are confined in the valley of the on-site potential which produces a weigh power spectrum in the high frequencies and on the other hand when the temperature

becomes higher the particles acquired enough kinetic energies for the thermal activation across the barriers [2], what means a movement of the power spectrum to lower frequencies.

The frequency range of the power spectrum of both segments controls the heat flux, since the more power spectrum overlapping, the more heat conduction. To get the desired strong thermal rectification, the strength of the on site potential in the two sides is set at different levels, more specifically the barrier height of the on-site potential for the right segment is chosen small [6], so it allows the particles to move almost freely, both in the low and in the high temperature regimes, which produces that the spectrum of the right side will be in lower frequencies as we can observe in Figure 2.3.

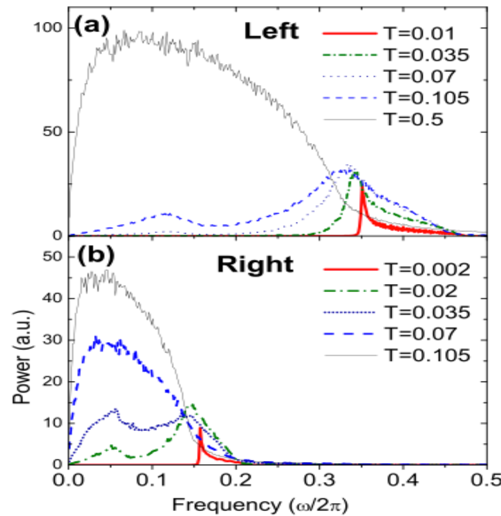

Figure 2.3: Spectra of the two particles at the interface for different temperatures [2]

A few years after the theoretical models of the thermal rectifiers presented above, some experimentally thermal rectifiers have been built, for example a nanoscale solid-state thermal rectifier has been demonstrated experimentally by asymmetrically deposited carbon and boron nitride nanotubes, the responsible of the rectification phenomenon is thought to be the solitons [7].

2.3 Negative differential thermal resistance: Thermal transistor

Once some models of thermal diodes has been presented as well as some experimental thermal rectifiers. The next aim to raise the thermal logic circuits is to create a thermal logic transistor, which controls heat current, analogous to the field-effect transistor that controls the flow of electric charge.

The thermal transistor is able to control the heat flux from the hot segment (source) to the cold one (drain), applying a control temperature to a point in the middle (gate). As well as the field-effect transistor the thermal transistor also must have a current gain; it means that changes in the heat current through the gate produces a larger increase in the heat flux from the drain to source.

In 2006 Li, Wang and Casati proposed a model for a thermal transistor consisting of three segments drain (D), source (S) and gate (G), following the notation in a MOSFET. Each segment is a FK lattice, as in the 2004 model of thermal diode. Segment D is connected with S via a spring with k_{int} constant and G is joined via another spring to a particle O in the middle of D and S [3], as it is shown in Figure 2.4.

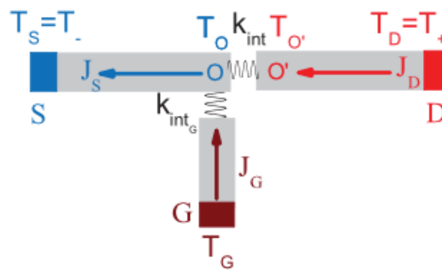

Figure 2.4: Scheme of thermal transistor [3]

They made several numeric simulations using the Hamiltonian model for the segments, supposing that the lattices were coupled at their first particles, using Langevin heat baths and connecting T_+=0.2ºC and T_-=0.03ºC [3]. These simulations revealed that the thermal transistor model can act as a thermal switch, with heat flux ratio between off and on mode of 100, as well as a thermal current amplifier, just adjusting the parameters values, in this case the only difference in the parameters for both function was the spring constant K_{intG}.

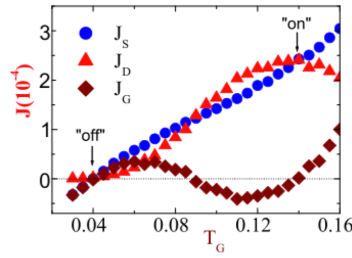

Figure 2.5: Heat flux vs. control temperature T_G, k_{intG} =1 [3]

There are three working points for T_G=0.04, 0.09 and 0.14, where J_D=J_S, these points corresponds to the off state (stable), semi-on state (unstable) and on state (stable).

The transistor function is based on the Negative differential thermal resistance (NDTR) that occurs at the interface between O and O′. When the T_G increases (T_o is close to T_G), it reduces the temperature difference $T_D - T_O$, which we could expect to produce a decreasing in J_D, however, as observed in Figure 2.5, it is seen that the current flux J_D increases with T_G. This fact is due to the FK lattice non linearity in segment D. It is expected that NDTR effect can experimentally be found in nanoscale materials such as nanotubes, nanowires, etc [6].

2.4 Thermal logic gates

Thermal logic gates based on thermal transistors are possible due to the NDTR effect, when heat flow J_D increases due to an increase in T_G, it produces an increase in the temperature difference $T_D - T_O$, and consequently $T_{O'}$ decreases. Thus, $T_{O'}$ changes in the opposite way of T_G.

First of all, as in electronic logic, two standard values are used for representing high and low level, which are T_{off} (0.03ºC) and T_{on} (0.16ºC) [4]. The basic element for achieving the thermal logic is the signal repeater, which is a two terminal device that standardize the output to T_{off}/T_{on} depending if the input is below or above a threshold temperature T_c (semi-on state), respectively. The principle is that when T_G changes slightly it produces a higher change in T_O, which makes T_O be closer to the stable temperatures. This repeater is build by connecting several thermal transistors in series, using the input G and the output O. The characteristic of the device is close to an ideal repeater.

The next basic element used in this thermal logic proposal is the temperature divider, which behaviour is similar to a voltage divider; the output temperature is an adjustable fraction of the input temperature.

The thermal NOT gate is made of a thermal transistor, using the input G and as output O' [4], since as it was explained before, an increasing in T_G generates a reduction in the value of $T_{O'}$, and vice versa, which means a negative response. The output O´ is always higher than T_{on}, therefore with the divider, the temperature is made lower or higher than T_c and then it is connected to a thermal repeater to normalize the output value to $T_{off}/T_{on.}$

Finally the thermal AND/ OR gate can be realized connecting the output O of two thermal transistors, via two thermal dividers to a single thermal repeater [4], as depicted in Figure 2.6. In both gates when the two inputs are T_{off} /T_{on} the output is T_{off}/T_{on}, to made the output T_{on} or T_{off} when the inputs are different it is just necessary to adjust the rate of the temperature divider.

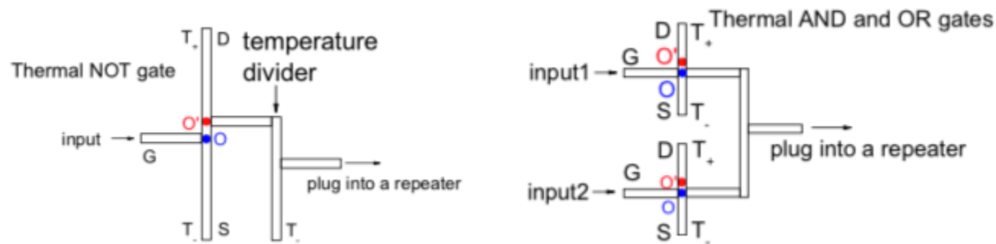

Figure 2.6: Scheme of Thermal NOT/AND and OR gates [4]

2.5 Thermal memories

Thermal memories are the last elements necessary for achieving the phononic computing, this device is supposed to storage the information encoded in temperature states.

In [8] it is proposed a model of thermal memory based on the thermal transistor, showed in the chapter 2.3. The node S and D of the thermal transistor model are fixed to a constant temperature $T_D>T_S$, and the parameters adjusted. After these, it appears three working points for T_G, which are T_{off} , T_{on} (stable) and $T_{semi-on}$ (unstable), where $J_G=0$, perfectly balancing J_D and J_S. These three working states keep constant even if the heat bath in G is removed, it means that the last temperature

coupled to G is saved, which is the required function of the thermal memory. Moreover, if small fluctuations of the working points temperature appear, the system goes back himself to the stable working points, so the thermal memory system can remain the working temperature unchanged for a long time, in spite of some perturbations that could be applied [6].

A scheme of the thermal memory working process is depicted in Figure 2.7, where the Boolean temperatures available to write are T_{off} and T_{on}. In the writing cycle the temperature is coupled to G/O point, after, the writer is removed and the temperature memorized is maintained until a new writing process. For the reading cycle, the reader, i.e. a small thermometer, is connected to the point G/O, in this process, the temperature T_O is self-recovered [8], as it was already mentioned, keeping the temperature invariable.

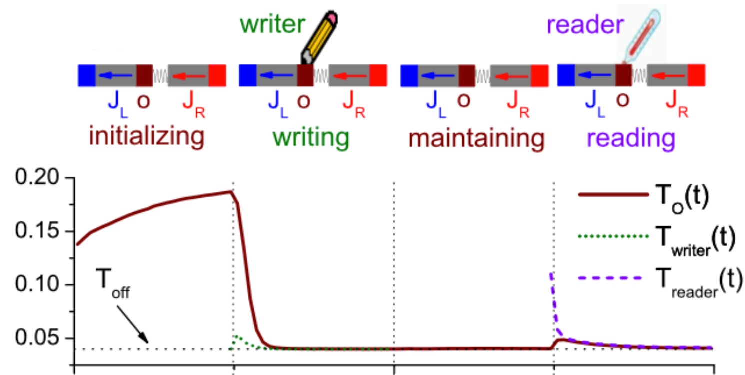

Figure 2.7: Thermal memory writing/reading process for an ´off´ state [8]

3 MIT (Metal insulator transitions)

3.1 Mott transition

Generally, materials can be differenced either to be an insulator or metal, depending on the position of the Fermi level in the band structure. This model is not sufficient in some cases, since it neglects the Coulomb interaction between electrons (electron correlation).

In materials, which should be a metal, with half filled conduction band, when the electrons hop from a site to a new one, which is already occupied by an electron, they can experience Coulomb repulsion from the electron sited in the new place. If the Coulomb repulsion energy (U) is larger than the electrons kinetic energy, it could drive to bound the electrons to their original site instead of being freely moving for conduction. This effect can be explained as a split of the single half-filled band into a full lower band (lower Hubbard band, LHB) and an empty higher band (upper Hubbard band, UHB) [13], with a band gap equal to the energy U, turning the material into an insulator.

Due to the screening, if the total electron density is increased the Coulomb repulsion will be lowered, and in a critical value the split bands could be merged leading to an insulator to metal transition. The Coulomb repulsion is relative to the band bandwidth (W), as we can observe in Figure 3.1. In transition metal oxides, with bandwidth of 1-2 eV and Coulomb energy 1-10 eV, the band gap is significant, however for conventional semiconductors Si and Ge, the bandwidth is usually 10-20 eV [13], so the Coulomb repulsion can be neglected.

Mott transitions can be induced by tuning the relation between the Coulomb energy and the bandwidth, for example applying stress to the material, or via changing the carrier density, in the last case for the transition to occur, it is needed to satisfy the equation $n_c^{1/3} a_H \sim 0.25$ [13].

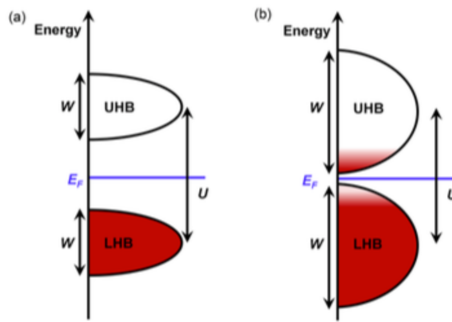

Figure 3.1: Split of the band due to Coulomb repulsion [13]

3.2 MIT in VO_2

Vanadium dioxide is an intensively studied material, which undergoes a reversible metal to insulator phase transition, which occurs at a temperature near 68ºC. The transition produces several changes, which are a lattice structural transition from monoclinic to tetragonal, changes in the electronic properties, since the electrical resistivity increases by 3 to 5 orders of magnitude, and variations in the optical properties, such as the optical reflectivity, at almost all wavelengths [14][10]. Doping the VO2 films and varying the film size, the transition temperature and the switching characteristics can be altered [15].

Although the transition is reversible, it exists a remarkable hysteresis, with widths that varies from approximately 1ºC in bulk crystals to 10-15ºC in thin films [15], and can be even larger in VO_2 nanoparticles. In Figure 3.2, it can be observed the hysteresis phenomenon in the graphics of the electrical resistance and optical reflection, measured for thin films of VO_2 with 100 nm thickness.

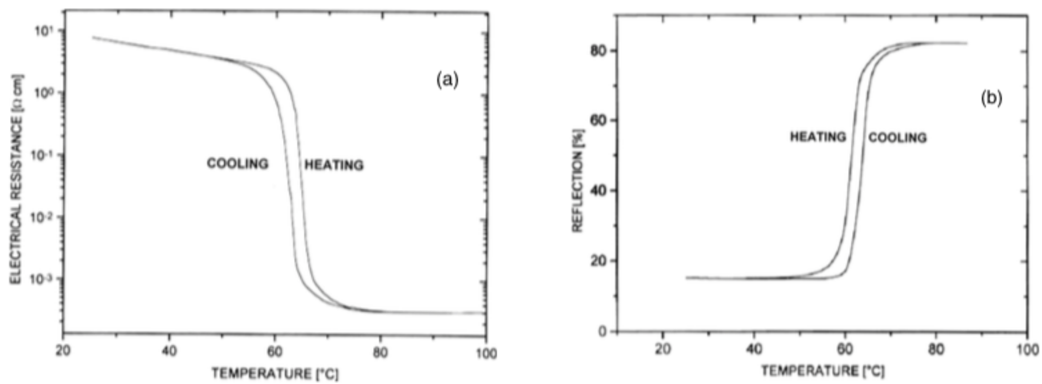

Figure 3.2: Measured hysteresis curves during the MIT of a thin VO2 film for (a) electrical resistance and (b) optical reflectivity at a wavelength of 2.0 µm [15]

The physical mechanism behind the MIT is mostly a Mott transition. However, some authors believe that MIT in VO_2 is not a purely electronic Mott-Hubbard transition, but a transition with two stages. The first step is an electronic Mott transition, that occurs when $T=T_t \sim 68^{\circ}C$, and then, this transition immediately initiates a structural change, which remembers to a Peierls phase transition [11]. Nevertheless, in some situations the structural change may not take place.

The MIT transition is triggered when a certain electron density is raised, and no matters if the value of necessary carriers is aimed by heating up the VO_2 to $T=T_t$, photo-generation, injection of carriers, or high field generation at switching. Consequently VO_2 thin films can be activated by thermal, electrical (charge injection or Joule heating), photon excitation or external pressure [9].

Some experiments injecting carriers into the VO_2 in a Si-SiO_2-VO_2 structure, through the Si substrate, have proved that this process can initiate the switching when the electron density in VO_2 exceeds a certain n_c. The value of n_c estimated from the experiments was about $n_{inj}=4.3 \times 10^{18}$ cm^{-3}, this value for the transition condition, can also be found from the Mott criterion: $(n_c)^{1/3}\alpha_H \approx 0.25$, which once operated for the values of the VO_2 gives: $n_c = (0.25/\alpha_H)^3 \approx 3 \times 10^{18}$ cm^{-3} [10], that is similar to the experimental results.

Other important effect in VO_2 is based on MOM films, when a voltage is applied to the film, the channel is heated up to the temperature of transition by the current circulating, which produces a change from the high resistivity to the low resistivity state, resulting in a S-shape voltage-current characteristic, as we can see in Figure 3.3.

Under non equilibrium conditions, with high electric fields approximately above 10^5 V/cm [14], the switching effect is proved not to be only a simple electro thermal procedure, but also a electron correlation effect [10][11], since the switching times experimented, around nanosecond scale, are considerable less that which should be if the process would be only by joule heating. Based on this, fast switching and the possibility to control the resistance state of VO2 electrically can be the principle for the utilization of VO2 in high speed electronics.

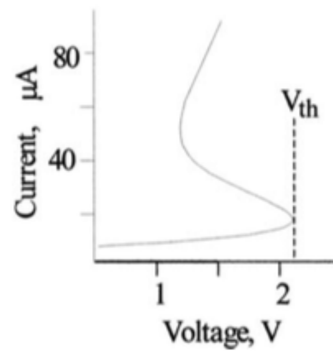

Figure 3.3: Voltage-current characteristics [10].

4 VO_2 based switches

In the last few years several switches based in the Vanadium dioxide, have been proposed. Vanadium dioxide ultrafast switching devices, where the MIT is induced by applying an electric field, could be one of the main applications, since the speed of such a switch is expected to exceed the speed of conventional field-effect transistors [18].

Also, prototypes of high speed and high density non-volatile memory structures, that use VO_2 as a switching element in the memory cell, are being explored [18].

Other transition-metal-oxide systems that have a phase transition could be used as well for novel solid state devices. Some of the materials are high-temperature superconductors, such as Y-Ba-Cu-O system, colossal magnetoresistance in manganites, such as La-Ca-Mn-O family, and also the recent observation of a high-mobility electron gas at the interfaces between $LaAlO_3$ and $SrTiO_3$ [23]. Switches based in NbO_2, which shows a thermally triggered MIT at around 1080 K, present switching times below nanoseconds [21].

It can be summarize, that the main benefits of these switches are the high-speed transitions, in the order of nanoseconds, and the size, that can be reduced up to the submicron scale.

Firstly, in this section there will be presented the most common VO_2 thin film growth techniques, and then, some theoretical and experimental electrical, optical and thermal switches, based on these VO_2 films.

4.1 Deposition techniques of VO_2

4.1.1 Chemical Vapor Deposition (CVD)

This process for depositing high quality and high performance thin films, consist on exposing a substrate to one or more volatile precursors, creating a reaction and/or decomposition on the substrate surface, that leads to the desired deposition. In

the reaction, undesirable secondary products produced are removed by a gas flow through the chamber.

CVD was the first deposition technique used for VO_2 thin films, and it is still extensively used. The process for VO_2 deposition, it is normally based on organometallic chemical vapor deposition or metal organic chemical vapor deposition. The main precursor formulations for growing VO_2 are: vanadium oxychloride ($VOCl_3$), which can be carried by N_2 or CO_2 gas into the growth chamber, pyrolysis of vanadium acetylacetonate $(C_5H_7O_2)_4V$ with mixtures of nitrogen and oxygen, and Vanadyl tri-isopropoxide ($VO(OC_3H_7)_3$) [15].

Some recent investigations, have demonstrated the deposition of VO_2 on glass via aerosol-assisted CVD, using as precursor (Vanadium (III) acetylacetonate and vanadyl (IV) acetylacetonate), dispersed in a solvent and converted in an aerosol ultrasonically [15]. In this case the precursor does not need to be volatile as in the previous cases.

4.1.2 Sol-Gel method

The Sol-Gel process is a wet-chemical technique for creating materials from a chemical solution, which contains colloidal precursors (sol). Once the sol is evolved to the formation of an inorganic network with a liquid phase (gel), is then deposited on a substrate. After, a drying process is applied to remove the liquid phase, usually alcohols, from the gel, thus forming a porous material that is finally moved to a thermal annealing step in order to favour the crystallization and enhance mechanical properties. This method allows metal doping by introducing the dopants into the sol. VO_2 is sometimes doped with tungsten or niobium to change the transition temperature [15].

In the case of VO_2 formation, generally a solution of vanadium isopropoxide $VO(OC_3H_7)_3$ diluted in an alcohol is deposited in a substrate via spin coating, and then followed by an annealing in a reducing atmosphere. Also, other vanadium oxide gels used, can be got via the acidification of aqueous solutions of $NaVO_3$, via hydrolysis of $VO(OR)_3$ or using V_2O_5 [15].

4.1.3 Sputtering

Sputtering is one of the most common physical vapor deposition processes for growing VO_2 thin films, mainly because of its film uniformity, scalability to larger substrates and the efficiency of deposition that can be reach. In this process, there are three different types of energy source that can be used for introducing the required electrons, which are: DC, RF and magnetron sputtering [15].

This method consists on a diode geometry in which the negative charged cathode, is the precursor material, generally a v-metal target (V_2O_3, V_2O_5), and the anode is the substrate [15]. A gas, normally oxygen/hydrogen mixed with argon is introduced into a pre-pumped vacuum chamber, the free electrons, provided by the energy source, are accelerated away from the cathode and when they approach the outer electrons of the neutral gas atoms, it drives the electrons off, and creates gas ions. The gas ions are fast-tracked into the cathode, striking the target and eroding the precursor material (target) via energy transfer, the neutral particles ejected, travel in a straight line until they get in contact with the substrate, creating a coating with the precursor material particles [16]. Finally, when the free electrons, produced in the eroding of the target, find the gas ions, it changes them back into neutral gas atoms, liberating photons. The formation of new neutral gas atoms, allows the starting of the process again and the eroding of more target particles.

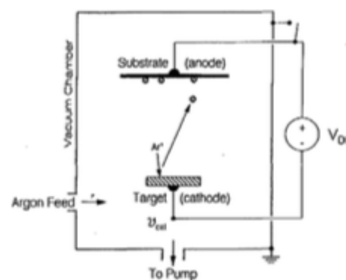

Figure 4.1: DC sputtering mechanism [15].

On one hand, the RF sputtering operates at lower voltage and lower gas pressures, producing higher deposition rates than the DC , and moreover, the RF allows the sputtering of an electrically insulated target [15]. On the other hand, the magnetron sputtering provides the highest deposition-rates sources since the magnetic field, created around the cathode, trap the free electrons close to it, increasing the rate

of gas ions created. Consequently, the quantity target material eroded and deposited on the substrate [16].

4.1.4 Pulsed Laser Deposition (PLD)

Pulsed laser deposition is a deposition technique, recently, became the most popular in the field of thin film depositions, mainly for oxide growth (VO_2). The scheme, as it is showed in Figure 4.2, consists on a laser emitter focused on the target, which is the material that will be deposited, and a substrate, which is facing the target. The target and the substrate are placed inside a vacuum chamber. The chamber can be in an ultra high vacuum or in the presence of a gas, such as oxygen.

The laser emits a high power pulsed laser beam, when the laser pulse strikes in the target, a energy conversion from electronic excitation to mechanical energy is produced, creating a group of ejected energetic species including atoms, molecules, electrons, ions and particulates, with the form of a plume. Then the mixture is deposited on the substrate, which is usually raised to a high temperature. Sometimes after the particles are deposited a process of annealed is used.

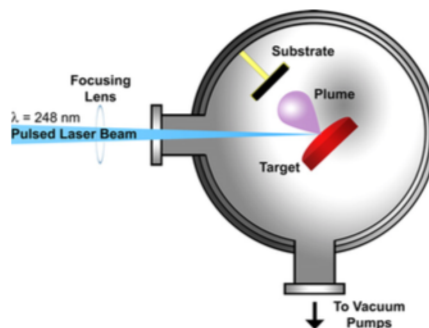

Figure 4.2: A typical experimental arrangement for PLD [15].

In the formation of VO_2, the target is usually metallic vanadium, placed into an ultrahigh vacuum chamber filled with a low pressure Ar and O_2 mixture. The substrates used are mainly silicon, glass, sapphire and quartz, which are heated up to approximately 500ºC [15].

4.2 Thermally driven VO_2 switch

The Vanadium dioxide experiments a resistance transition at a temperature of approximately 68ºC, as it was explained before. Therefore, it could be built a switch, activated by some heater, i.e. a resistance, thermally coupled to a VO_2 film.

A resistance-capacitance thermal circuit model has been proposed in ref. [12] to determine the switching time of a thermally driven MIT VO_2 nanoscale switch, using some experimental values of the thermal conductivity in the film, and the interfacial thermal resistances. The switch is a metal/VO_2/substrate structure, modelled, as showed in Figure 4.3. The thickness of the VO_2 film varies from 20 to 100 nm in the simulations.

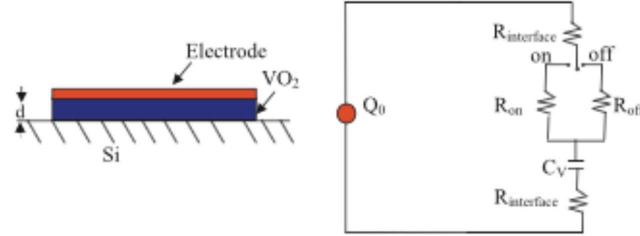

Figure 4.3: Sandwich structure of VO_2 thermal switch and the RTC circuit model [12]

In the nanoscale, the contact resistances ($R_{interface}$) at the electrode/VO_2 and VO_2/substrate interfaces are the main point in the heat conduction. The thermal capacitance of VO_2 can be defined by $C_V= \rho C\Omega$, where $\rho= 4340$ kg/m^3 is the mass density, C = 690 J/K kg is the thermal capacity and $\Omega = d \times A$ is the volume of VO_2 [12]. The thermal conductivity (κ) of VO_2 is dependent of the temperature, in the model, it is simplified by two values, one for $T<T_c$, $\kappa(T)=3.5$, and another for $T>T_c$, $\kappa(T)=6$, where $T_c=335K$ is the critical temperature that separates the "on" and "off" state. From the thermal conductivity, the thermal resistance can be found from the equation: $R_v(T)=\frac{d}{A\times\kappa(T)}$. Summarizing, the circuit can be simplified by a total thermal resistance $R_{total}= 2R_{interface}+R_v$, and the thermal capacitance of VO_2 (C_v).

After some operations, an equation for the minimum switching time for the heating process, is presented in Equation (1), assuming the initial temperature $T_0=298K$, and the temperature inside the VO_2 higher than the critical temperature (T_c).

T_∞ is the steady state temperature, which depends of the input thermal energy Q_o, via the equivalence $Q_o = d \times \kappa \times (T_\infty - T_o)$.

$$\mathbf{T(t) \geq T_c \rightarrow t_{msw} = R_{total} C_v \ln\left(\frac{T_o - T_\infty}{T_c - T_\infty}\right)} \quad \text{(1)[12]}$$

This previous equation is similar for both, cooling and heating process, the differences are the initial temperature, the steady-state temperature and the different thermal conductivity, which results in a different minimum switching time.

As we can deduce from Equation (1), the switching time depends mainly on the interfacial thermal resistance, VO_2 thickness (d), the critical temperature (T_c) and the external thermal source (Q_o). The figures presented below show the switching time dependence with these factors. It is observe that the thinner the VO_2 layer, the faster the switch. When the thermal energy (Q_o) applied is increased, the switching time decreases. Moreover, it is observed that reducing the T_c, the switching on time decreases, but it takes more time to switch off. Finally, it is also found, that when R_b is smaller than 10^{-9} m^2 K/W, the minimum switching time is similar for both process; although slightly smaller for the switch off process. For higher interfacial thermal resistance (R_b) values, the minimum switching on time of both processes increases exponentially.

Summarizing, the estimated minimum switching time from the model is of the order of ~1ns [12], which is approximated to the experimentally observed switching times, this switching time can be adjusted with the parameters presented above and generally the switching off process is faster.

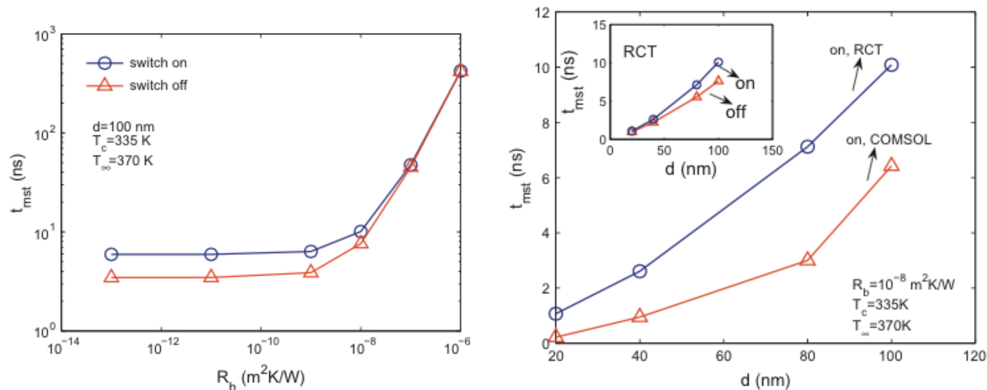

Figure 4.4: Effect of the interfacial thermal resistance (Rb) and the thickness (d) on the switching time [12].

4.3 Electrically driven VO_2 switch

In this chapter, there will be discussed the electrically activation reason of the MIT in VO_2 films, and the results acquired in refs. [17][18][19], which present different electrically triggered switches structures.

The electrically triggered phase transition (E-MIT) in VO_2 devices is been investigating nowadays for novel devices for information storage, memory resistances and neural circuits [21].

When an electrical field is applied to a VO_2 switch, there are two main possibilities that can explain the MIT, the Joule heating, due to the current that flows through the channel between the metallic contacts, and the electronic correlation effects, produced by the electronic field applied.

On one hand, the ref. [19] shows, that the Joule heating is the main reason of the dc voltage or dc current induced MIT in VO_2. For the experiments, they used a Vanadium dioxide 130 nm thick film, deposited by magnetron sputtering on a r-cut sapphire substrate, with gold electrodes over the film, creating channels of 10 and 20 μm. They measured the temperature increase in the VO_2, placing a fluorescent particle of ~1μm inside the channel, and applying a dc voltage through a resistance in series with the contacts, at different initial temperatures T_{set}.

The experimental measurements of the channel temperature, incrementing the voltage, fixed the results of the model, assuming an ohmic Joule heating. The results are depicted in Figure 4.5(a,c). Moreover, the resistance measured in the channel, while heating the VO_2 film with a Peltier heater and while increasing the dc voltage, were superposed, and both curves were very close, they are labeled as Equilibrium R(T) and Non-equilibrium R(T) respectively, in Figure 4.5(b,d). From these results, it is proved that the Joule heating plays a key role in the dc voltage or dc current induced MIT in micro sized VO_2 channels.

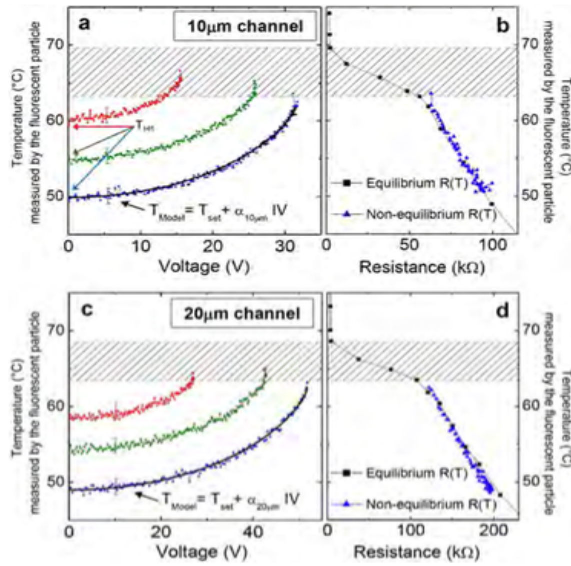

Figure 4.5: Temperature of flourescent particle vs dc voltage [a,c] and local temperature vs resistance.

On the other hand, the references [17][18] discussed that the electric field is the main reason in the MIT in ultrafast VO_2 switches, since the Joule heating would lead longer switching times.

Firstly, in the ref. [17], it is presented a MOIM (Metal oxide insulator metal) structure, where the oxide is the VO_2 film and the insulator is a thin SiO_2 layer. This structure is believe to be a very desirable option in ultrafast electronic devices, since the insulator layer reduce significantly the current between the two metal layers, in the metallic and insulator state of VO_2, reducing the Joule heating effect and consequently the “on” to “off” switching time.

The perpendicular structure was prepared by depositing firstly a 200 nm Pt layer onto Si/SiO_2. Secondly, the SiO_2 buffer (180 nm) was grown in the Si/Pt substrate with a chemical vapor deposition, and after, it was created, using RF magnetron sputtering, the VO_2 thin film with 200nm thickness. Finally, an Au patch of 100 μm x 100 μm was placed over the VO_2, the structure is shown in the inset of Figure 4.6. The temperature-resistance curve was measured, and it showed an abrupt changed around Tc=66ºC with a resistance increment of approximately 2 x 10^2 and a hysteresis window of AT ≈ 10ºC, which confirms a clear MIT in the structure.

For investigating the E-MIT of VO_2 structure, it was measured the I-V characteristics, measuring the current and incrementing the applied source voltage, between the metallic electrodes, under different temperatures. The results are shown in Figure 4.6. The maximum current of the power source was limited to 100mA to protect the switch when the metallic state is reached.

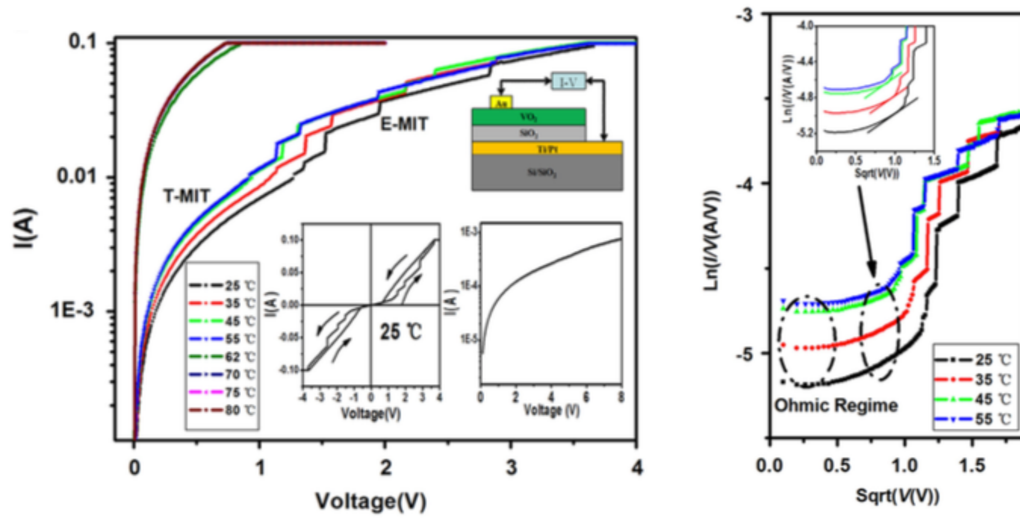

Figure 4.6: (a) (I-V) curves measured for different initial temperatures (T_o); inset: schematic of the MOIM structure, hysteresis at T_o=25°C and leakage current in the SiO_2 buffer. (b) Poole-Frenkel analysis.[17]

When the threshold voltage V_T≈1.6V is overwhelmed, which is equivalent to an electric field of ~$4.2x10^6$V/m, it is observed a notable series of jumps in the current, produced by the decreasing of the resistance, which is the MIT. The MIT is even more clear, with the Poole-Frenkel analysis, showed the right graphic of Figure 4.6, where the difference between the ohmic and metallic region are easily notice. These subsequent small MIT steps are may due to the sequential switching of different VO_2 grains, or local domains [17], which are induced by the ionization impact.

The voltage applied to the electrodes produce a carrier injection via the Pt layer into the SiO_2 insulator, and the carriers are kept. The accumulated carriers generate a large charge, that creates an electric field, and acts in the electron subsystem of VO_2, producing the phase transition [17]. However, a leakage current exists through the SiO_2 layer, so Joule heating causing by defective oxide, probably also contributes to the VO2 film for MIT.

Secondly, in the ref. [18] it is reported the results of the experiments made in a nanoscale VO_2 device. The switch consists on a VO_2 ~100nm thickness film, deposited by dc sputtering over a n-Si substrate, and several Au nanodots of 200nm diameter, deposited on the top of the VO_2 film by electro beam lithography. The structure shows a MIT near 73ºC, with a resistance increment of approximately three orders of magnitude.

The electrical measurements were done using a tip AFM between the Au contacts, which are the top contact, and the Si substrate as the bottom contact. The results were done at room temperature. It can be noticed from the results, showed in Figure 4.7, that an abrupt jump in the current and an increment in the conductance are produced when the critical voltage (~1.8V) is reached, clearly showing the phase transition in the VO_2 film. The electrical field at the MIT is approximately E_c=1.8V/d=18x10^{6}V/m, which is a value close to the example presented above.

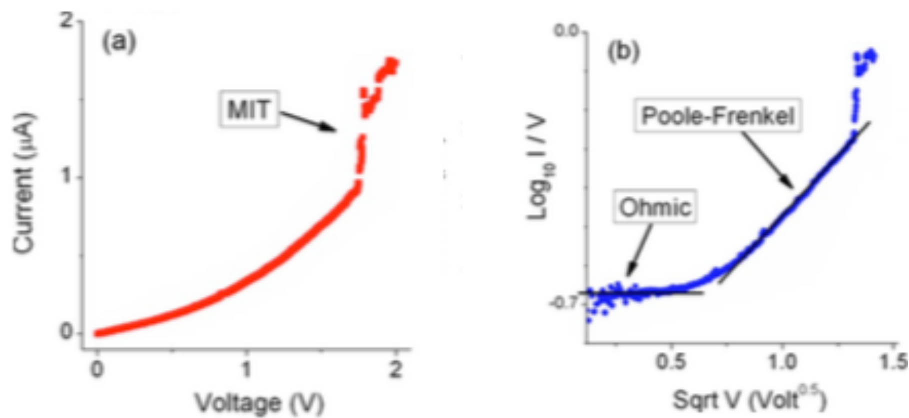

Figure 4.7: Electron transport measurements in nanoscale VO2 at room temperature using conducting tip AFM. I-V curve from a dot (left), and Poole Frenkel analysis (right). [18]

Finally, it could be considered, that Joule heating due to the current through the junction between the electrodes, could be the possible mechanism of the MIT in the nanoscale devices presented; however, it is only proved in microsize devices with dc current/voltage triggering. The Joule heating power, at the onset of the MIT in the nanojunctions, is comparable to the Joule power of the microdevices used in ref. [20]. It can be deduced from the electrothermal simulations, presented in reference [20], for different microsize switches, that the Joule heating produced by the power required to induce the MIT is insufficient to heat the VO_2 film up to the critical temperature

(68ºC), meaning that the transition is a field effect. Also, it was found a weak reduction in the temperature rise at the transition point for narrower channels, produced by a decrease in the channel current, which is proportional to a channel width. A similar decrease is observed in the reduction of the channel length, since the applied power necessary to raise the critical field is reduced. Moreover, since the heat dissipation speed is higher in smaller structures, the heating in the nanojunction should be lower [20].

For measurements done with a voltage source, the temperature rise in the channel just beyond the transition is notably larger than in the semiconductor state, leading to a rapidly thermal phase transition after the field-induced transition. Then, the electronic phase transition precedes the structural phase transition. In most of the simulations, the Joule heating appears insufficient to induce the MIT, however, in the metallic state the heating is enough to maintain the metallic state even if the voltage applied is reduced significantly. It is observed in the large hysteresis between the power required to switch "on" and "off" the VO_2 channel, depicted in the I-V characteristics [20].

The origin of the electric field assisted MIT is an area of ongoing research. It has been argued that the electric field in VO2 causes the doping of the valence band with holes to a critical hole density, thus triggering the hole-driven MIT. The fact that the injection of hole carriers into the material can trigger the MIT, was also established from the optical pump-probe experiments where the carriers were excited by laser pulses [18].

5 Thermal electronic logic circuit TELC

Since some decades ago, in the electronics and information technology field, the silicon technology has been the huge dominant. However, nowadays some other technologies are being investigated to developed nanoscale devices with a simpler scheme, and to face the impossibility of the silicon technology for scaling down more due to the tunnel effect.

The new thermal electronic logic (TELC) has been proposed in reference [22], which is based on the VO_2 switches, instead of the current CMOS technology. The technology consists in mixing heating resistors with single SMT-material bulks. The heating resistors are used to set the temperature of the bulks, inducing on it a change from the insulating “off” to metallic “on” state.

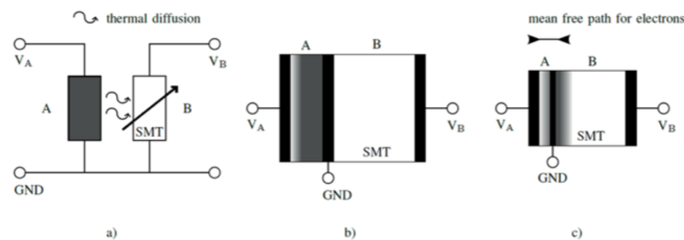

Figure 5.1: The phonsistor concept. [22]

The Figure 5.1 shows the simplest phonsistor device, which consists on a heating resistor (A) and a SMT resistor (B) thermally coupled. In b) it can be observed a phonsistor formed by a resistor between the two electrodes on the left, which is heated by the Joule-effect, and consequently heats the MIT material between the middle and right electrodes, which can switch on the material. Finally, in c) it is pointed the effect of scaling down the phonsistor, where the heating resistor thickness is lower than the mean free path for electrons, and it leads the hot electrons to be injected by ballistic transport directly into the SMT material, and then, they thermalize there.

The thermal electronic gates are formed of one or more input, which are normally heating resistors voltage/current driven (or SMT resistors), thermally coupled to one or more SMT resistors, which are the outputs, as it is observed in

Figure 5.2. The combination of the heating resistors and SMT resistors can produce different type of gates. If the thermal coupling is strong it could be possible to switch on the SMT resistor of the output, only with one input activated, otherwise if the coupling is weak, it may be necessary to active more than one input to switch the output, forming OR and AND gates respectively. Therefore, adjusting the thermal coupling between the inputs and the outputs, via geometrical distance and/or using different isolating materials between them, it could be easily created OR/AND logic gates and combinations of them.

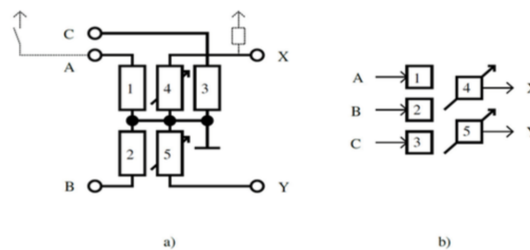

Figure 5.2: Conventional a) and simplified b) scheme of a general thermal-electronic logic gate. [22]

The TELC consists on many phonsistors, which can be thermally coupled to each other or connected through metallic wires to longer distances via electric signals, if the output SMT resistor of the phonsistor is connected to a pull up resistor.

The TELC is supposed to be compatible with silicon integrated circuits. The TELC can be created by lateral arrangement or vertical arrangement, which seems more promising, since it could be compatible with standard silicon CMOS VLSI circuits and it could be more dense. The thermal time constants in this nanoscale integration can be comparable to the electric constants, approximately 10^{-10} seconds.

Since the TELC scheme is simpler than the conventional VLSI circuit, it contains less interfaces, and allows an easier and more effective scaling down, limiting the linear size due to the tunnel effect to 10nm in phonsistor devices, instead of 50nm, as in complex logic gates (CMOS).

This technology has been proved on a complex gate, realized on a VO_2 thin layer deposited onto an isolator substrate, with metallic contacts forming rings, Figure 2.1 b). The outer rings are connected together forming the ground, and the electrical

controller of each gate is insulated. The internal contacts are the input and outputs, and all the gates are thermally coupled.

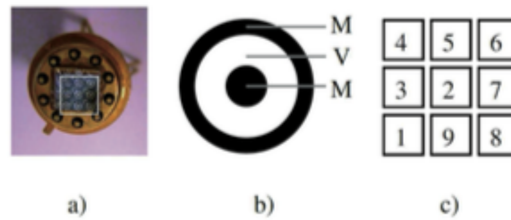

Figure 5.3: a) Photograph of the experimental thermal-electronic integrated circuit. b) Structure of a single device. c) Numbering of the coupled devices [22]

For the test, the gates were connected to current limited power supplies, through pull up resistors. It was tested the NOR operation and the AND operation, with the gate No. 3 as output and gates No. 5 and 7 as input. In the NOR operation any of the input gates could switch on itself and the output. However, with lower supply voltages in the inputs or shorter time scale, it was needed unless two inputs to generate enough Joule heat to switch on the output gate, thus, simulating a NAND gate. The phonsistor is switched off only by decreasing the supply voltage of the output. The device switching time can be estimated about 10 ms for this relative large size TELC device.

6 VO_2 Laboratory Measurements

For the experiments of the Thermal Logic Circuit, it has been used a layer with an VO_2 thin-film of 100nm thickness and Platinum contacts of approximately 50nm width.

The VO_2 layer was developed using the Pulsed Laser Deposition technique, where exactly 20000 laser pulses were stroke in a vanadium target during a period of 33 minutes. The target and the substrate were placed into a vacuum chamber, filled with O_2 gas at $2x10^{-3}$ mbar. The substrate used was SiO_2-Si and was kept at 600ºC during the process. This VO_2 layer was fabricated in Finland.

The desired geometries of the Pt contacts, which are shown in Figure 6.1, were made with a lift-off technology. For the deposition of the platinum in the wafer, it was used RF reactive cathode sputtering, the sputtering power used was 100W with a voltage of approximately 1kV and the current through the magnet was 5A. Firstly the chamber was pre-vacuumed up to ~2×10-4 Torr and then, Argon was introduced into the chamber until a pressure of 10×10-4 Torr was reached. The plate was covered with a 5 min pre-sputtering, and then 5 min of sputtering. The vacuum pressure of the chamber at the end of the process was ~1×10-4 Torr. The deposition process of the platinum contacts has been made at the BME University.

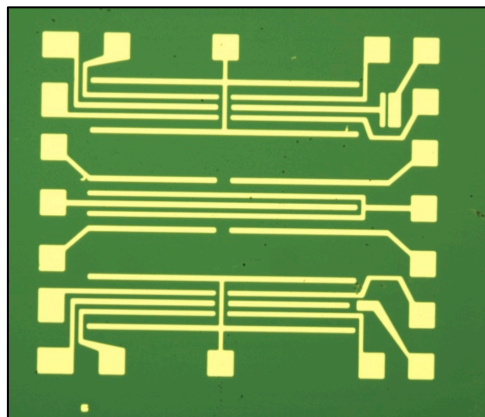

Figure 6.1: The three different geometries of the platinum contacts over the VO_2 film.

6.1 SMT resistance

Firstly, it has been measured the characteristics of the SMT resistance formed between two upper platinum contacts on the left, in the below geometry of Figure 6.1, the scheme is represented in the Figure 6.2.

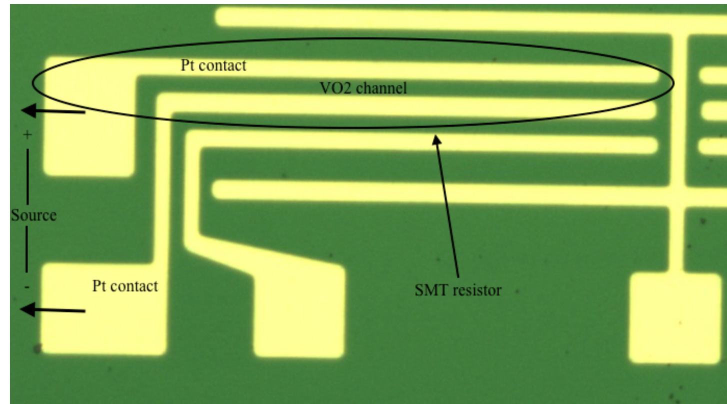

Figure 6.2: Scheme of the SMT resistor based on VO_2 channel.

The graphic of the temperature-resistance, showed in Figure 6.3, has been achieved varying the temperature of a hot plate situated below the VO_2 layer and with a thermal coupling paste between them, to facilitate the heating. The temperature of the hot plate is controlled by heating and cooling the water that flows inside the plate. The resistance was measured by placing two probes over the contacts. The probes were connected to a Kethley 2450 source meter and it was applied 10 µA to the contacts for measuring the resistance.

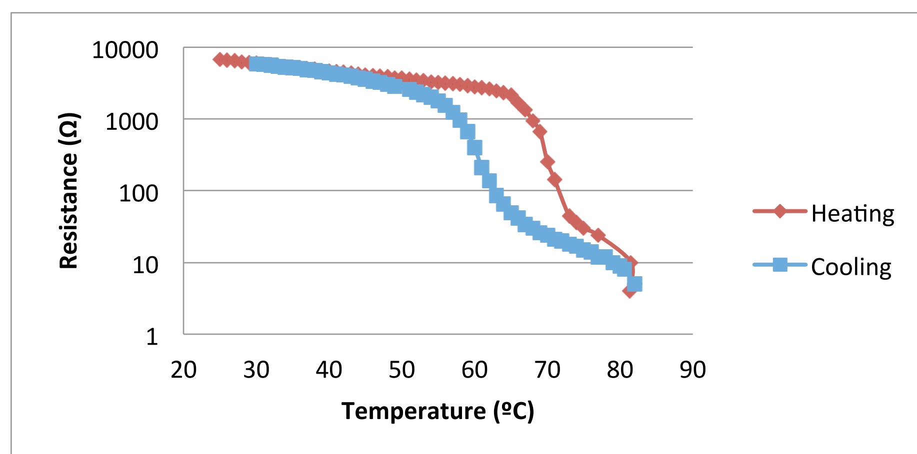

Figure 6.3: Resistance – temperature graphic between the two platinum contacts.

The phase transition was produced at approximately 70ºC, and the resistance changed from 6,5kΩ at the room temperature to 5Ω in the metallic state, it means a change of 3 orders of magnitude, as it could be predicted from the references presented in the previous chapters. Also, there is a hysteresis of ~10ºC, which is the usual for thin films. In the metallic state, the colour of the VO_2 layer changes from green to dark purple.

Then, the voltage-current characteristic has been measured in the same contacts, the source meter was connected to the contacts, and it was varied the current while the voltage was monitored. The tests were done for different temperatures of the hot plate; these plots are shown in Figure 6.4, 6.4 and 6.5.

In a first approximation, it can be explained the phase switch between the platinum contacts, as a Joule-heating effect, produced by the current through the VO_2 channel, since as it can be deduced from Chapter 4.3, the electric field effects appeared for nanoscale ultra-fast switches, but for micro size channels voltage/current driven as ref. [19] expounds, the Joule heating is the reason of the switch.

It can be observed in the figures below, that the VO_2 resistor has a tyristor like characteristic. When the current increases, the voltage increase as well with the ratio of the resistance existing between the contacts. Once the critical power is reached, which produces the enough Joule heat to achieve the transition temperature (68ºC), the VO_2 channel switches to the metallic state. When the metallic state is raised the resistance drops, and consequently the voltage decreases. The "on" state is kept until the current decrease so much, that the metallic state cannot be maintained and the channel recovers the semiconductor state. The resistance during the "off" state decreases slightly with the current increment, due to the temperature increment produced by the Joule heating.

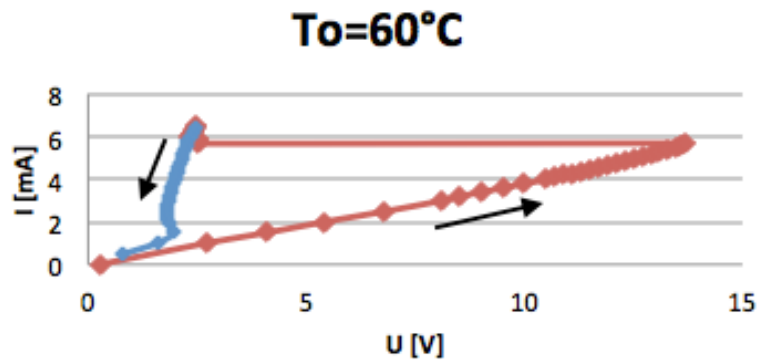

Figure 6.4: Current - voltage graphic of the SMT resistor at 60ºC

At the 60ºC temperature measurement, the resistance varies from 2800 Ω, with 10μA, in the off state, up to 380 Ω in the metallic state at 6,5mA. The transition was produced at 5,7 mA, the voltage dropped from 13,7V to 2,5V, this means that the Joule heat power required was 78mW.

The experiments with the layer at 55ºC, showed, that for the phase transition it was required approximately 6mA, which produced a 91mW Joule heat power. The resistance changed from 2870Ω, with 10μA, to ~400 Ω in the metallic state.

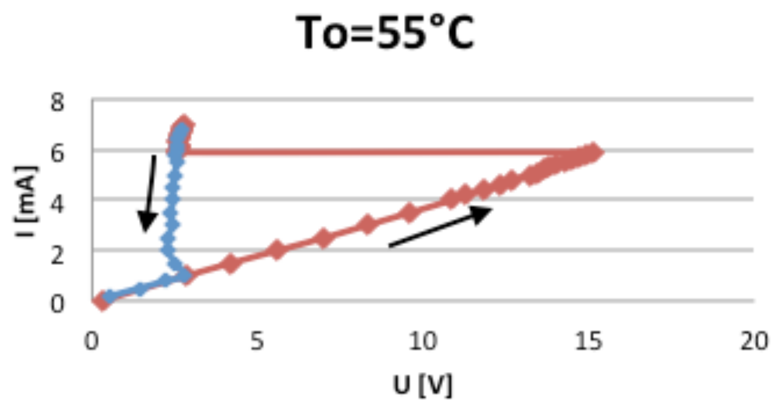

Figure 6.5: Current - voltage graphic of the SMT resistor at 55ºC

Then at the temperature of 45ºC it was measured the I-V characteristic, at the first measurement, which is showed in Figure 6.6, the phase transition was produced at 8,1 mA and 25,5V, which means a power of 207,4 mW, but on the posterior measurements the transition was achieved at around 7mA (160 mW). The resistance varies from 3980Ω, at 10μA, to 425Ω at 9mA, which corresponds to semiconductor and metallic state, respectively.

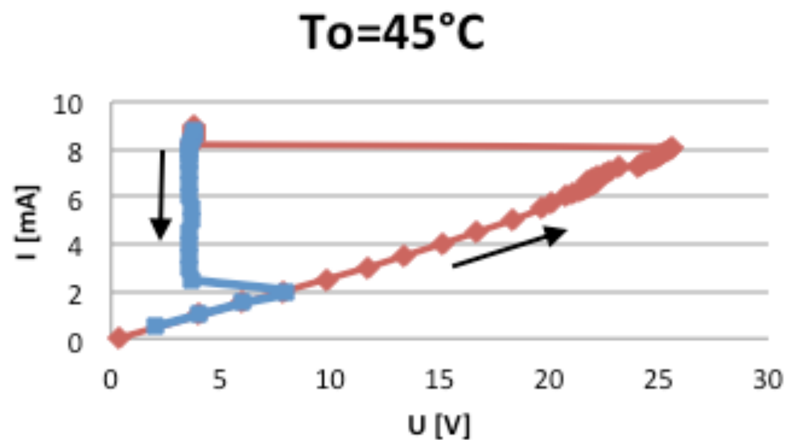

Figure 6.6: Current - voltage graphic of the SMT resistor at 45ºC

It can be summarize from the figures above, that while the temperature of the layer decrease, the power required to switch the resistor increase, which is due to the bigger temperature increment needed to raise the transition temperature. From the Joule heating equation $\Delta T = P \; x \; R_{th}$, it can be established an average thermal resistance for the VO_2 resistor, establishing the transition temperature at 70ºC, as observed in Figure 6.3, and the power required to achieve the transition as P=V x I, where V and I is the voltage and current in the moment of the transition, observed in the characteristics on Figure 6.4, 6.4 and 6.5. In the Table 1, it is presented the experimental thermal resistance for each temperature.

The average thermal resistance is 140 K/W, which is a first approximation to find the Joule heat power needed to switch on the channel for each working temperature, however this is not a exact approximation due to the leakage current flow variations, since the current path is not completely defined.

The resistance change between the on and off state is less than one order of magnitude, which is quite lower than the measured at the resistance temperature graphic, which was 3 orders. These increment on the on state resistance is produced because only a narrow metallic state channel is formed in the VO_2 film between the contacts, instead of switching on the whole VO_2 film channel, as it was produced when the whole layer was heated. The reason for this narrow channel is that the current is not equally distributed through the whole metallic pad due to the current leakage. Therefore, it produces that the current which flows in the proximity of the pad connexion to the needles, is higher than in the further parts, leading to heat more

the closest portions of the VO_2 film than the others, and consequently the phase transition is done only in the zone where the critical temperature is reached first.

Table 1: Thermal resistance experimentally found from Joule equation

T_o	ΔT	I_{th} (transition current)	P_{th} (transition power)	R_{th} (thermal resistance)
60ºC	10ºC	5,7 mA	78,1 mW	130 K/W
55ºC	15ºC	6 mA	91,2 mW	160 K/W
45ºC (first measurement)	25ºC	8,1 mA	207,4 mW	120 K/W
45ºC (posterior measurements)	25ºC	7 mA	164 mW	150 K/W

It was reported some problems when it was tried to switch on at 35ºC. For switching on the SMT resistor the current was increased by 1mA steps, but at 5mA (165mW) it appeared a big increased in the voltage, since the electrical resistance started to increase, it changed from 4,9 kΩ to 6,6 kΩ. A crack in the VO_2 channel and the platinum contact was observed with the microscope, the image of the break is showed in Figure 6.7.

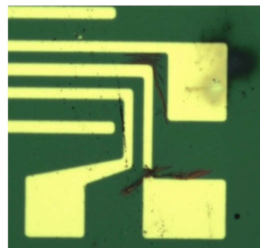

Figure 6.7: Crack in the VO_2 channel and Pt contact at 35ºC measurements.

After the crack, the measuring probes were changed to another part of the layer over the same geometry, to try again to switch on the channel at 35ºC. This second time, the current was increased slowly, with 0,1 mA steps. The current-voltage characteristic found is shown in Figure 6.8.

At 10,5mA and 36,1 V, which produced 379 mW, the resistance changed from 3438Ω to 1367Ω which could be associated to the SMT transition, although the change is not large. After increasing current, the metallic state continued, but when the current decreased to 10,5 mA again, the resistance increased to 3809 Ω, since the channel switched off. The thermal resistance observed from this measurement is approximately 100 K/W, which is not too far from the one found at the other tests.

It can be noticed, that in the last experiment at 35ºC the channel switched off at the same current of the switch on, which is very fast compared with the measurements done at the other temperatures, where the hysteresis between the current needed for change from the semiconductor to metallic state and viceversa, was quite large. The high temperature increment needed to heat for switching on the channel cannot be maintained when the current starts to decrease. The reason may be, that the temperature difference between the whole plate and the channel is large, leading to a high heat flow, which produces a faster cooling of the VO_2 channel.

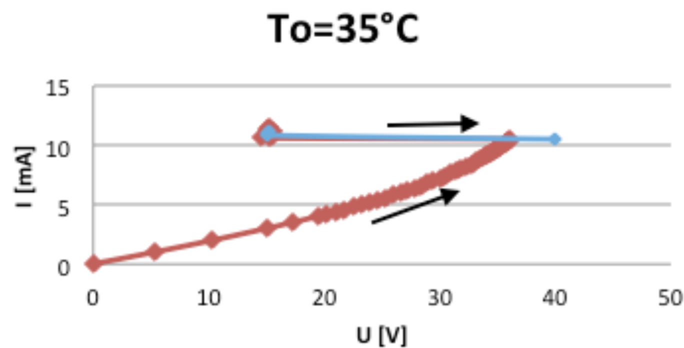

Figure 6.8: Current - voltage graphic of the SMT resistor at 35ºC

Finally, on the figure below it is displayed the black stain produced in the channel after switching on and off the resistor several times, in the 45ºC experiment.

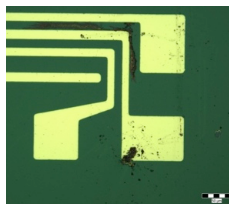

Figure 6.9: Crack in the VO_2 channel at 45ºC measurements.

6.2 NOR thermal gate experiment

Based on the theory of the TELC (thermal logic circuits) presented in chapter 5, it is known that several SMT resistances thermally coupled can realize the function of different gates. In the layer reviewed for the study, the platinum contacts over the VO_2 layer forming different geometries, showed in Figure 6.1, can function as the thermal gates.

It has been studied the logic function and properties of the scheme showed in Figure 6.10, which consists on four SMT resistors, which are thermally coupled to other SMT resistor in the middle, following the scheme of the phonsistors depicted in Figure 5.1.

The NOR gate function is tested, using four input SMT resistors current driven, which are formed between the platinum contacts, named as Input 1, 2, 3 and 4, a platinum contact in the middle labelled as Ground, and an output SMT resistance between output and ground contacts. The input resistors activate the output SMT resistor by Joule heating. The output contact of the output resistance, is connected to a voltage source through a 1kΩ resistance, limiting the current through the SMT resistance, and creating the NOR function, since when an input turns on it leads the output resistance to switch to the metallic state, consequently Vout is connected via the small resistance value, at the metallic state, to the ground. The 1kΩ pull-up resistance absorbs the most of the Vdd voltage drop.

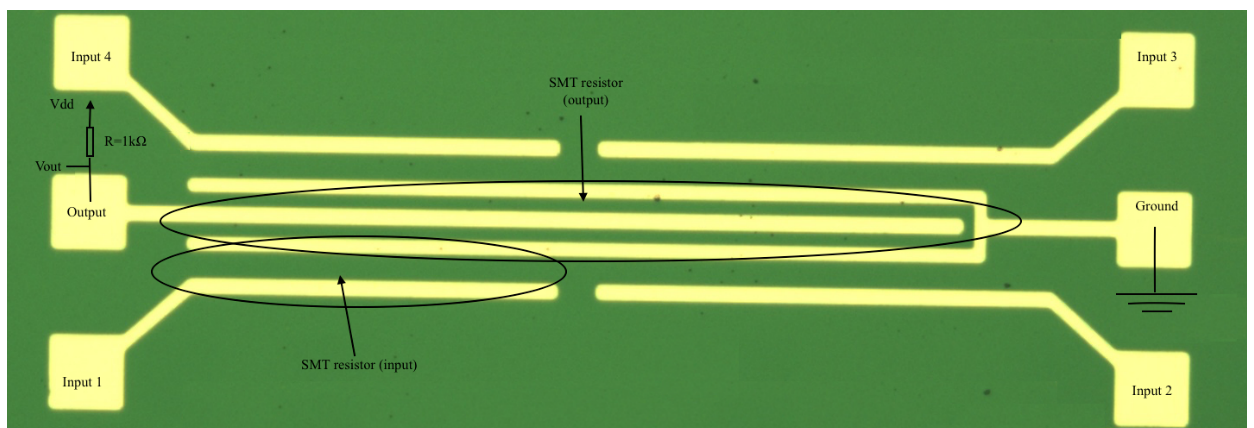

Figure 6.10: Modified image, obtained from the microscope, of the NOR thermal gate structure

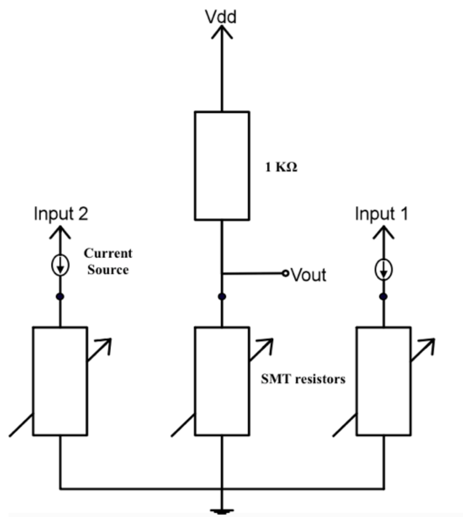

Figure 6.11: Electrical scheme of the thermal NOR gate

Firstly, it has been measured the resistance-temperature characteristic of the SMT output resistance, which is showed in Figure 6.12, following the method described in section 6.1 used to obtain the Figure 6.3. As it was expected, at a temperature of approximately 70ºC the VO_2 channel switched from the semiconductor to metallic state, the resistance decrease from 2,3kΩ at 30ºC to 85Ω at 80ºC. At the cooling process as noted before, the switch from metallic to semiconductor state is not produced at the same temperature, this hysteresis is observed to be more or less 7 ºC.

In this scheme it is noticed that the resistance between the platinum contacts at the semiconductor state is lower than the resistance at the SMT resistance studied in section 6.1. The reason must be the better geometry, which reduces the quantity of current leaking through other parts of the VO_2 film, instead of following the path between the high potential and the ground. Since the current path is better defined, the resistance is less.

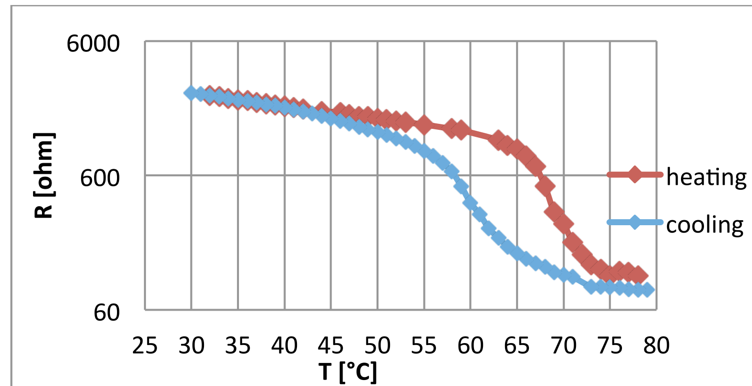

Figure 6.12: Resistance-Temperature graphic of the SMT resistor between the Output and Ground

Then, the hot plate placed below the VO_2 was heated up to 50ºC, after, increasing the current applied and monitoring the voltage, it has been found the current-voltage characteristic of the SMT output resistor, and it is depicted in Figure 6.13. This test was done before connecting the output to the supply voltage "Vdd".

When the power applied to the output resistance reached 387,5 mW the channel switched from the semiconductor to metallic state, it is noticed a drop on the resistance from 1,5 kΩ to 420 Ω at the semiconductor and metallic state respectively. The resistance at the metallic state is higher than the observed in Figure 6.12, since the metallic state is just produce in a narrow channel at the VO_2. This affirmation is derived from the resistance equation: $R = \rho \times \frac{L}{S}$, where S is the section/area, L the length and ρ the resistivity constant of the conductor. Therefore, the higher the material surface the less the resistance.

The metallic state is conserved until the power supplied descends below approx. 8 mW, where the resistance jumps from 800Ω to 1550Ω. While the power supplied is decreasing, the electrical resistance rises slightly due to the temperature reduce, (as observed in the resistance-temperature graphic), until the critical temperature is reached and it switches to the semiconductor state. This is clearly seen in the graphic below, where at 3mA and 2,7V, the slope of the descending line (resistance), turns back to the previous slope at the semiconductor state, when the current was increasing.

Despite the low power applied, the metallic state is maintained until quite below the power value needed to switch on the channel. The reason is that once the metallic channel is created in the VO_2 film, all the current flows through this narrow channel, increasing the collisions between the electrons and consequently producing a higher amount of heat, which turns into a higher thermal resistance in the metallic phase, (as it will be see in Table 2,3). Then the temperature at this channel is maintained over the switch "off" critical temperature, approximately 63ºC, with a low Joule heat power.

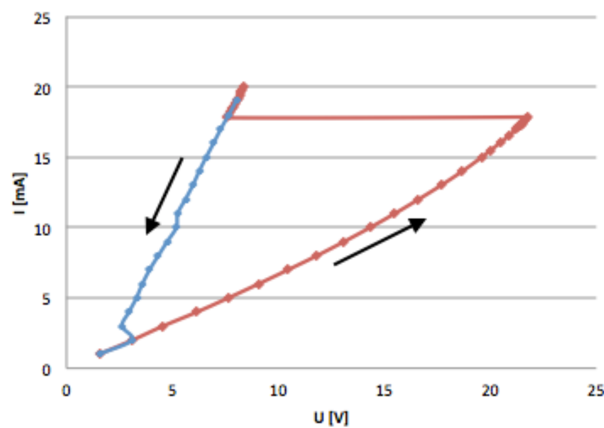

Figure 6.13: Current - voltage graphic of the SMT resistor between the Output and Ground contacts at 50ºC

Then, it has been measured the current voltage characteristics of the SMT resistances created between the Input 1, 2 and the ground, at 50ºC, before connecting Vdd. The plots are showed in Figure 6.14, 6.14. The average power measured, required to switch on the resistances after several test, was 210mW and 230mW for the Input 1 and 2 resistances, correspondingly. Otherwise, the power measured in the transition from metallic to semiconductor state was approximately 10mW for both cases.

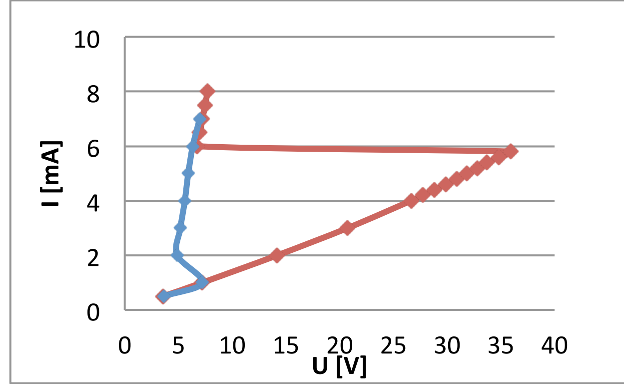

Figure 6.14: I-V characteristic of SMT resistance between Input 1 and ground contacts.

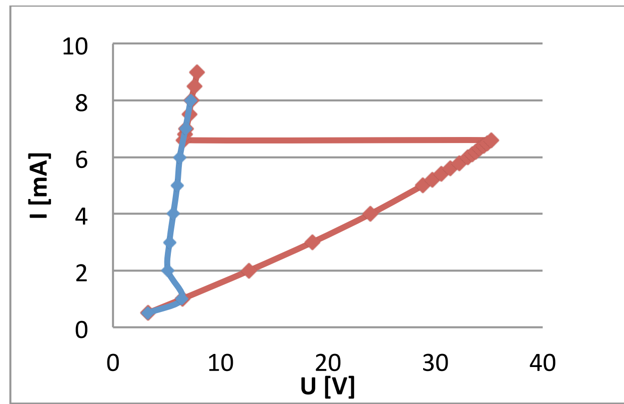

Figure 6.15: I-V characteristic of SMT resistance between Input 2 and ground contacts.

The thermal resistance can be found experimentally using the Joule heating relation: $\Delta T = P\ x\ R_{th}$, as it was done in the previous section, or through the equation of the thermal resistance in an specific material, this has two variations depending if the surface crossed by the current (heat source), is big or small compared to the heat sink, in this case the silicon substrate. In the second case it has to take in account the spreading resistance approximation. The equations of the thermal resistance are the Thermal resistance in a specific material (2) and the Spreading thermal resistance (3).

$$\boldsymbol{R}_{\mathbf{th}} = \boldsymbol{\rho}_{\mathbf{th}} \times \frac{\boldsymbol{t}}{\boldsymbol{A}} \quad \textbf{(2)}$$

$$\boldsymbol{R}_{\mathbf{th}} = \boldsymbol{\rho}_{\mathbf{th}} \times \int \frac{\boldsymbol{dr}}{\boldsymbol{2\pi r^2}} = \frac{\boldsymbol{\rho}_{\mathbf{th}}}{\boldsymbol{2\pi}} \times \left[\left(-\frac{\mathbf{1}}{\boldsymbol{r}_{\mathbf{in}}}\right) - \left(-\frac{\mathbf{1}}{\boldsymbol{r}_{\mathbf{fin}}}\right)\right] \quad \textbf{(3)}$$

Where ρ_{th} is the resistivity of the material, “t” thickness, “A” area/surface and r_{in}, r_{fin} are the radio of the narrow metallic channel created on the VO_2 over the silicon surface, and the radio at the end of the silicon, which can be approximated to ∞, respectively.

From the previous equations, it is calculated the values of the experimental and theoretical thermal resistance of the output SMT resistance, and the input resistances, this values are presented in Table 2 and 3.

Table 2: Thermal resistance estimated from experimental values

	ΔT	**Current**	**Power**	**R_{th}**
Output resistance "Semiconductor state"	20 ºC	18 mA	387 mW	52 K/W
Output resistance "Metallic state"	13 ºC	3 mA	8 mW	1625 K/W
Input 1 resistance "Semiconductor state"	20 ºC	5,7 mA	210 mW	95 K/W
Input 1 resistance "Metallic state"	13 ºC	2 mA	9,8 mW	1325 K/W
Input 2 resistance "Semiconductor state"	20 ºC	6,5 mA	230 mW	87 K/W
Input 2 resistance "Metallic state"	13 ºC	2 mA	10,2 mW	1275 K/W

For the theoretical equations, it can be supposed that all the heat is produced in the silicon substrate layer, which thickness is 300μm, since the thickness of the VO_2 film and the platinum contacts is of the order of nm, than, the value of the thermal resistance of this films is negligible compared to the thermal resistance of the silicon substrate. The value of the thermal resistance used for the silicon layer is 0,77 cmºC/W, extracted from Ioffe Institute web page.

Table 3: Thermal resistance estimated from Eq. (2) and Eq. (3)

	Width	**Length**	**Area /Radius**	**R_{th} (thermal resistance)**
Output resistance "Semiconductor state"	60 μm	800 μm	0,0464 mm^2	50 K/W

Output resistance /Input 1,2 "Metallic state"	10 µm (metallic channel width at the beginning)		5 µm (radius of circle equivalent to rectangular channel)	245 K/W
Input 1 resistance "Semiconductor state"	45 µm	380 µm	0,017 mm^2	135 K/W
Input 2 resistance "Semiconductor state"	45 µm	400 µm	0,018 mm^2	128 K/W

The values of the thermal resistance experimentally and theoretically, showed in the tables above, are in concordance, proving that the Joule heating effect, which occurs in the device is the reason for phase transition from metallic to semiconductor and from semiconductor to metallic state. The Joule heating increases the temperature in the VO_2 film and then produce the phase transition. The small differences produced in the thermal resistance in the semiconductor state are may be due to the current leakages, since not the totally of the current flows to the surface between the input and the ground surface, it is been supposed at the theoretical results.

Nevertheless, it is observed a big difference at the thermal resistance values at the metallic state, which can be explained with the following remarks.

A decreasing in the current is tested to produce a slight increasing in the electrical resistance, due to the cooling of the channel and the decrease of the channel thickness. It has been observed, that the higher the power the larger the width of the channel, and viceversa. This channel width decrease could be the reason for explaining the large thermal resistance observed experimentally in the switch from metallic to semiconductor state, and consequently the high hysteresis between the power necessary to switch on and off.

When metallic state is achieved the thermal resistance increase, assuming a channel width of 10 µm (r_{in}=0,5 µm) just after the switch, the thermal resistance, using the eq. 3, would be 245 K/W which is not enough to maintain the temperature necessary for the metallic state with such a low power, however, since the width of the channel decreases when the current decreases, it would produce a higher thermal resistance which could keep the metallic channel longer. For example, if the thickness

of the channel is 0,2 μm (r_{in}=0,1 μm), the thermal resistance from the eq.3 is 1225K/W which is the experimental value.

Once it has been studied separately the characteristics of the Input and Output SMT resistances, used for the thermal gate, the 1kΩ resistance and the power supply was connected to the output SMT resistance, as presented in Figure 6.10.

The current-voltage characteristics of the input resistances have been studied, observing the variations with the supply voltage connected to the output resistance. It was tested as well, the effect of the inputs on the output.

Firstly, it has been measured the Input 1 graphics. The Figure 6.15, was obtained setting Vdd=16V, (Vout=9V), with this voltage the output was "off", (before applying any current to the inputs). Then, the same graphic was found (Figure 6.16), when the output resistance was in the metallic state, for this, the power supply was increased up to Vdd=24V, at this value the resistance switched on, and Vout changed from 12V to 7,4V.

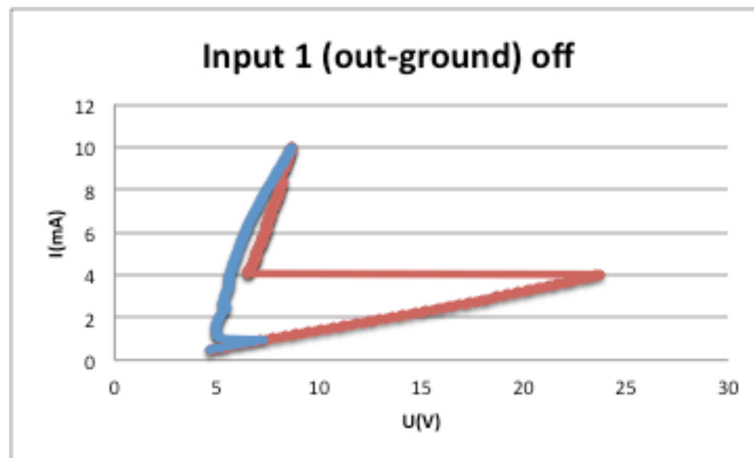

Figure 6.16: I-V characteristic between Input 1 and Ground contacts, when the SMT output resistor off state

It is perceived a variation between the power required to switch on the Input 1 SMT resistor, when the output resistor is active or not. As it is showed in Figure 6.16, Figure 6.17, when the output resistor is in the metallic state the phase transition is produced at 75,7 mW, which is a bit lower than in the semiconductor state, 95,43 mW. In both cases the power is also considerably lower than in the case without connecting the output resistor to the power supply, where the power required was 210 mW.

The reason for the decreasing in the necessary power to switch on the Input resistor, when the power supply is applied to the output resistor, is that the current flowing through the output resistor produces a Joule heat (proportional to the power applied), which propagates to the input resistor, since all the SMT resistors are thermally coupled via the silicon substrate. This principle perceived, is the same used to switch on the NOR gate activating the inputs.

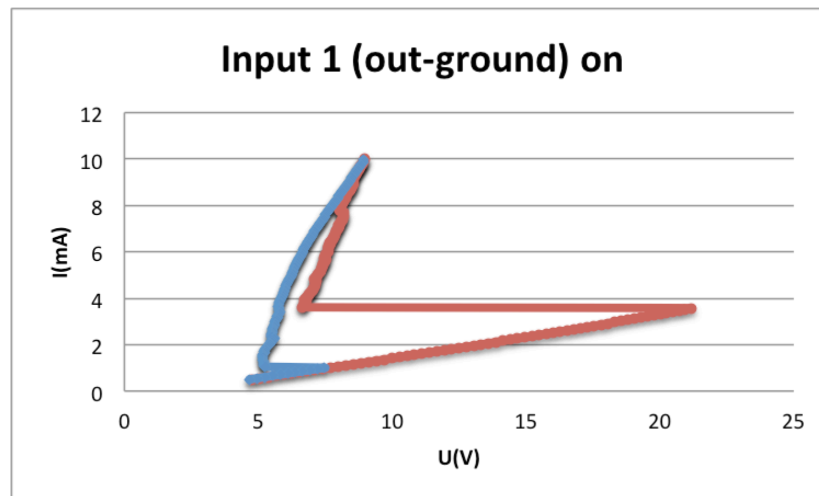

Figure 6.17: I-V characteristic between Input 1 and Ground contacts, when the SMT output resistor on state

Following, it has been studied the effect of the input 1, on the output of the NOR gate. For this, firstly Vdd was setted into 15,50V, Vout measured value was 9V. Then it was applied 6mA to the input 1, after this the Input 1 SMT resistor was ”ON” and the output resistor as well, since Vout changed from 9V to 5,88V. The metallic channels created on the VO_2 material of the resistances, can be observed in Figure 6.18. After disconnecting the current source to the input, the input resistor switch off, but the metallic channel in output resistor continued (Vout=5,59) until the power supply Vdd was disconnected. This test was tried several times with the same result.

It was tried to switch on the gate, setting the power Vdd to 8,8V, the input 1 current applied was increased until 10mA (87mW) but with no succeed. Then, as it was tested before that the power necessary to induce the phase transition in the Input 1 was dependent of the power applied to the output resistance, it was tried to ”switch on” the Input 1, with 1mA in the input resistor and increasing Vdd until 30V, but the input resistor did not “switch off”. When Vdd was increased, it was appreciated a

increasing in the width of the metallic channel, the reason is that when the metallic channel is formed in a fragment of the VO_2 film, all the current flows through it, increasing the Joule-heat produced around the channel and posteriorly if the power applied on the channel rises, the heating produce induces the phase transition in the VO_2 particles in the vicinity of the channel and consequently increasing the metallic area.

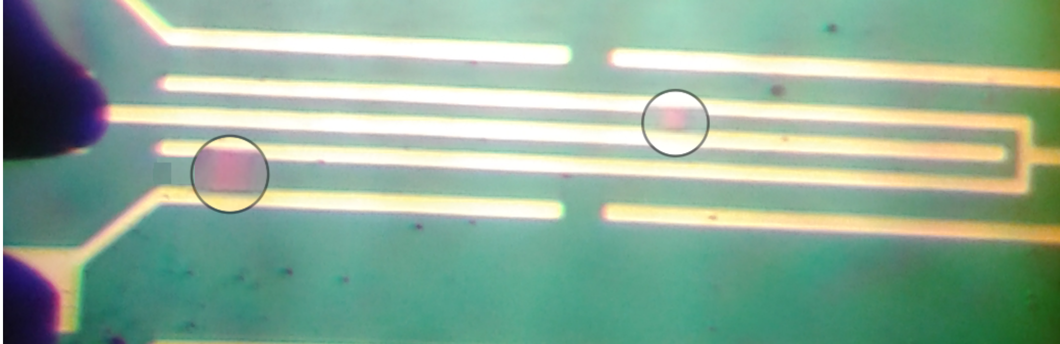

Figure 6.18: Metallic channels formed on the VO_2 at NOR gate, when Input 1 activated

After, the NOR gate function was proved in another place of the plate, but with the same geometry. Now, with Vdd=16V, the output resistor ”switches on”, Vout changes from 9V to 6V. To prove the NOR function, Vdd was decreased until Vout=7V, and the current applied to Input 1 was varied. The results are showed in the table above.

Table 4: NOR gate test activation with Input 1, Vout initial 7V

Input 1 current	Input 1 voltage	Vout	Input 1 resistor	Output resistor
6 mA	6,70 V	7,30 V	ON	OFF
7 mA	7,23 V	7,35 V	ON	OFF
8 mA	7,40 V	7,40 V	ON	OFF
9 mA	8,14 V	7,5 V → 5,8V	ON	ON
10 mA	8,61 V	6V	ON	ON

From the table, it is observed that the Input 1 resistor ”switches on”, when it is applied 6mA to the input, as expected from the last results, but the phase transition in the output resistor does not happen until it is applied 9mA (73mW) to the input. Since the power supply to the output resistor is less than in the previous test, the temperature on the resistor is less, so it is needed to produce more Joule-heat in the Input 1, that will propagate to the output resistor and will rise the temperature until achieve the critical point in the VO_2 film of the output resistor, and subsequently activate the gate.

The metallic channels appeared in different positions than in the previous test location of the plate, it can be saw in Figure 6.19, also it is detected a difference in the power required to switch on the output resistor, 144mW in the first place and 64mW in the second.

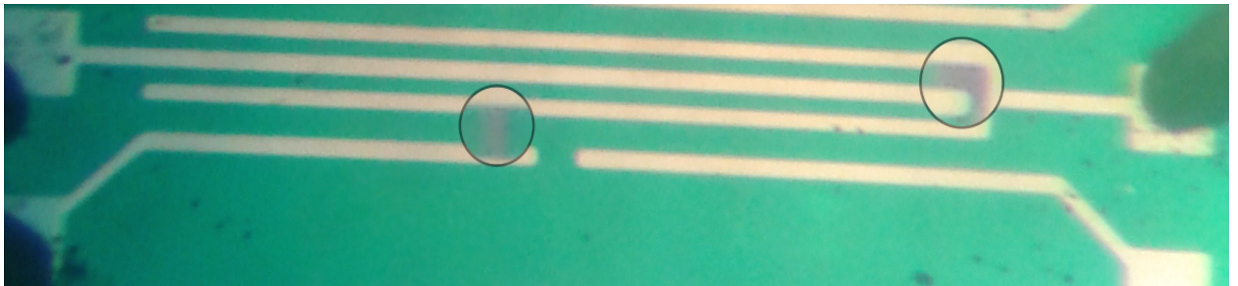

Figure 6.19: Metallic state channels formed on the VO_2 at NOR gate, when Input 1 activated

Finally, as in the previous case with the Input 1, it has been studied the characteristics of the Input 2 in the NOR gate. The current-voltage graphics of the Input 2 resistor, showed in the figures below, have been measured, firstly putting Vdd= 16V, (Vout=9V), which means a power of 63mW to the output resistor in semiconductor state, and then with the output resistor in the metallic state, which was reached at a estimated power of 166mW (Vdd=25,82V and Vout changed from 13V to 7,8V).

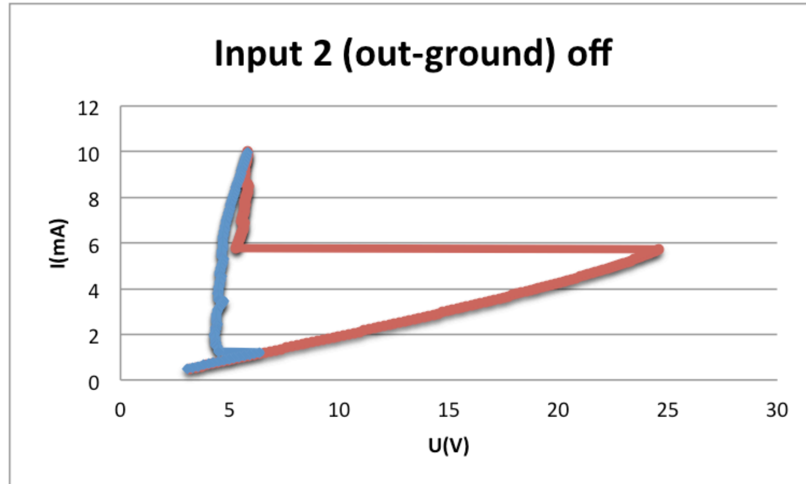

Figure 6.20: I-V characteristic between Input 2 and Ground contacts, when the SMT output resistor off state

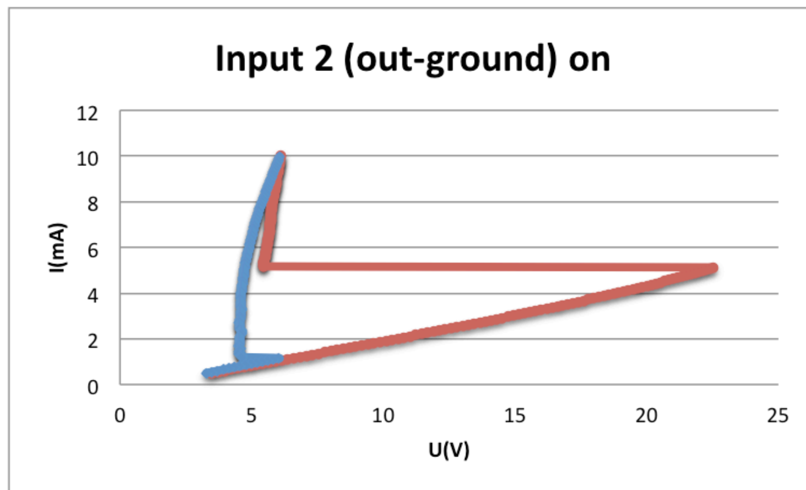

Figure 6.21: I-V characteristic between Input 2 and Ground contacts, when the SMT output resistor on state

The power used to switch on the input resistor, also varies depending on the state of the output resistor, in the first case with the output resistor in semiconductor state, it was needed 140mW and in the second case 115mW. The reason is the same explained for the input 1. It is also noticed that the power required to do the phase transition in the input 2, is higher than for the Input 1, this could be produced because the platinum contact of the input 2 (depicted in Figure 6.10) is larger than in the Input 1, this may stimulate the current leakage, producing that not all the current flows from the platinum contact to the ground contact in the shortest path, leading to a less Joule heating power to switch on the resistor and consequently to need more power.

When the Input 2 resistor switches on, with Vdd=16V (Vout=9V), the VO_2 channel of the output resistor also switches to the metallic state so the NOR gate is activated, the Vout changes from 9V to 5,2V. The NOR gate keeps ”ON” after deactivate the input resistor, so it presents memory of the last output value as in the previous case with the Input 1. For turning off the gate it is necessary to turn off the power supply.

7 Conclusion

The possibility of building integrated thermal logic gates based on the phase transition of the vanadium dioxide has been proved. It has been tested the functionality of a NOR thermal gate with four inputs, consisting on four VO_2 based SMT resistances, thermally coupled to another SMT resistance connected to a pull up resistor. Each of the four inputs current driven can switch on the NOR gate, producing a decreasing in the output voltage.

Through the previous studies on the VO_2 switches technology and the tests done, it can be deduced that similarly to this NOR thermal gate, it could be created other different gates. For example, a NAND gate function may be reproduced decreasing the power applied by the power supply, connected to the output through the pull-up resistor, so it will be necessary to activate more than one input to produce the Joule heating power enough to switch the output resistor; also, applying less current to the inputs, increasing the distance or reducing the thermal coupling between the inputs and the output resistor a NAND function or other gates could be created.

As discussed in chapter 4.3, it can be deduced that in relative large phonsistors size of the order of micrometres, actived by slow current/voltage pulses (or dc), the Joule heating is the key for the SMT on the VO_2. The switching times are larger, and the power consume is higher than in SMT resistors scaled down to nanoscale size. In the nano structures, the electric field effects are supposed to be the main reason of the SMT transition, in this nanoscale channel devices, the switching times could be reduced to nanoseconds and the power required would be also decreased, which will produce a better performance, even better than the current CMOS technology.

8 References

[1] M. Terraneo, M. Peyard and G. Casati: "*Controlling the energy flow in nonlinear lattices: a model for a thermal rectifier*", http://arxiv.org/abs/cond-mat/0201125v2, (2002 January)

[2] Baowen Li, Giulio Casati, Lei Wang: "*Thermal diode: Rectification of heat flux*", http://arxiv.org/pdf/cond-mat/0407093.pdf , (2004 October)

[3] Baowen Li, Giulio Casati, Lei Wang: "*Negative differential thermal resistance and thermal transistor*", www.arxiv.org, (2006 March)

[4] Baowen Li, Lei Wang: "*Thermal Logic Gates: Computation with Phonons*", www.ScienceDirect.com , (2007 October)

[5] Physicsworld: "*Phononics gets hot*", www.cse.nus.edu.sg, (2008 March)

[6] Nianbei Li, Jie Ren, Lei Wang, Gang Zhang, Peter Hänggi and Baowen Li: "*Colloquium: Phononics: Manipulating heat flow with electronic analogs and beyond*", www.physik.uni-augsburg.de, (2012 July)

[7] C. W. Chang, D. Okawa, A. Majumdar, A.Zettl: *"Solid-State Thermal Rectifier"*, www.sciencemag.org, (2006 September)

[8] Lei Wang and Baowen Li: "*Thermal memory: a storage of phononic information*", http://arxiv.org/pdf/0808.3311.pdf , (2008 August)

[9] Crunteanu, Givernaud, Leory, Mardivirin, Champeaux, Orlianges, Catherinot and Blondy: "*Voltage- and current-activated metal–insulator transition in VO2-based electrical switches: a lifetime operation analysis*", http://iopscience.iop.org, (2010 August)

[10] G Stefanovich, A Pergament and D Stefanovich: "*Electrical switching and Mott transition in VO_2*", http://iopscience.iop.org, (2000 May)

[11] Alexander Pergament: "*Metal-insulator transition: the Mott criterion and coherence length*", www.stacks.iop.org/JPhysCM/15/3217 , (2003 May)

[12] Yang Zhang, Shriram Ramanathan: "*Analysis of "on" and "off" times for thermally driven VO_2 metal-insulator transition nanoscale switching devices*", www.sciencedirect.com, (2011)

[13] You Zhou and Shriram Ramanathan: "*Correlated Electron Materials and Field Effect Transistors for Logic: A Review*", (2012)

[14] Márton C. Bein and János Mizsei: "*Contracting Current Paths in Vanadium Dioxide Thin Films*", www.ieeexplore.ieee.org, (2011 September)

[15] Joyeeta Nag and R F Haglund Jr: "*Synthesis of vanadium dioxide thin films and nanoparticles*", http://iopscience.iop.org, (2008 June)

[16] AJA INTERNATIONAL INC: "*Sputtering*", http://www.ajaint.com/what-is-sputtering.html, (visited: 2015 April)

[17] Qiu, Wen, Yang, Chen, Jing and Zhang: "*Electrically-driven metal-insulator transition of vanadium dioxide thin films in a metal-oxide-insulator-metal device structure*", www.sciencedirect.com, (2014 July)

[18] Dmitry Ruzmetov, Gokul Gopalakrishnan, Jiangdong Deng, Venkatesh Narayanamurti and Shriram Ramanathan: "*Electrical triggering of metal-insulator transition in nanoscale vanadium dioxide junctions*", JOURNAL OF APPLIED PHYSICS, http://scitation.aip.org, (2009 October)

[19] A. Zimmers, L. Aigouy, M. Mortier, A. Sharoni, Siming Wang, K. G. West, J. G. Ramirez, and Ivan K. Schuller: "*Role of Thermal Heating on the Voltage Induced Insulator-Metal Transition in VO2*", PHYSICAL REVIEW LETTERS, http://ischuller.ucsd.edu/papers/Paper%20512.pdf, (2013 January)

[20] Gokul Gopalakrishnan, Dmitry Ruzmetov and Shriram Ramanathan: "*On the triggering mechanism for the metal–insulator transition in thin film VO2 devices: electric field versus thermal effects*", Journal of Materials Science, (2009 April)

[21] You Zhou, Xiaonan Chen, Changhyun Ko, Zheng Yang, Chandra Mouli and Shriram Ramanathan: "*Voltage-triggered Ultra-fast Metal-insulator Transition in Vanadium Dioxide Switches*", IEEE, www.ieeexplore.ieee.org,(2013)

[22] János Mizsei, Jyrki Lappalainen, Márton C. Bein: "*Thermal-Electronic Integrated Logic*", 19th INTERNATIONAL WORKSHOP on Thermal Investigations of ICs and Systems, www.ieeexplore.ieee.org, (2013)

[23] Zheng Yang, Changhyun Ko, and Shriram Ramanathan: *"Oxide Electronics Utilizing Ultrafast Metal-Insulator Transitions",* www.annualreviews.org, (2011)