```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if
instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Register_1bit is
    port(
        DATA: in STD_LOGIC;
        EN: in STD_LOGIC;
        RELOJ: in STD_LOGIC;
        Q: out STD_LOGIC
     );
end Register_1bit;

architecture Behavioral of Register_1bit is
    signal AUX: STD_LOGIC;

begin
    Q <= AUX;

    process(RELOJ, EN)
    begin
        if falling_edge(RELOJ) and EN='1' then
            AUX <= DATA;
        end if;
    end process;

end Behavioral;
```