```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if
instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Register_19bits is
    Port (
        RELOJ : in STD_LOGIC;
        EN : in STD_LOGIC;
        PARALLEL_IN : in STD_LOGIC_VECTOR (18 downto 0);
        PARALLEL_OUT : out STD_LOGIC_VECTOR (18 downto 0)
    );
end Register_19bits;

architecture Behavioral of Register_19bits is

begin

    process (RELOJ, EN, PARALLEL_IN) is
    variable temp : STD_LOGIC_VECTOR (18 downto 0);

    begin
        if rising_edge(RELOJ) then
            PARALLEL_OUT <= temp;
            if (EN='1') then
                temp := PARALLEL_IN ;
            end if;
        end if;
    end process;

end Behavioral;
```