```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if
instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Register_16bits is
    port(
        DATA: in STD_LOGIC_VECTOR(15 downto 0);
        EN: in STD_LOGIC_VECTOR(3 downto 0);
        RELOJ: in STD_LOGIC;
        Q: out STD_LOGIC_VECTOR(15 downto 0)
     );
end Register_16bits;

architecture Behavioral of Register_16bits is

begin
    process(RELOJ)
    variable AUX: STD_LOGIC_VECTOR (15 downto 0);

    begin
        if rising_edge(RELOJ) then
            if EN(3)='1' then
                AUX(15 downto 12) := DATA(15 downto 12);
            end if;
            if EN(2)='1' then
                AUX(11 downto 8) := DATA(11 downto 8);
            end if;
            if EN(1)='1' then
                AUX(7 downto 4) := DATA(7 downto 4);
            end if;
            if EN(0)='1' then
                AUX(3 downto 0) := DATA(3 downto 0);
            end if;
        end if;
        Q <= AUX;
    end process;

end Behavioral;
```