```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if
instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Shift_Register_151bits is
    Port (
        RELOJ : in STD_LOGIC;
        EN : in STD_LOGIC;
        CARGAR : in STD_LOGIC;
        PARALLEL_IN : in STD_LOGIC_VECTOR (150 downto 0);
        DATA_IN : in STD_LOGIC;
        PARALLEL_OUT : out STD_LOGIC_VECTOR (150 downto 0);
        DATA_OUT : out STD_LOGIC
    );
end Shift_Register_151bits;

architecture Behavioral of Shift_Register_151bits is

begin

    process (RELOJ, EN, CARGAR, PARALLEL_IN, DATA_IN) is
    variable temp : STD_LOGIC_VECTOR (150 downto 0);

    begin
        if rising_edge(RELOJ) then
            PARALLEL_OUT <= temp;
            DATA_OUT <= temp(0);
            if (CARGAR='1') then
                temp := PARALLEL_IN ;
            elsif EN='1' then
                temp := DATA_IN & temp(150 downto 1);
            end if;
        end if;
    end process;

end Behavioral;
```