```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if
instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Register_3bits is
port(
    DATA: in STD_LOGIC_VECTOR (2 downto 0);
    RELOJ: in STD_LOGIC;
    Q: out STD_LOGIC_VECTOR (2 downto 0)
);
end Register_3bits;

architecture Behavioral of Register_3bits is
    signal AUX: STD_LOGIC_VECTOR (2 downto 0);

begin
    Q <= AUX;

    process(RELOJ)
    begin
        if rising_edge(RELOJ) then
            AUX <= DATA;
        end if;
    end process;

end Behavioral;
```