```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if
instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Contador_4bits is
    port(
        EN: in std_logic;
        RELOJ: in std_logic;
        RESET: in std_logic;
        OUTPUT: out std_logic_vector(0 to 3)
    );
end Contador_4bits;

architecture Behavioral of Contador_4bits is
    signal temp: std_logic_vector(0 to 3);

begin

    Output <= temp;

    process(RELOJ,RESET,EN)
    begin
        if RESET='1' then
            temp <= "0001";
        elsif(rising_edge(RELOJ) and EN = '1') then
            if temp="1111" then
                temp <= (others => '0');
            else
                temp <= temp + 1;
            end if;
        end if;
    end process;

end Behavioral;
```