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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if
instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Contador_9bits is
    port(
        EN: in STD_LOGIC;
        RELOJ: in STD_LOGIC;
        RESET: in STD_LOGIC;
        OUTPUT: out STD_LOGIC_VECTOR (8 downto 0)
    );
end Contador_9bits;

architecture Behavioral of Contador_9bits is
    signal temp : STD_LOGIC_VECTOR (8 downto 0);

begin
    Output <= temp;

    process(RELOJ, RESET, EN)
    begin
        if RESET='1' then
            temp <= (others => '0');
        elsif(rising_edge(RELOJ) and EN ='1') then
            if temp="11111111" then
                temp <= (others => '0');
            else
                temp <= temp + 1;
            end if;
        end if;
    end process;

end Behavioral;

```