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ABSTRACT

ZrO_2-graphene-ZrO_2 layered structures were built and their crystallinity was characterized before resistive switching measurements. Thin nanocrystalline ZrO_2 dielectric films were grown by atomic layer deposition on chemical vapor deposited graphene. Graphene was transferred, prior to the growth of the ZrO_2 overlayer, to the ZrO_2 film pre-grown on titanium nitride. Nucleation and growth of the top ZrO_2 layer was improved after growing an amorphous Al_2O_3 interface layer on graphene at lowered temperatures. Studies on resistive switching in such structures revealed that the exploitation of graphene interlayers could modify the operational voltage ranges and somewhat increase the ratio between high and low resistance states.

I. INTRODUCTION

Application of graphene, either directly deposited or transferred on other thin films functional in different devices,[1,2] has emerged as one of the major, focused, directions in the research and development of novel materials relevant to nanotechnology. For possible applications in nanoelectronics, for instance, graphene has been introduced in the structure of resistive random-access memories (RERAM) in order to enhance different physical properties such as mechanical flexibility and transparency.[3] The fact that these devices fit, but only partially, to some memory technology requirements in terms of operating voltages, switching times, and sufficient on/off voltage and current ratios makes the deposition and resulting quality of functional graphene layers worth further investigations.[4]

The preparation of large-area graphene by chemical vapor deposition (CVD) on metal substrates[5–12] and transferring to various substrates[13–16] is widely exploited.

For graphene-based stacks, atomic layer deposition (ALD) is a promising method, which should allow accurate control over the thickness of the deposited layer.[17] However, the deposition of a uniform dielectric layer on graphene is still difficult.[18,19] On the other hand, boundary regions, wrinkles, and impurities from graphene growth and lift-off process have beneficial effects on the nucleation of ALD dielectrics such as Al_2O_3 and HfO_2.[18,20]

Memristors have been built on several oxides grown by ALD, using HfO_2 and Al_2O_3 oxides[21] or SiO_2-Nb_2O_5 nanolaminates[22] and combining sputtering and ALD methods[23] or using pulsed laser deposition for amorphous ZrO_2 films.[24] To enhance resistive switching (RS) performance in a ZrO_2-based RERAM, Mo (Ref. 25) or thin TiO_x layers[26] have been embedded in ZrO_2 host films. It has been noticed some time ago that a combination of relatively conductive and relatively better insulating materials, if deposited alternately, can provide decrement in the forming voltage to the level of switching voltages. This was examined, e.g., in $HfO_x/TiO_x/HfO_x/TiO_x$ multilayers.[27] Conventionally, resistively switching films should consist of materials, which are mostly insulating dielectrics, but inherently defective whereby the defect densities should be controllable and stabilized at tunable levels. ZrO_2 as an insulating metal oxide is known as a dielectric easily formed in metastable phases, which can be assisted by oxygen vacancy defects. Such defects can also be laterally tuned, for example, by depositing $ZrO_2/ZrO_{2-x}/ZrO_2$ stacks[28] containing an artificially formed oxygen deficient and laterally probably more conductive ZrO_{2-x} layer between dioxide layers. Such structures may, due to the additional internal barriers, exhibit quicker

conductive channel formation process together with implications of multilevel switching behavior. Moreover, the switching properties of metal oxide-based media may become usefully modified by insertion of conductive materials in the host films. For instance, Al_2O_3/Cu/Al_2O_3 based multilayers have been realized and described as resistively switching media.[29] In the latter stacks, the conductive Cu layer acted as a connector between conductive filaments formed in Al_2O_3, providing feasible switching process. Analogously, three sequential layers of ZrO_2/Cu/ZrO_2 (with thickness of 20/3/20 nm) were repeatedly deposited as resistively switching media,[30,31] where the ZrO_2 host layer performed as solid electrolyte.

Analogously, laterally conductive graphene barriers could be introduced as useful functional constituents in multilayered resistively switching media. Resistively switching cells have been formed, e.g., as multilayered graphene oxide sheets,[32] multilevel switching media based on graphene oxide sheet embedded in plastic host,[33] or graphene-Al_2O_3 layers also suited to transparent flexible switching devices.[34] Between Ta_2O_5 host layers, the embedded single layer graphene sheets have made possible tuning ionic conduction currents in the switching regime.[35]

Moreover, graphene has been used as an electrode to form an atomically thin memory structure[3,36] or employed as an active layer in RERAM devices to allow multilevel switching[37] or to block atomic diffusion and limit the number of conductive filaments in the dielectric layer.[3] Furthermore, creating nanoscale openings with controlled sizes in graphene ion-blocking layers have enabled tuning of resistive switching behavior in a typical oxide-based memristor.[35] However, ZrO_2/graphene/ZrO_2 RERAM-like structures based on CVD-grown large-area graphene have not been systematically discussed before.

Considering the knowledge gained earlier on resistive switching media formed on the basis of either ZrO_2 or graphene, combinations of ZrO_2 layers grown using atomic layer deposition with graphene obtained by chemical vapor deposition method and transferred between ZrO_2 host layers may open up a new possibility when seeking routes to low-cost and flexible RERAM cells, provided that the fabrication processes of component layers can further be developed.

In the present study, the quality of graphene layers grown by CVD and transferred onto ZrO_2 films pre-grown by ALD was evaluated. ZrO_2 films were then grown also on the transferred graphene in order to create a triple-layer structure, where graphene was embedded in ALD-grown ZrO_2. Two different ALD routes to ZrO_2 films on transferred large-area CVD-grown graphene have been studied and compared. Amorphous Al_2O_3 buffer layers were grown on graphene, prior to the ALD of ZrO_2, at lowered temperatures and exploited in order to structurally affect graphene as little as possible when coating its surface with crystalline ZrO_2. The structural integrity of the multilayers was evaluated by microscopic and spectroscopic means. Concurrently, it was necessary to examine whether the application of graphene in a ZrO_2-based medium can modify the parameters of resistive switching and, possibly, allow multilevel switching on RERAM-like structures.

II. EXPERIMENT

Before the fabrication of dielectric/graphene/dielectric stack structures, graphene was grown on a commercially available 25 μm thick polycrystalline copper foil (99.5%, Alfa Aesar) using a home-assembled CVD reactor. Prior to graphene deposition, the copper foils were annealed at 1000 °C in Ar/H_2 (both 99.999%, AGA Estonia) flow. Then, the copper foils were exposed to a mixture of 10% CH_4 (99.999%, AGA Estonia) in Ar also at 1000 °C to form graphene.

After the CVD process, the graphene film was transferred from copper foils onto ALD-grown metal oxides by using poly(methylmethacrylate) (PMMA; with molecular weight of ~996 000 g/mol, Sigma-Aldrich) as the supporting material. The PMMA solution in chlorobenzene (Sigma-Aldrich) was carried by spin-coating onto one side of the graphene/Cu/graphene structures and the graphene film on the uncoated side of the foil was removed by plasma treatment. Then, the Cu foil was dissolved in 1M $(NH_4)_2S_2O_8$ solution overnight. The floating PMMA/graphene film was rinsed with de-ionized water and transferred onto substrates. The samples were dried in air and then heated at 70 °C to allow the PMMA film to soften in order to improve the contact between graphene and the substrate. Finally, the supporting layer was removed by dissolving it in dichloromethane (Sigma-Aldrich).

For the deposition of ZrO_2 dielectric films, $ZrCl_4$ and H_2O as the metal and oxygen precursors, respectively, were used. The ZrO_2 films were grown in an in-house built hot-wall flow-type ALD reactor.[38,39] The pressure in the reactor was about 250 Pa. $ZrCl_4$ was evaporated in an open boat inside the reactor at 155 °C and transported by in an inert carrier gas (N_2) flow to the substrates. $ZrCl_4$ was the chosen precursor primarily because the growth of ZrO_2 from $ZrCl_4$ and H_2O is an inherently carbon-free process, although small amounts of carbon impurities in the solid films deposited cannot be avoided, due to either reactor contamination or temperature-enhanced interdiffusion between neighboring layers. At the same time and for comparison, alkylamides, including those of zirconium, which may be considered perhaps more recognized metal precursors in contemporary nanoelectronics, are also carbon-containing precursors. It has been studied and revealed some time ago that ZrO_2 grown by ALD from alkylamides contain residual carbon whereby the carbon content is quite sensitive to the cycle time parametrization.[40] In any case, residual carbon content elevated in ZrO_2 layers could further complicate the recognition of graphene in stacked structures, especially when probed by cross-sectional energy dispersive x-ray spectroscopy (EDX) profiling. In addition, $ZrCl_4$ does not thermally decompose at any practical deposition temperature, which has earlier been examined also in a reactor similar to that used in the present study.[41] One can also mention that, at the same time, the onsets of thermal decomposition in the case of alkylamides of zirconium lie in the temperature range of 250–300 °C.[40,42] One has to recognize, on the other hand, that the ZrO_2 films grown from $ZrCl_4$ certainly contain residual chlorine. In the films earlier grown under the same reactor conditions, the chlorine content has been measured by time-of-flight elastic recoil detection analysis (TOF-ERDA) and did not rise above 0.5 at. % in the ZrO_2 films deposited at 300 °C.[43]

Two different ALD routes to ZrO_2 films on CVD graphene were studied and compared. At first, 90 ALD cycles at 300 °C were used to form a ZrO_2 film on the TiN substrate, with the deposition rate of 0.7 Å/cycle. These substrates were pieces cut out of Si(100) wafers with a resistivity of 0.014–0.020 Ω cm, i.e., Si boron-doped to the concentrations up to 5×10^{18}–1×10^{19}/cm^3, and coated with

a 10 nm thick titanium nitride layer. Such structures further enabled convenient through-wafer measurements during the electrical evaluation of the oxide layers.

TiN was grown by pulsed chemical vapor deposition using a batch $TiCl_4/NH_3$ process[44,45] at temperatures of 450–500 °C in an ASM A412 Large Batch 300 mm reactor at Fraunhofer IPMS-CNT. For ZrO_2, the ALD cycle times were 4–3–2–5 s, denoting metal precursor pulse length–purge–water pulse length–purge times. After transferring graphene on the Si/TiN/ZrO_2 substrate, another ZrO_2 film was grown by ALD onto the transferred graphene layer [Fig. 1(a)]. In the separate experiment, Al_2O_3 seed layers were additionally employed prior to the ZrO_2 film growth in order to improve the nucleation of ZrO_2 and ease the ZrO_2 film growth on graphene. At first, two growth cycles of Al_2O_3 from trimethylaluminum as the metal precursor and H_2O as the oxygen precursor were applied at 28 °C, followed by the next two cycles of Al_2O_3 at 200 °C. The cycle times for the deposition of Al_2O_3 were 2–2–2–5 s in both cases. Deposition of Al_2O_3 was followed by 80 cycles of ZrO_2 at 300 °C, in order to grow continuous ZrO_2 film [Fig. 1(b)]. Similar structures were comparatively prepared without graphene embedded in ZrO_2, as well.

Two sequentially applied growth temperatures for ALD oxide films on graphene were reported as useful, as proven earlier in the cases of ALD of HfO_2 (Ref. 46) and Al_2O_3.[47] In the latter studies, it was observed, that the deposition of the first oxide layers at strongly lowered temperatures have assisted in the creation of the first but already functional nucleation layer on top of chemically inert graphene, promoting the further, intensified, growth of metal oxide films. Particularly, in the paper by Pirkle *et al.*,[47] the authors recognized that even if the Al_2O_3 film grown at room temperature may remain inferior to those grown at elevated temperatures, in terms of dielectric properties, the exploitation of low process temperatures for the very first seed layer enhances the nucleation density of metal oxide on relatively inert graphene and also may avoid further damaging of graphene by growing overlayers at higher temperatures.

The surface morphology of the graphene and ZrO_2 films was evaluated by high-resolution scanning electron microscopy (HR-SEM; FEI Helios NanoLab 600). The focused ion beam [FIB; FEI NanoLab 600 Dual Beam (SEM-FIB) system] *in situ* lift-off technique was used to prepare the high-resolution transmission electron microscopy (HR-TEM) sample. TEM analysis was performed in the scanning mode (STEM) at 200 kV using a Cs-probe corrected transmission electron microscope (FEI Titan Themis 200) equipped with an EDX system.

Structural characterization of graphene was performed by using a micro-Raman spectroscopic system Renishaw inVia at the excitation wavelength of 514 nm. The radiant power was set to less than 1 mW in order to avoid the destructive effect on the graphene due to local heating.

The thickness, density, and crystal structure of the deposited ZrO_2 films were evaluated by x-ray reflectometry and by grazing incidence x-ray diffractometry (GIXRD), respectively, using Cu Kα radiation (x-ray wavelength of 0.154 06 nm, diffractometer SmartLaB, Rigaku). The elemental composition of the films was measured in the present study by a wavelength-dispersive x-ray fluorescence (WD-XRF) spectrometer Rigaku ZSX400 with the zsx software (version 5.55). The standard target element is Rh (Rh-KA excitation energy is 23.2 KeV). The x-ray emission was gathered from the area with a diameter of 10 mm.

For the electrical measurements, the stack structures were equipped with Ti electrodes (110 nm) that were deposited through a shadow mask[48] by electron beam evaporator at 230 °C in high vacuum (10^{-6}–10^{-7} mbar). To provide ohmic contact, the backside

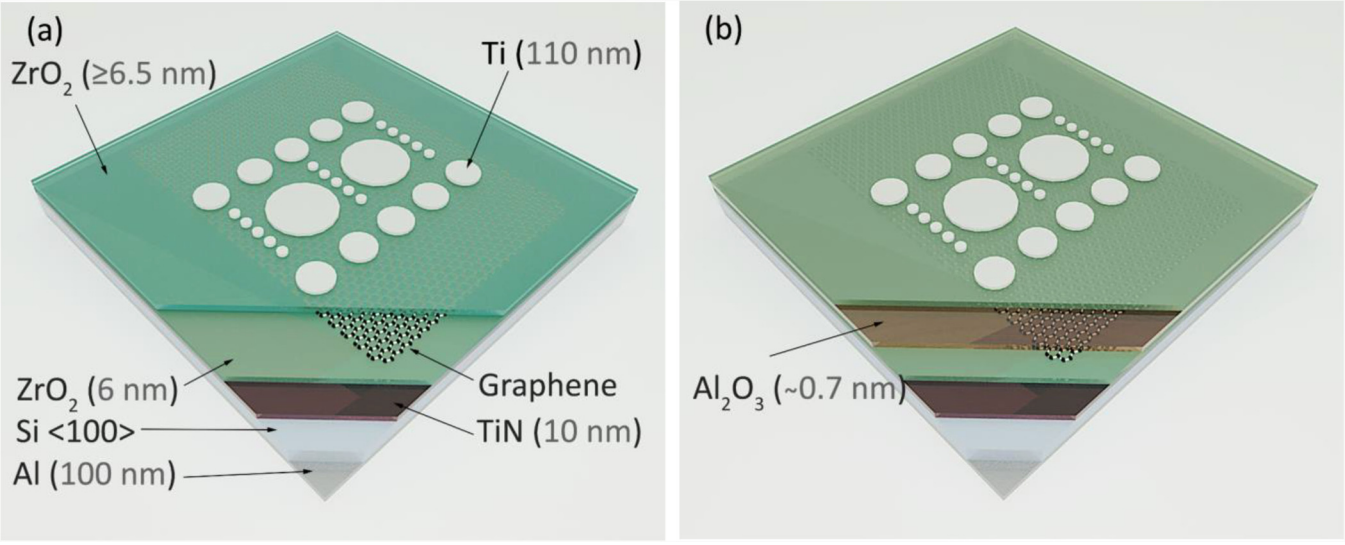

FIG. 1. Schematic illustration of stack structures. Ranked from bottom to top: (a) Al-electrode/Si/TiN/ZrO_2/graphene/ZrO_2/Ti electrodes and (b) same structure with Al_2O_3 interface between graphene and ZrO_2 film. The schematic layer thicknesses are not to scale.

of silicon substrate was etched with hydrogen fluoride solution and covered with evaporated aluminum with a thickness of 100 nm at room temperature. Electrical measurements were carried out in a light-proof and electrically shielded box. The Ti electrodes had a circular shape and cross-sectional diameters of 50 μm (area 0.002 mm^2), 250 μm (area 0.052 mm^2), and 500 μm (area 0.204 mm^2). Samples were electrically characterized in both dc and ac regimes using a Keithley 4200 SCS semiconductor analyzer. The bias voltage was applied to the top electrode, while the bottom electrode was grounded. To record the admittance parameters, a small signal of 30 mV rms was superimposed with the dc bias voltage. The measurement frequency did not affect the resistive switching behavior in the range of 20 kHz–1 MHz. The forming procedure was carried out as a voltage sweep with positive bias, and the current limiting was applied to avoid irreversible breakdown of devices. In general, the forming took place under about 4 V bias.

III. RESULTS AND DISCUSSION

A. Morphology and structure

Graphene was formed on the metal (copper) surface after initial nucleation, growth, and, further, coalescence of graphene domains as described before.[49] SEM studies implied the formation of almost continuous graphene layers with clear boundaries between large-area domains. Hence, grain boundaries that are part of any polycrystalline material were also formed in large-area single layer graphene to a greater or lesser extent, depending on the CVD conditions.[49]

The transferred graphene films had some ruptures and wrinkles emerged during the transferring process. Rupturing of the graphene was somewhat expected as it has been noticed and described before.[50] Ruptures, boundary regions, and graphene wrinkles can alter surface properties, which actually would have a beneficial effect on the nucleation of ALD dielectrics.[18,50,51] Figures 2(a) and 2(c) show that the ZrO_2 film on TiN/Si substrates appear continuous and quite uniform with few microscopic surface defects. In contrast, the nucleation and growth of ZrO_2 on graphene without Al_2O_3 interface layer appeared markedly less homogeneous even after 90 cycles at 300 °C [Figs. 2(b) and 2(d)].

In addition to its polycrystalline[52] nature, as it can be considered after actual synthesis processes, graphene is also hydrophobic and inert. Therefore, the deposition of a uniform dielectric is challenging due to the necessity to apply alternating pulses of water and other precursor materials in ALD. However, the ZrO_2 film on graphene turned out more uniform and defect free when using two-step deposition comprising an Al_2O_3 seed layer [Fig. 2(d)]. Al_2O_3 could physisorb onto graphene by the van der Waals forces at lower temperatures, causing minimal alterations to the quality of graphene. Thus, absorbed Al_2O_3 could act as nucleation sites, and their consistency would play an important role in the growth of the ZrO_2 top layers, as described more specifically earlier.[53]

Figure 3(a) shows a cross-sectional STEM image of ZrO_2/graphene/ZrO_2 stack structure. The top and bottom ZrO_2 films are clearly seen in the image. The location of the ZrO_2 films was confirmed by EDX mapping of zirconium [Fig. 3(c)] taken from the area given in Fig. 3(b). The graphene layer, the presence of which in the region chosen for the preparation of the STEM sample was confirmed by Raman measurements (Fig. 4), is not discerned in the image. A single monolayer, planar, graphene sheet could not possibly be convincingly visualized in cross-sectional images. The increased thickness of the C-rich region is due to the roughness of the graphene-ZrO_2 interfaces. One can, however, rely on a justified assumption that the composition profile does not change significantly along the interface in the case of ALD-grown multilayers. Nonetheless, a nanocrystalline metal oxide film cannot grow atomically smooth, and also the graphene layer, as adhered to the oxide substrate, does not necessarily follow the substrate topography. This inevitably requires averaging of the interface positions through the whole cross-sectional sample thickness.[54] In the latter paper, it was realized that the total width of a visually recognized interface

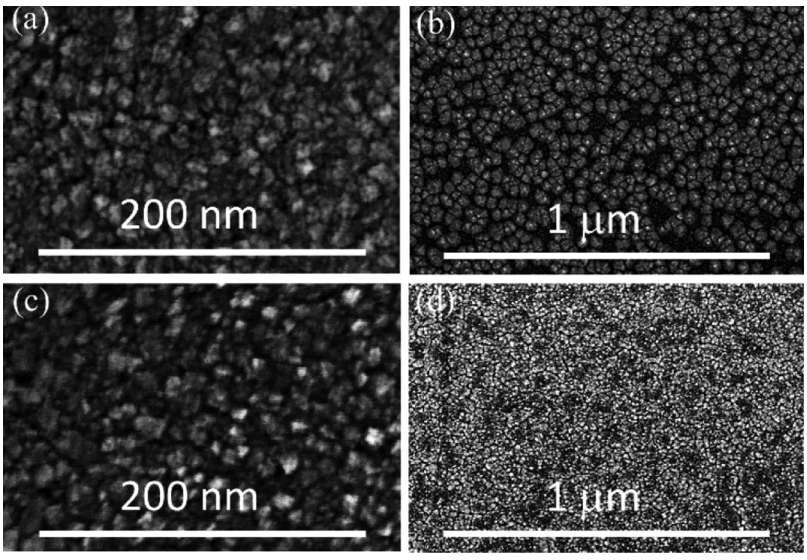

FIG. 2. SEM images of (a) Si/TiN/ZrO_2/ZrO_2, (b) Si/TiN/ZrO_2/graphene/ZrO_2, (c) Si/TiN/ZrO_2/Al_2O_3/ZrO_2, and (d) Si/TiN/ZrO_2/graphene/Al_2O_3/ZrO_2 structures.

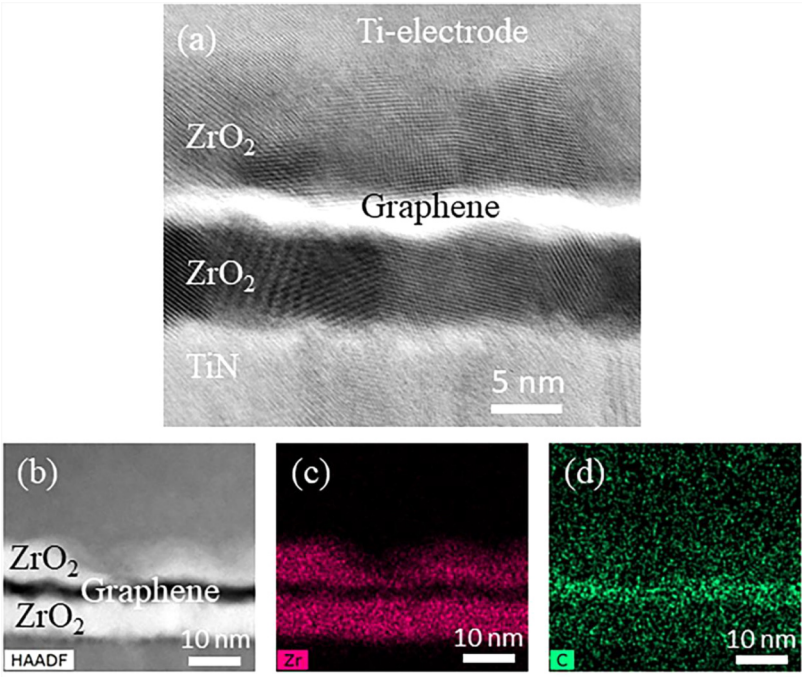

FIG. 3. (a) Cross-sectional high-resolution STEM bright field image of the ZrO_2/graphene/ZrO_2 stack structure. STEM high-angle annular dark field image (b) and EDX elemental mapping [(c) and (d)] of zirconium and carbon in the ZrO_2/graphene/ZrO_2 stack structure.

by using two-dimensional information from either images or chemical maps does, thus, not necessarily match with the physical thickness of an interfacial layer. In regard with embedded graphene layers, Lee *et al.*[35] have observed graphene layers between Ta_2O_5 films in resistively switching structures and obtained cross-sectional images analogous to those acquired in our study.

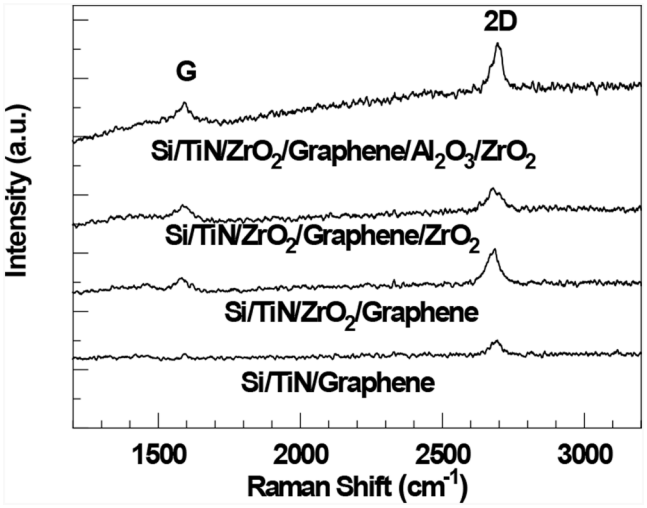

FIG. 4. Raman spectra of graphene-based stack structures in the case of differently stacked structures described by labels.

Regarding the results of Raman spectroscopy, all graphene-based structures showed two bands in the spectra, clearly related to graphene, at ~1586 cm^{-1} (G band) and ~2687 cm^{-1} (2D band), as measured on reference silicon substrates. In the case of the Si/TiN substrate, the G band was extremely weak (Fig. 4). In this regard, certain earlier studies have indicated that the effect of substrate coupling weakened the Raman signal of graphene and, therefore, the G band can become suppressed.[55] Since the overall signal of the graphene bands was generally low on the investigated stack structures in the present study, the D band at 1350 cm^{-1}, indicating graphene defects, was also difficult to detect even after the ALD process. The Raman measurements additionally indicated that the graphene should be predominantly single-layered, because the I_{2D}/I_G value was about 2 and the 2D band could be fitted by a single narrow Lorentzian function on Si/SiO_2/graphene reference samples.[55] In the present study, in the case of stack structures with a graphene interlayer, the 2D band was broadened and moderate shift in the locations of the main bands has occurred as showed in Table I, indicating that the formation of graphene was affected by the substrate, surface treatment, and dielectric layers.[55,56] These shifts are also associated with deflection, strain, or doping.[18,55,56]

The top layer ZrO_2 without Al_2O_3 interface probably serves as an effective passivation layer, causing the enhanced air stability of graphene.[19] Doping might be induced when graphene was covered with Al_2O_3/ZrO_2, resulting in a shift of G and 2D bands like has been reported previously by Wang *et al.*[56] A similar result is seen in our Table I.

Figure 5 represents the results of phase analysis by GIXRD. The ZrO_2 films grown to the thicknesses of around 6 nm on Si and Si/TiN substrates showed a few diffraction reflections that could be

TABLE I. Raman data (fitted in accord with Lorentz function) of graphene-containing structures. The average Raman shifts values are to reflect the effects of substrate and dielectric layers on graphene. The parameters shown express the positions of G and 2D bands (ω_G and ω_{2D}, respectively) and FWHM values for 2D bands (Γ_{2D}).

	Sample	ω_G (cm^{-1})	ω_{2D} (cm^{-1})	Γ_{2D} (cm^{-1})
Effect of substrate to graphene	Si/SiO_2/graphene (reference)	1586	2687	30
	Si/TiN/graphene	1590	2688	40
	$Si/TiN/ZrO_2$/graphene	1581	2678	48
Effect of deposited dielectric layers on graphene	$Si/TiN/ZrO_2$/graphene/ZrO_2	1586	2682	52
	$Si/TiN/ZrO_2$/graphene/Al_2O_3/ZrO_2	1588	2694	40

assigned to cubic or tetragonal phases. As expected for the films grown to thicknesses in the range of tens of nanometers only,[57] it was not possible to distinguish between these phases because of severe overlapping and increased broadening of reflections. The phase determination relies mainly on the basis of the strongest reflections which, when located at 30.1° and 50.2°, are attributable to the 111 and 220 reflections of the cubic (ICDD PDF 049-1642) phase, and when located at 30.3° and 50.4° are attributed to the 011 and 112 reflections of the tetragonal (ICDD PDF 050-1089) phase of ZrO_2, respectively. The ZrO_2 films on graphene possessed the same phase composition, and its thickness was around 6.5 nm. Furthermore, after using the ~0.7 nm Al_2O_3 as the amorphous intermediate nucleation layer before the deposition of ZrO_2, the main ZrO_2 reflections at ~30° and ~50° were broadened significantly as compared to those in the ZrO_2 layers grown in stacks without interfacial Al_2O_3 layer structures. This can, plausibly, be attributed to the growth of more homogeneous and continuous, but also rather thin ZrO_2 layer on another oxide, Al_2O_3, as compared to the tendency of formation of larger but more separated and discontinuous ZrO_2 nanocrystals on chemically quite foreign carbon surface. Similar phenomena have been observed earlier as well.[58] However, the broadening of the ZrO_2 diffraction reflections was the strongest in graphene/Al_2O_3 structures compared to other stack structures studied in this work, referring to the decrease in crystallite size in the top ZrO_2 layer.[58] If the main GIXRD reflection at 30.3° was used for evaluating the size of crystallites in accord with Scherrer's formula and using standard reference material SRM-660 (LaB_6) to take into account instrumental broadening, one could obtain an x-ray crystallite size varied in different structures in the range of 5–10 nm (standard deviation ~1 nm). As expected, in the case of graphene-aided interlayered structures, the crystallite size of the top layer ZrO_2 varied in range from 7.5 (with Al_2O_3 interface) to 8.5 nm. In those samples where ZrO_2 was deposited on TiN or Si substrates, the average size of crystallites was around 5 nm. For $Si/TiN/ZrO_2/Al_2O_3/ZrO_2$ and $Si/TiN/ZrO_2/ZrO_2$ structures, the average size of crystallites was 9 and10 nm, correspondingly. The thicknesses of the dielectric layers and the average sizes of the crystallites are in a good agreement with the TEM images (Fig. 3). Regarding the degree of the film purity in terms of the residual contamination, the results of WD-XRF measurements revealed the chlorine content in the samples as low as 0.5–0.6 at. %, which reasonably well compares to the earlier results obtained by TOF-ERDA,[43] carried out on ZrO_2 films grown under the same reactor conditions.[38,39]

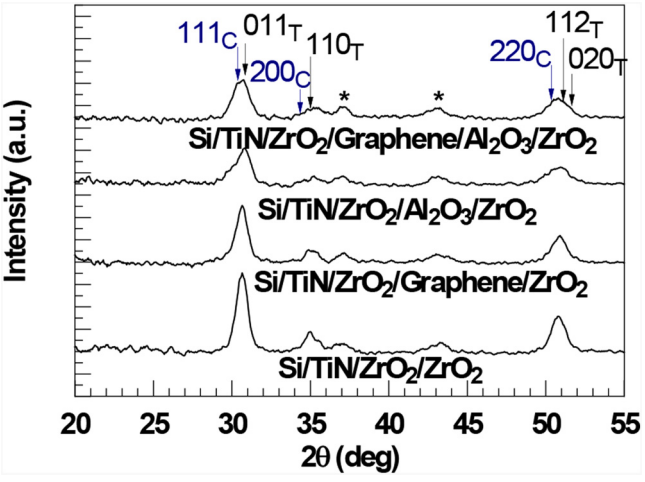

FIG. 5. Background subtracted GIXRD diffraction patterns of different stack structures. Reflection of Si/TiN substrate is marked by asterisks.

B. Electrical behavior

In order to follow the effect of graphene layer on electrical properties, the devices were selected on the areas with graphene and on the areas without graphene (Fig. 6).

The electroforming of the RS process (Fig. 7) was observed and recorded on both types of stack structures, that is, with and without graphene interlayers. The initial leakage currents before electroforming were in the range of some tenths of a picoampere at 0.1 V bias. After the electroforming step, the leakage current was increased about nine orders of magnitude to a range of tenth of a microampere at the same bias voltage.

It was noticed that one stack structure containing a graphene interlayer showed nearly two times lower forming voltage compared to devices without a graphene interlayer. It can be discussed whether the graphene or ZrO_2 top layer as shown in SEM image [Fig. 2(b)] was more uniform beneath this certain electrode than the others, which were measured in the area of graphene layer, or vice versa. From the electroforming perspective, it means that conductive filaments formed under voltage potentials lower than those in other devices with thicker stacks. It is necessary to point out that a similar reference structure as Al/Si/TiN/ZrO_2/Ti (Fig. 7), that is,

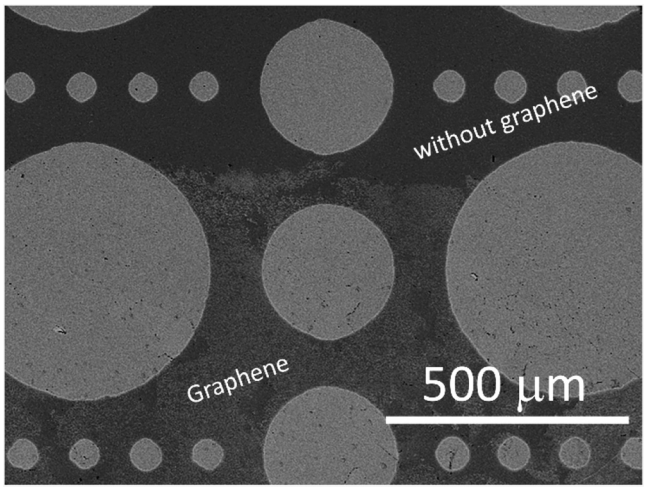

FIG. 6. SEM image of evaporated Ti electrodes with different sizes on stack structures.

the structure without graphene, demonstrated forming voltage of the same magnitude. It is worth pointing out that in the case of the stack structure with a graphene interlayer and low forming voltage, the leakage current was initially two magnitudes lower before the first sudden increase of current at ~1 V before the final forming at about 2.2 V [Fig. 7(a)]. If this initial low current curve was discarded and projected two magnitudes higher [dashed line on Fig. 7(a)] the resulting electroforming loop became similar to that in the Al/Si/TiN/ZrO_2/Ti layer device [Fig. 7(b)]. As one could expect, thinning of ZrO_2 films to 6 nm allowed the leakage current to increase. In the case of Al/Si/TiN/ZrO_2/Ti, as a reference structure, the leakage currents were in range of nanoamperes, and in case of Al/Si/TiN/ZrO_2/graphene/ZrO_2/Ti and Al/Si/TiN/ZrO_2/ZrO_2/Ti, the leakage currents were in range of picoamperes. According to GIXRD measurements (Fig. 5), the average crystallite size of ZrO_2 in Si/TiN/ZrO_2 samples was almost equal to the thickness of the structure (5 nm compared to 6 nm); thus, probability of penetrating grain boundaries between the electrodes of the structures was high. As mentioned in the literature,[59] the grain boundaries of the ZrO_2 film are the dominant paths for the leakage current. The double layer ZrO_2 embedding the graphene interlayer and further the same stack with the Al_2O_3 interface layer were both more uniform and were thicker (14–15 nm). The first sudden rise of forming current (the step itself) of the Al/Si/TiN/ZrO_2/graphene/ZrO_2/Ti structure with lower forming voltage [Fig. 7(a)] may be due to the two stacked layers of different morphology, which cause the forming to take place in two steps at different voltage levels. If this type of two-step resistivity change would have happened also during further RS, then from this perspective, it would be worth to investigate if graphene could produce multilevel RS.

RS behavior was repeatable in both types of devices, i.e., with and without graphene interlayer. The conventional resistive switching current-voltage characteristics were measured along with linear voltage sweeps and resulted in uniform switching with a defined high resistive state (HRS, R_{on}) and low resistive state (LRS, R_{off}), although the difference between those states was rather small as the R_{off}/R_{on} ratio was around 2. The resistive switching behavior was of bipolar counterclockwise type as for the switching from one resistive state to another different polarity of the applied voltage was needed. The switching from HRS to LRS, i.e., the SET procedure, took place during positive voltage sweep and switching from LRS to HRS, and RESET took place during the negative voltage pulse sequences (counterclockwise

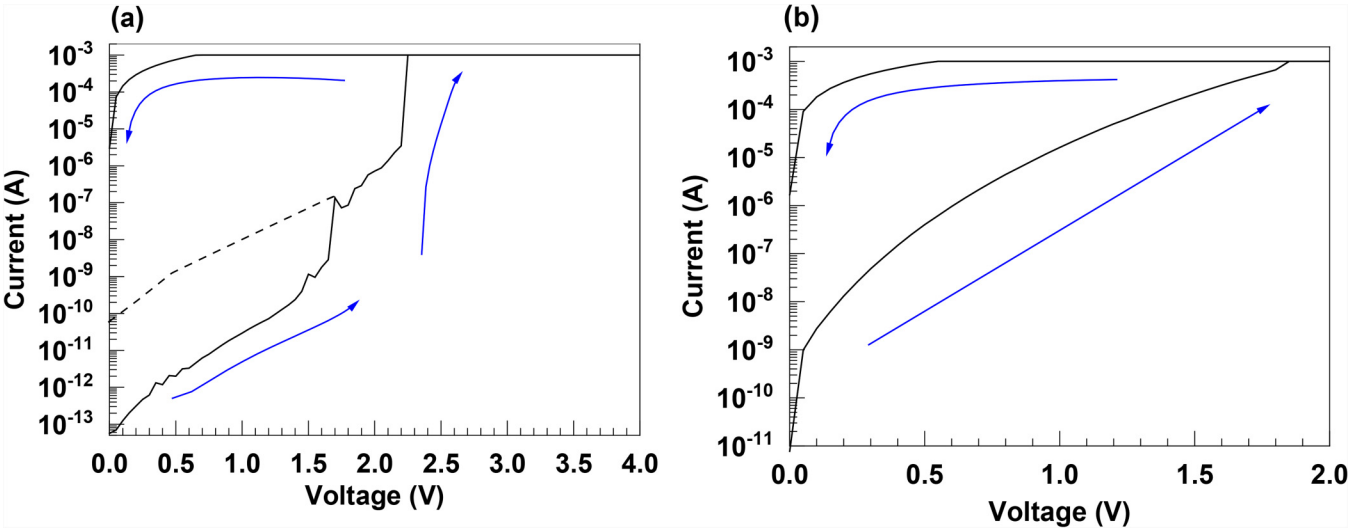

FIG. 7. Electroforming loops for (a) Al/Si/TiN/ZrO_2/graphene/ZrO_2/Ti and (b) Al/Si/TiN/ZrO_2/Ti stack structures. The Ti dot electrode area was 0.002 mm^2.

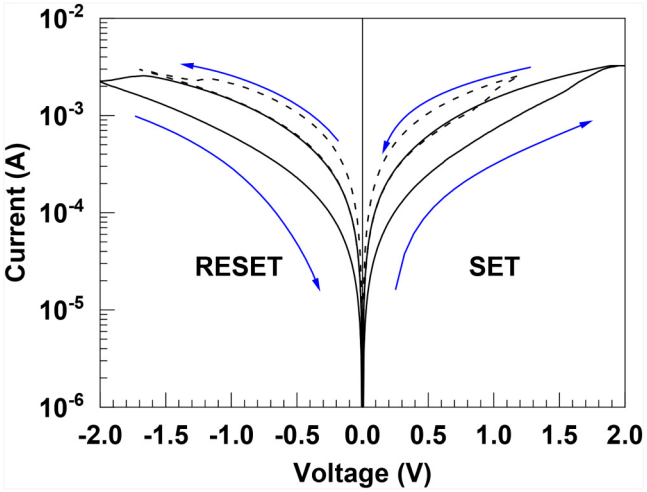

FIG. 8. Current-voltage loop measured in conventional resistive switching mode for Al/Si/TiN/ZrO_2/graphene/ZrO_2/Ti (solid line) vs Al/Si/TiN/ZrO_2/ZrO_2/Ti (dashed line) structures.

RS). In the case of the stacked structures with the graphene interlayer, the voltages for SET and RESET appeared more symmetric comparing the ranges of voltages where both SET and RESET procedures are recorded. In the samples with graphene, both SET and RESET occurred at around +2 and −2 V, respectively, while the samples without graphene interlayer switch to LRS (SET) at around 1 V. Current-voltage characteristics comparison demonstrated that in the case of graphene being present in similar structures, RS took place at lower currents and the memory window (R_{off}/R_{on}) was somewhat wider (Fig. 8).

As graphene is supposed to have good conductance in its lateral dimension, it may be viewed as a virtual electrode and the first sudden increase in the electrical current might occur when one of the metal or metal nitride electrodes becomes connected to the virtual graphene electrode through conductive paths or filaments forming under the electric field. However, conductance and capacitance measurements are not exactly consistent with these assumptions, because the devices with the internal graphene layer seemed to possess lower conductance and higher capacitance than those without graphene interlayer. This could be observed from conductance and capacitance memory maps (Fig. 9) measured with small signal during the programming voltage sweep.[60] Hence, the graphene layer seemed to act more like a barrier to charge carriers. One can suppose that vertically (from top to bottom) graphene acts as a barrier for the leakage current, but once it gets connected with conductive paths, then in the planar direction it conducts electricity and raises the probability of different conductive filaments to get connected with each other. For example, if the RS loops of Al/Si/TiN/ZrO_2/graphene/ZrO_2/Ti structures were compared to the reference object, i.e., Al/Si/TiN/ZrO_2/Ti, then the RS currents occurred nearly one magnitude higher in the first case.

The small signal current hysterons (memory maps) measured indicated that the application of an internal graphene layer could lower the currents by nearly 100 μA. The capacitance and conductance memory maps indicated that graphene lowered the conductance, hence raising the resistance and capacitance as expected. The capacitance memory maps, if compared in samples with and without internal graphene, reveal that graphene-containing devices

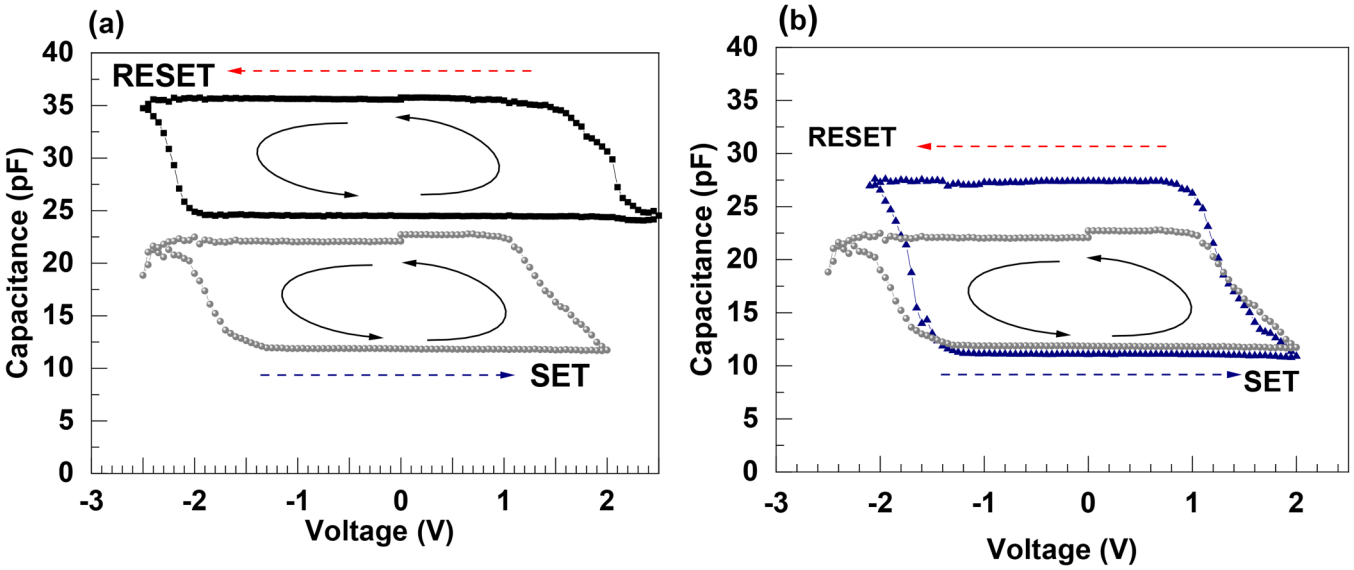

FIG. 9. Capacitance memory maps for (a) Al/Si/TiN/ZrO_2/ZrO_2/Ti (circles) vs Al/Si/TiN/ZrO_2/graphene/ZrO_2/Ti (squares) structures, and (b) Al/Si/TiN/ZrO_2/ZrO_2/Ti (circles) vs Al/Si/TiN/ZrO_2/Al_2O_3/ZrO_2/Ti (triangles). The measurements were made at 500 kHz.

switched at higher capacitance values [Fig. 9(a)]. Comparison of Al/Si/TiN/ZrO_2/Ti, Al/Si/TiN/ZrO_2/Al_2O_3/ZrO_2/Ti, and Al/Si/TiN/ZrO_2/ZrO_2/Ti stack structures demonstrated that the application of the Al_2O_3 interface layer somewhat promoted the widening of the switching memory window in capacitance maps [Fig. 9(b)]. This can, partially, be related to the effect of Al_2O_3 on graphene as well as between ZrO_2 layers (Fig. 4 and Table I), as also mentioned earlier in the literature.[56] Devices with Al_2O_3 could be switched to higher resistance (in HRS) than devices without the interface Al_2O_3 layer, while in LRS, the resistances remained similar, as derived from capacitance memory maps.

The changes in symmetry and operating currents possibly caused by graphene could be harnessed for adjusting RS parameters.

IV. SUMMARY AND CONCLUSIONS

Two different atomic layer deposition-assisted approaches for the preparation of ZrO_2-based films on chemical vapor deposited single layer graphene were comparatively studied. Morphology and Raman shift measurements revealed that the deposition of a ZrO_2 film on graphene did not affect the quality of graphene, whereas in the case of an Al_2O_3 interfacial layer deposited on graphene prior to the growth of ZrO_2, the possible doping effect on graphene was more pronounced and the nucleation of ZrO_2 somewhat enhanced. ZrO_2 consisted of cubic and/or tetragonal phases, whereas Al_2O_3 remained amorphous. The estimated crystallite size in the ZrO_2 films on graphene varied in the range from 7.5 to 8.5 nm, and the film was the most homogeneous when ZrO_2 was grown on the Al_2O_3 interface layer. The electrical measurements demonstrated that the application of graphene embedded between ZrO_2 layers enabled lowering the resistances in resistive switching states and widened the ratio between low and high resistance states. Due to the graphene interlayer, higher but more symmetric operation (programming) voltages had to be applied before the switching events could occur. It is suggested that graphene can be used to modify parameters of resistive switching and, possibly, even multilevel resistive switching could be introduced to the switching medium, considering two-step formation voltages alternatively to the conventional one-step switching process.

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