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Single and complex devices on three topological configurations of HfO_2 based RRAM

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***Abstract*—Three topologies of TiN/Ti/HfO₂/W resistive switching memories (RRAM) are proposed in this work: crossbar, isolated and isolated-crossbar configurations. All configurations use the same sequence of technological processes. The different topologies are obtained by customizing the layouts corresponding to the bottom electrode (W), and the silicon oxide layer that is deposited on the bottom electrode. A comparative study of the resistive switching mechanisms in the three configurations has been carried out. DC current-voltage cycles and small signal conductance memory maps of single RRAM show relevant differences among the three topologies. Complex structures containing various devices (series, anti-series, parallel, anti-parallel) have also been fabricated. Switching loops and memory maps obtained for these complex structures demonstrate that they are fully operative, validating the technological route to manufacture complete RRAM memory chips.**

***Index Terms*—Resistive switching memory (RRAM), crossbar cell, isolated cells, memory maps.**

I. Introduction

Nowadays, nonvolatile memories are mainly based on flash technology. However, the race to miniaturization demands devices with higher performance, lower operating voltages and lower consumption that exceed the physical and technological limits of flash drives. Resistive random-access memories (RRAM) are one of the leading candidates that meets the requirements of non-volatile memories. An individual RRAM cell consists in a metal-insulator-metal structure, which allows for miniaturization, low power consumption and compatibility with CMOS technology. In addition, RRAM cells typically exhibit multilevel behavior. Because of that, there is a great and growing interest in the study of RRAM memories for digital storage, but also for other fields such as analog computing, artificial intelligence, deep learning and neuromorphic computing [1-3]. In these devices, a conductive filament (CF) formed between a top electrode and a bottom electrode by reversible dielectric breakdown (set operation) results in the low resistance state (LRS). A high resistance state (HRS) is obtained in the reset operation, when the conductive filament is ruptured.

Hafnium oxide is one of the dielectrics most widely studied to fabricate this kind of devices. The resistive switching in HfOx is attributed to the movement of oxygen vacancies in the dielectric film, which leads to a valence change in the Hf cations and in the local conductivity [3-5]. Oxygen-deficient conductive filaments are formed during an electroforming process in which oxygen ions are extracted from the film. Once the conductive filament is formed the device is at the low resistance or ON state (LRS). The high-resistance or OFF state (HRS) is achieved by an oxidation reaction in which oxygen vacancies are partially removed from the filaments by injecting oxygen atoms into the oxide. Subsequently, the ON state can be recovered by a new oxidation reaction in which oxygen vacancies are moved into the filament, that is, by extracting oxygen atoms from the filament.

Despite the many advances that have been made in the study of RRAM memories, there are still many topics to be solved or optimized including materials selection, manufacture, integration, and other function beyond the data storage [6]. In this work, we focus on manufacture and integration. We investigate three different topological configurations (crossbar, isolated and mixed isolated crossbar) to determine which of them provides the best resistive switching capabilities.

II. Experiment Section

TiN/Ti/HfO_2/W MIM devices were fabricated on 100mm Si wafers. Initially, a 500nm SiO_2 layer was grown by thermal oxidation to isolate the MIM devices from the Si wafer. The bottom electrode consists of a 200 nm W layer, and the top electrode consists of a 200 nm TiN layer and a 10 nm Ti layer. Metal electrodes were deposited by magnetron sputtering. The bottom electrode structures were defined by photolithography and wet etching. The top electrode structures were made by a lift-off process. The 10nm-15nm HfO_2 insulating film was deposited by Atomic Layer Deposition (ALD) at 225°C using

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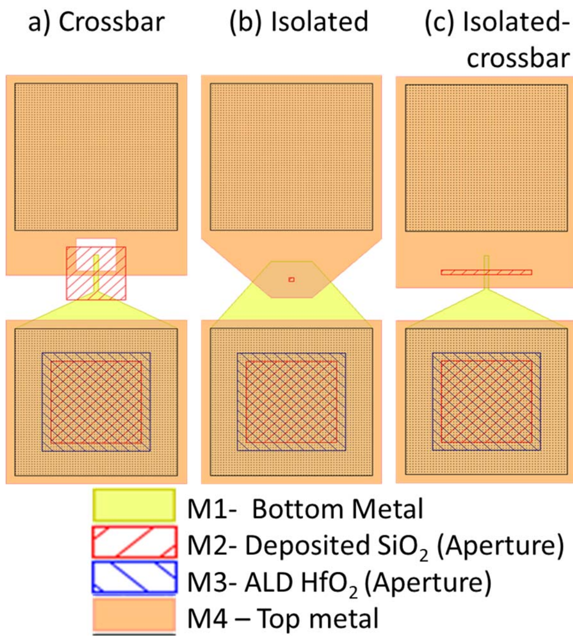

Fig. 1. Layouts of three devices with an MIM structure of 2.5 x 2.5µm^2 obtained by the three types of configuration.

TDMAH and H_2O as precursors and N_2 as carrier and purge gas. Subsequently, this film was opened at the contact areas to the bottom electrode by photolithography and dry etching. For the isolated and isolated-crossbar configurations, previously to the ALD process, a 100 nm-thick SiO_2 layer was deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD) using SiH_4 as precursor over the bottom electrode structures. This isolating layer was opened by photolithography and dry etching at the contact areas to the bottom electrode and at the active areas of the MIM structures. So, depending on the configuration, the MIM cell area is defined by: the width of the top and bottom crossing bars (crossbar configuration), the area of the etched aperture in the deposited SiO_2 layer (isolated configuration) and the width of the bottom electrode bar and the width of the etched bar-like aperture in the deposited SiO_2 layer (isolated-crossbar configuration).

A variety of simple and complex structure devices have been fabricated with the three topologies including unitary cell, two cells in series and anti-series configuration, two cells in parallel and anti-parallel configuration, bridges of four individual cells, radial configuration of 12 devices with a common terminal (bottom electrode) and array of 6x6 individual devices in which all the devices in each row share the top electrode and all the devices in each column share the bottom electrode.

The layouts of single MIM structures for the three configurations are depicted in Fig.1. The main difference among the three configurations is the existence or not of the deposited SiO_2 and bottom electrode layers in the region surrounding the active device. In the crossbar configuration both layers have been completely removed in the region around the device. In contrast, in the isolated configuration both layers are kept. Finally, in the isolated-crossbar configuration the bottom electrode is removed as in the crossbar configuration and the deposited SiO_2 is removed in one direction but not in the perpendicular one. As a result, staggered structures such as those seen in Figure 2 are formed. In the case of crossbar configuration, the active device is shaped like a plateau, while in the isolated configuration they are valley-like shaped. A mixed of both appears for isolated-crossbar configuration.

Electrical measurements were carried out putting the samples in a light-tight, electrically shielded box. DC-current

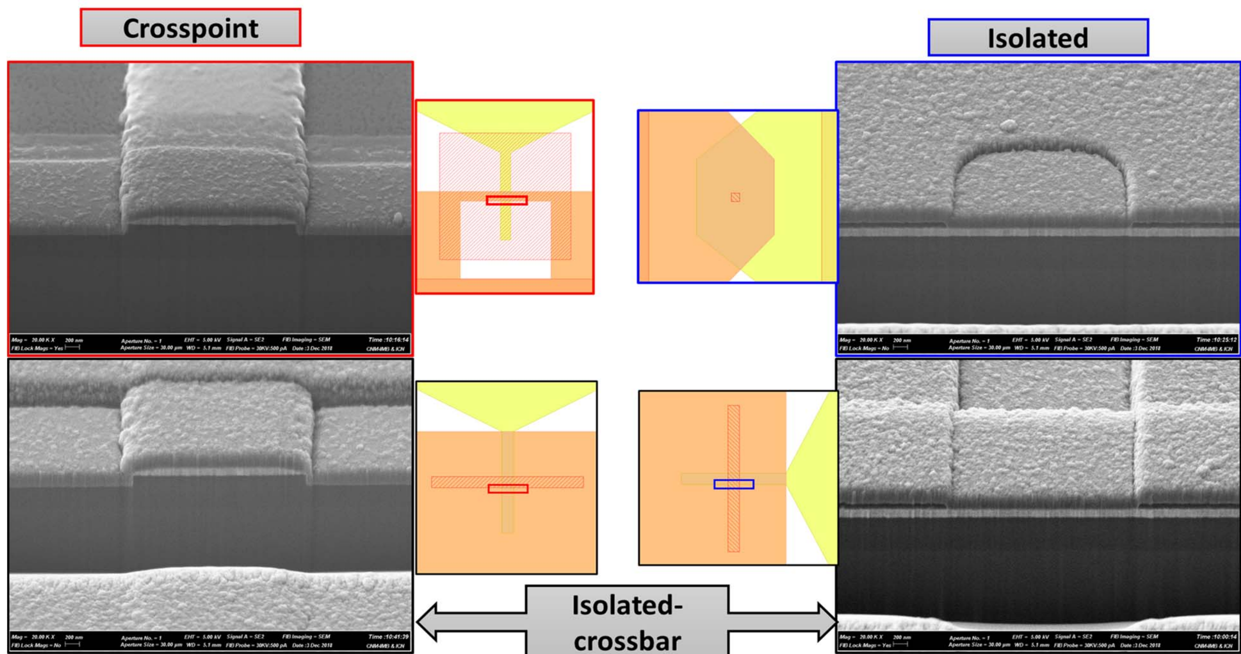

Fig. 2. SEM inspection of three devices with an MIM structure of 2.5 x 2.5µm^2 obtained by the three types of configuration. In spite of the surface roughness in both top/bottom electrodes is quite large, it does not influence the resistive switching properties.

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and admittance were measured using a Keithley 4200SCS semiconductor analyzer. The voltage was applied to the TiN/Ti top electrode with the W bottom electrode grounded. The small signal admittance parameters were measured by adding a 500 kHz small signal of 30 mV r.m.s. to the d.c. bias voltage. A parallel admittance model was selected which directly provides the real component value of the admittance (conductance, G) and the imaginary one (susceptance, B).

III. RESULTS AND DISCUSSION

Fig. 3 shows the voltage-current loops for single cells of the three configurations. The isolated configuration shows higher current values at both the high-resistance state (RESET) and low resistance state (SET). Crossbar and isolated-crossbar configurations show similar values at both states. Moreover, in the crossbar technology (Fig. 3(c)) both transitions SET to RESET and RESET to SET are more abrupt than in the other configurations. The softer drop from SET to RESET occurs for the isolated-crossbar configuration. The more abrupt the transitions, the more difficult it is to get intermediate states. Therefore, the isolated-crossbar methodology is the most favorable for applications requiring the multilevel behavior of RRAM cells (neuromorphic computing, artificial synapses). It is important to mention that we have not limited the maximum current for every SET condition. In the case of RRAM devices were used for memory application, it will be mandatory to use a current compliance which limit the SET current to lower levels so reducing the power consumption.

In previous works, we introduced the concept of admittance memory maps [7] which provide information about the state of a RRAM memory. To obtain the memory maps we apply a return-to-zero voltage pulse sequence as follows: with the sample at the HRS state, we apply a positive voltage pulse during 1 ms, and then the voltage returns to zero. At this moment we measure the admittance at 0 volts (G, B). The pulse amplitude (V) is linearly increased until the SET transition occurs. Once the sample is at the LRS state, V is linearly decreased to negative values. When V reaches negative values enough to take the device back to the HRS state (reset), it is linearly increased again until 0 V. The plots of G and B/ω as a function of the programming voltage, V, previously applied constitute the memory maps. Conductance memory maps for isolated-crossbar and crossbar single cells are plotted in Figure 4. These maps confirm that transitions to SET and RESET states are more abrupt in the case of crossbar than in the mixed one, and that intermediate states can be more easily achieved and controlled with the last one.

Complex devices consisting of several cells connected together were also fabricated in the same chip. One example of two cells in anti-series configuration is shown in Fig. 5, in which the two devices share the top electrode pad (TC) and the voltage is applied to the bottom electrode pads (BC1 and BC2). I-V switching curves (Fig. 5(a)) exhibit the complementary resistive switching (CRS) behavior expected for this configuration. The memory maps consisting in the current of the structure measured at 0.1 V after applying a voltage V are depicted in Fig. 5(b). The CRS behavior is here even more clearly observed than in IV loops of Fig. 5(a).

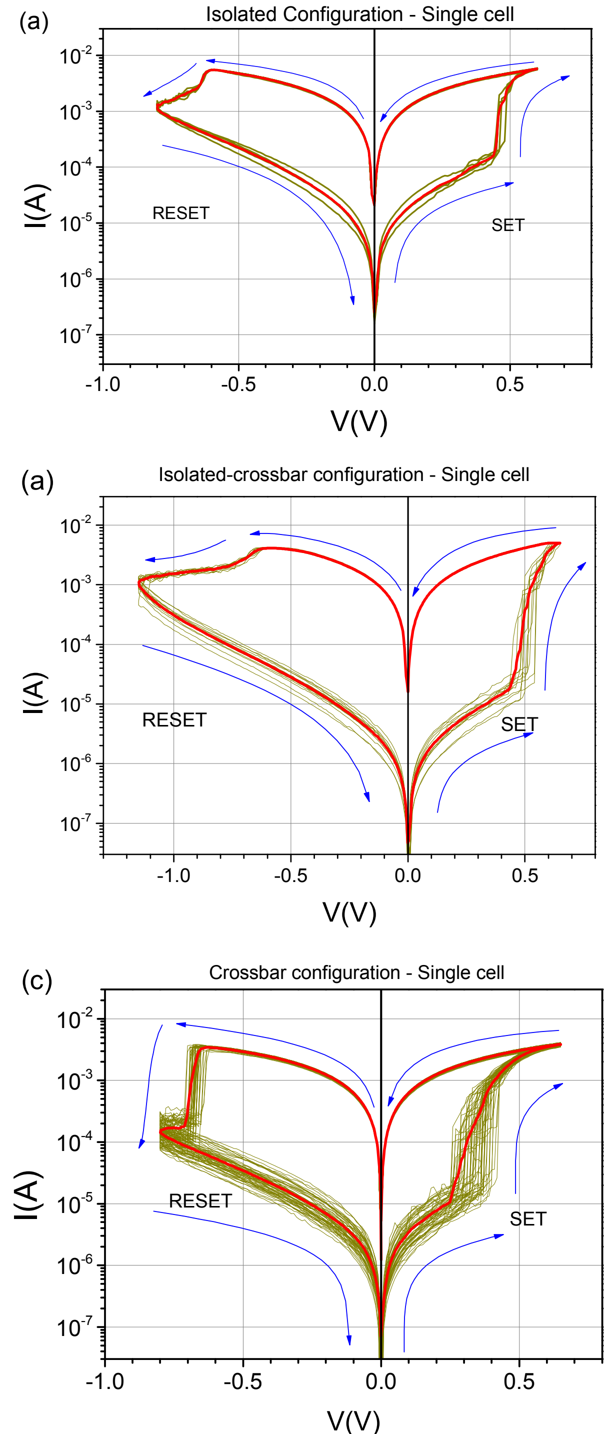

Fig. 3. Current-voltage resistive switching loops of single 2.5 x 2.5µm² MIM structures for the three types of configuration obtained with voltage sweeping rates of 50mV/s.

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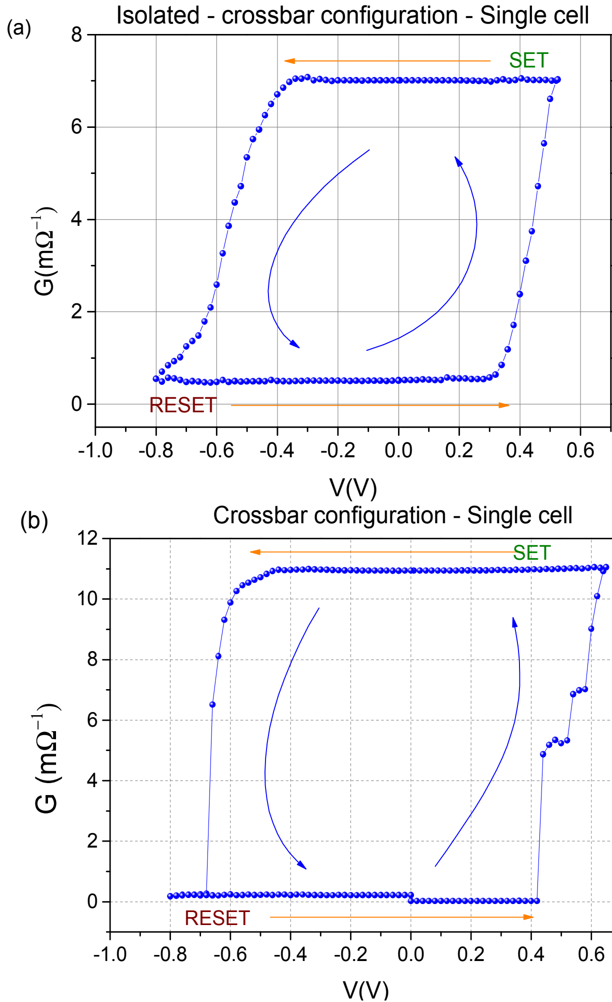

Fig. 4. Conductance memory maps for single devices obtained by insolated-crossbar (a) and crossbar (b) configurations.

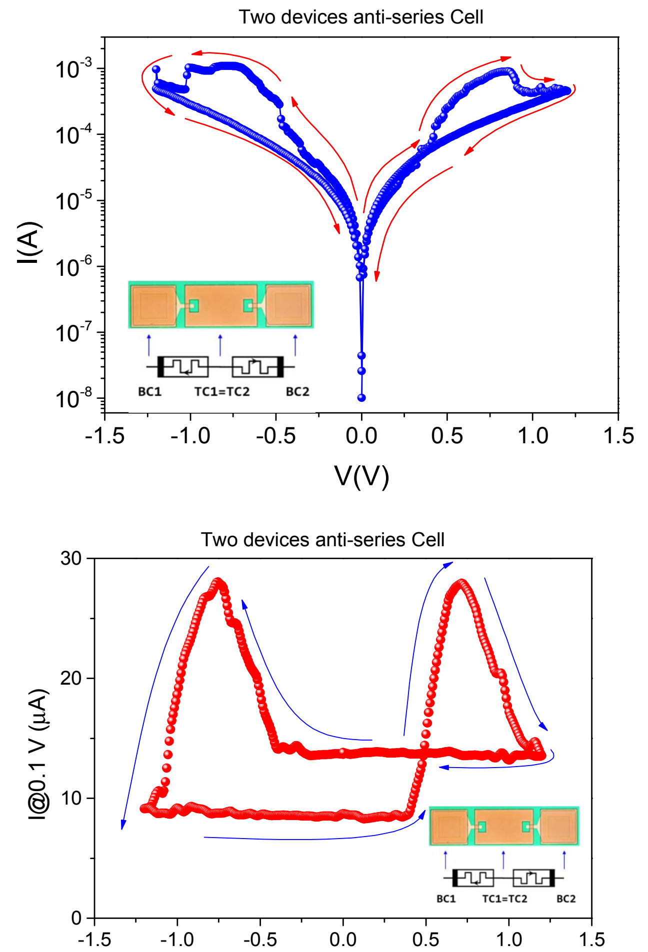

Fig. 5. Current-voltage loop (a) and current memory map (b) obtained for a two-devices series cell obtained by insulated-crossbar configuration

IV. Conclusions

Three topologies of HfO_2 resistive switching memories (RRAM) have been designed and fabricated: crossbar, isolated and isolated-crossbar. I-V and memory maps obtained for single MIM devices indicate that the isolated configuration shows higher current values at both RESET and SET states, whereas crossbar and isolated-crossbar configurations show similar levels at both states. The transitions between the two states are more abrupt in the crossbar technology case, whereas they are smoother for isolated and isolated-crossbar devices. Intermediate states can be more easily achieved and controlled in isolated-crossbar cells. Consequently, the isolated-crossbar methodology appears as the most favorable for multilevel applications such as neuromorphic computing or artificial synapses. Complex devices fabricated with these configurations prove to be fully operative, warranting that high functionality can be achieved.

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