Memory Maps: Reading RRAM Devices Without Power Consumption

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A comparative study of MIM-RRAM structures with different insulator materials is presented. Admittance memory mapping was carried out at 0 V dc bias, revealing two clearly separated states, both in terms of conductance and susceptance. The memory in the ON state can be modeled by means of a two parameter (resistance and inductance) equivalent circuit. The parameter extraction provides memory maps for the resistance and the inductance as well. The transition shapes between the ON an OFF state are different for each structure due to specific physical mechanisms.

Introduction

According to the 2014 International Technology Roadmap for Semiconductors (ITRS), resistive switching memories (RRAM) are good candidates for the next generation nonvolatile memories. Their main properties are fast switching speed, good reliability, low power consumption and CMOS technology compatibility [1, 2], as well as potential scalability beyond NAND flash [3, 4]. They are based on the change in the physical properties of a conductive filament by applying an electric field across a metal-insulator-metal (MIM) or metal-insulator-semiconductor (MIS) structure. A set switching forms and closes the filament, and induces a transition from the high-resistance state (HRS) to the low-resistance state (LRS). A reset switching disrupts the filament and induces the opposite transition. The resistance switching is generally caused by the diffusion of oxygen vacancies, charge carrier trapping and detrapping, and Schottky barrier modulation to produce the memory effect [5]. The implementation of RRAM memory devices in the industry requires a detailed understanding of switching mechanisms, hence significant improvement in the knowledge limits is still needed. To expand the conventional characterization techniques spectrum of RRAM devices, we propose to study the small-signal parameters, namely, conductance (G) and susceptance (B) [6, 7]. Both G and B memory maps provide complementary information about the physical nature of the switching mechanisms. Moreover, reading of the memory state is carried out without dc power consumption. Here we present comparative results of MIM-RRAM with different insulator materials. Stacks or doped dielectrics are used in order to increase the defect densities and enhance the resistive switching phenomena.

Experimental

The film growth process was carried out in a in-house built low-pressure flow-type atomic-layer-deposition (ALD) reactor [8]. The dielectric film compositions and thicknesses of the samples under study are listed in Table I. Pt/Ta_2O_5-TiO_2-Ta_2O_5/RuO_2/TiN/Si MIM samples were obtained by depositing the films on 15 nm-RuO_2/10 nm-TiN/Si at the substrate temperature of 350 ºC. Oxide films were 5 nm thick stacks formed as Ta_2O_5-TiO_2-Ta_2O_5 triple layers. Metal chloride precursors, $TiCl_4$ and $TaCl_5$, were used to grow TiO_2 and Ta_2O_5, respectively. Zirconium and cobalt based samples were made on TiN/Si substrates at 300 ºC, with Pt as top electrode, using $ZrCl_4$ and $Co(acac)_3$ [acac = tris(2,4-pentanedionato)cobalt] as the metal precursors. Two kinds of layers were made: cobalt oxide-doped zirconium oxide (ZrO_2:Co_3O_4) and nanolaminate (ZrO_2-Co_3O_4). In all cases O_3 was used as oxygen precursor and N_2 as purge gas.

Admittance parameters were recorded by using a Keithley 4200SCS semiconductor analyzer. The bias voltage was applied to the top electrode with the bottom electrode grounded. A 30 mV rms-ac signal was superimposed to voltage bias. A parallel admittance model which provides G and B values was selected to perform the characterization. To obtain the memory maps we apply a return-to-zero voltage pulse sequence as follows: with the sample at the HRS state, we apply a positive voltage pulse during 1 ms, and then the voltage returns to zero. At this moment we measure the admittance at 0 volts (G_0, B_0). The pulse amplitude (V_P) is linearly increased until the HRS to LRS state transition (set) occurs. Once the sample is at the LRS state, V_P is linearly decreased to negative values. When V_P reaches negative values enough to take the device back to the HRS state (reset), it is linearly increased again until 0 V. The plots of G_0 and B_0/ω as a function of the programming voltage, V_P, previously applied constitute the memory maps.

TABLE I. List of the dielectric films studied in this work.

Sample	Dielectric film composition	t, nm
Ta-Ti-Ta	Ta_2O_5-TiO_2-Ta_2O_5	5
ZC	ZrO_2:Co_3O_4	4.5
Z-C	ZrO_2-Co_3O_4	14 - 12

Results and Discussion

In Figs. 1-3 we show the results obtained at 100 kHz for Pt/Ta_2O_5-TiO_2-Ta_2O_5/Ru/TiN, Pt/ZrO_2:Co_3O_4/TiN/Si/Al, and Pt/ZrO_2-Co_3O_4/TiN/Si/Al MIM samples. I Very similar results are obtained in the whole experimental frequency range, 20 kHz – 1 MHz. In all cases, we observe that G_0 and B_0 are very stable in a wide V_P range, so indicating that the conductive filaments are also very stable at both states. Reset and set transitions are very sharp, being reset more vertically than set. That is, the filament restoring is in some extent a gradual process, whereas its dilution is instantaneously broken.

In the case of MIM structures with inert noble metal electrodes, the change of the resistance has been related to the migration of oxygen anions, usually described by the motion of the corresponding oxygen vacancies [9]. A positive voltage on the top electrode attracts to the oxygen cations, so the filament is formed by oxygen vacancies accumulation between top and bottom electrode, and the set process is produced. A negative voltage pushes the oxygen cations back into the dielectric, and the filament dilution takes place (reset process). The results of Ta_2O_5-TiO_2-Ta_2O_5-based samples (Fig.1) as well as those of

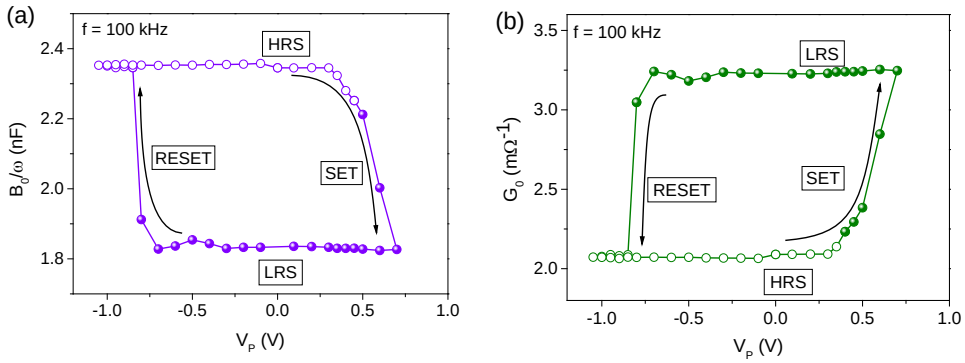

Figure 1. Admittance memory maps for a Ta-Ti-Ta MIM RRAM.

ZrO_2-Co_3O_4-based samples (Fig.3) are consistent with this mechanism. In fact, set is produced at positive voltages, and reset at negative voltages. Remarkably, in Fig. 3 a two-steps set process is clearly seen, which might be related to the fact that two relatively thick layers (14 and 12 nm, respectively) of very different materials (ZrO_2 and Co_3O_4) are stacked. It seems that the conductive filaments in each layer are likely not formed simultaneously. In the case of Ta_2O_5-TiO_2-Ta_2O_5-based samples, there are three much more thin layers of more similar materials in terms of possible oxygen deficiency and stoichiometry deviations. As it is seen in Fig. 1, in this case the one-step set process seems to be a unique process produced at the same time through the three layers.

Regarding the ZrO_2:Co_3O_4 sample, its behavior is different from that of the stacked sample. We can see in Fig. 2 that the one-step set occurs at negative polarity, whereas the reset takes place for positive voltages. It could be explained as follows: the filament would be produced by means of an electrochemical migration mechanism, in which negative charged cobalt ions would be driven to the positively biased bottom electrode, forming a metallic path. The free enthalpy value of cobalt oxide is much lower than the zirconium oxide one, so this hypothesis is plausible.

According to a recently proposed model [6, 10], the conductive filament behaves as an inductance (L_0) in series with a resistive term (R_0), and both are in parallel with the capacitance of the MIM structure (C). Using this equivalent circuit, we have extracted L_0 and R_0 (as an illustration, see Fig. 4 for Pt/Ta_2O_5-TiO_2-Ta_2O_5/Ru/TiN sample). Again the signals, and hence the filaments, are very stable in both states, with abrupt set and reset transitions. The inductive term is negligible in the HRS, and reaches high values (50 µH)

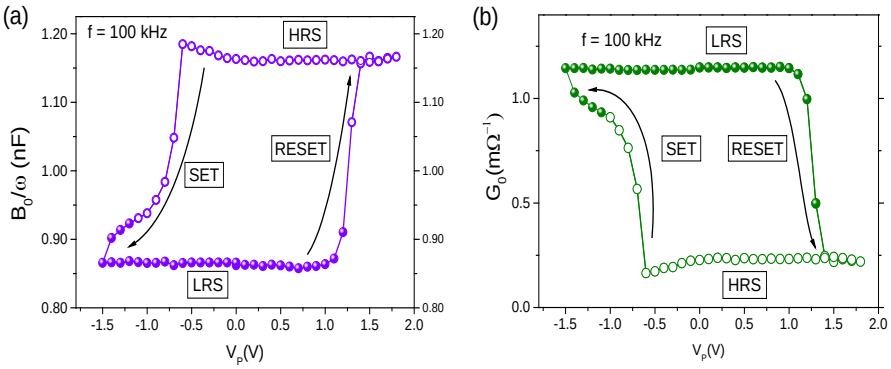

Figure 2. Admittance memory maps for a ZC MIM RRAM.

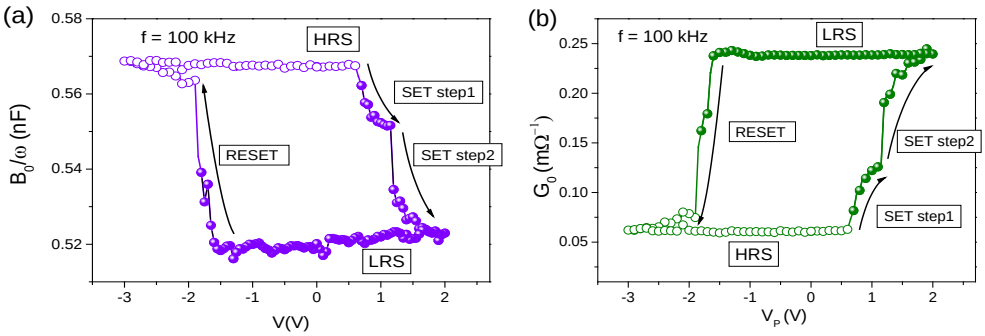

Figure 3. Admittance memory maps for a Z-C MIM RRAM.

when the filament is formed. This indicates the existence of delays between the current and voltage caused by charge transport mechanisms occurring at the filaments.

Conclusions

Excellent resistive switching behavior has been demonstrated in Pt/Ta_2O_5-TiO_2-Ta_2O_5/Ru/TiN, Pt/ZrO_2:Co_3O_4/TiN/Si/Al, and Pt/ZrO_2- Co_3O_4/TiN/Si/Al MIM structures. Admittance memory maps show two clearly different states, which would allow one to use them as non-volatile memories. The transitions between the two states (set and reset process) provide relevant information about the underlying physical dynamics. In the stacked-dielectric layers the conductive filaments are formed by oxygen vacancies accumulation between top and bottom electrodes. In the cases of two thicker layers stacked as nanolaminates the set process proceeds in two steps. On the other hand, when the dielectric is a Co_3O_4-doped ZrO_2 layer, the conductive filaments can be due to the accumulation of metallic ions forming a path connecting the electrodes. Sensing of memory state may be carried out at 0 V bias, hence without dc power consumption.

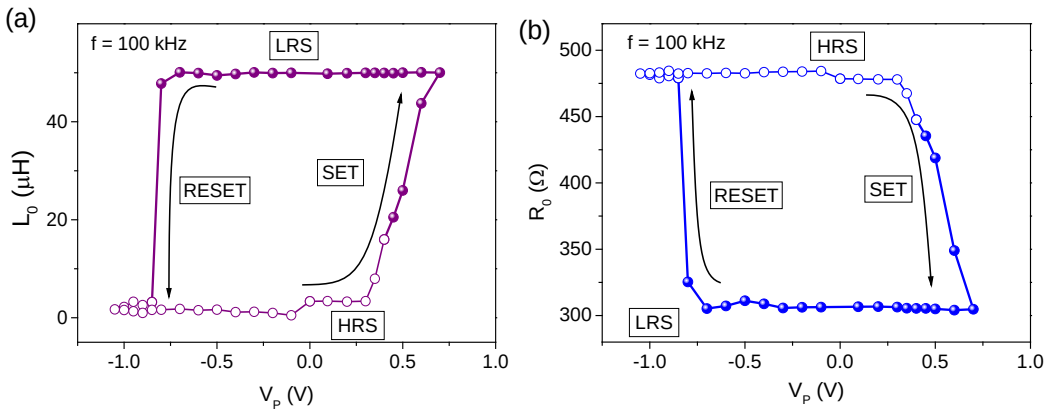

Figure 4. Inductance (a) and Resistance (b) of conductive filaments extracted from the admittance memory map of Fig.1 for a Ta-Ti-Ta MIM RRAM. These parameters were obtained according the model described in Ref. 7.

Acknowledgments

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