Control of the set and reset voltage polarity in anti-series and anti-parallel resistive switching structures

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Abstract

In the attempt to control the polarity of the set and reset voltages in bipolar resistive switching capacitors, we have studied the switching properties of structures consisting of either two anti-series or two anti-parallel metal-insulator-metal capacitors. The capacitors were based on hafnium oxide, and W and TiN/Ti were used as bottom and top electrodes respectively. MIM capacitors showed bipolar resistive switching behavior, with very good repetitiveness and endurance properties. Both anti-series and anti-parallel structures showed again bipolar resistive switching behavior, being the polarity of the set and reset voltages controllable by applying higher biases. In the case of anti-series configuration, there is a stretch-out in the current-voltage characteristic because the bias is applied across two different structures. Changing the polarity is equivalent to the process of write and erase of complementary resistive switching devices in crossbar arrays. In the case of anti-parallel configuration, the resistance window between both resistivity states is reduced. The control of the switching polarity has also been observed when applying an small ac signal, and measuring the conductance of the structures.

INTRODUCTION

Although the resistive switching phenomena (RS) was reported in 1962 [1], it has recently been getting a wide interest due to its potential wide range of applications, such as non-volatile memories [2-3], neuromorphic computing and artificial synapses [4-6], and analogue signal processing [7]. Resistive random access memories (RRAMs) devices consist of an insulating layer interposed between two metal electrodes, and their behavior is characterized by the capability of exhibiting memory when operating as a two terminal variable resistor, since they exhibit resistive switching behavior. Both metal-insulator-metal (MIM) and metal-insulator-semiconductor (MIS) structures can be employed. In these devices, a conductive filament (CF) can be formed between top and bottom electrodes by reversible dielectric breakdown (set operation), resulting in the low resistance state (LRS). The reset operation dissolves the conductive filament resulting in a high resistance state (HRS). The set and reset operations can be obtained by applying a voltage with the same polarity (unipolar RRAM devices) or with opposite polarities (bipolar RRAM devices).

When using the RRAM devices in passive crossbar arrays, there exists a problem when reading specific memory positions due to the sneak path currents, undesired current paths parallel to the desired path due to cells in the LRS state [8]. Sneak path current is one of the major problems regarding passive crossbar arrays. Rectifying elements such as diodes have been studied to solve the sneak paths problem [9]. The concept of complementary resistive switching (CRS) has attracted interest since it would prevent the use of external diodes in the memory cell [10]. CRS consists of two RRAM devices in anti-serial configuration that share a common electrode. The CRS are designed in a way one device is always in the HRS at low voltages, so it can suppress the sneak currents. When enough high voltage is applied, both cells are in the LRS state in order to read the cell [11]. However, this configuration has also been employed for some other purposes: $Ta/Ta_2O_5/Pt/Ta_2O_5/Ta$ CRS cells have been use for the implementation of boolean logic functions [12-13], and other structures based on HfO_x/TaO_x dielectrics were used to implement the Max and Min basic functions of the fuzzy logic [14].

In this work, we used the concept of complementary switching device in order to create a RS structure in which we are be able to select the set and reset polarities. This means we can change the polarity of the switching structure when advantageous. In fact, this behaviour can be achieved not only with CRS structures; it can also be obtained with two RRAM devices in anti-parallel configuration, although a different performance has been obtained, as shown in this work. This kind of performance could be interesting not only in non-volatile memory applications but also in neuromorphic computing applications. In this kind of application, multilevel RS device are used [15] since different synaptic weights must be simulated [4]. Again, the polarity of the write or erase pulses can be modified during the operation. We have carried out the experiment using MIM capacitors based on hafnium oxide (HfO_2) as switching devices, connected in two different configurations: anti-series and anti-parallel configuration, as shown in Figure 1. Not only we have checked the dc current-voltage (I-V) properties, but also we have studied the behavior when applying an ac signal to the structure.

EXPERIMENTAL

The devices used in this work are TiN/Ti/10-nm HfO_2/W MIM capacitors. The high-k dielectric was deposited by the atomic layer deposition (ALD) technique at 225 ºC using TDMAH and water as hafnium and oxygen precursors respectively. Nitrogen was used as carrier and purge gas. The bottom electrode consists of a 200 nm W layer, and the top electrode consists of a 200 nm TiN layer and a 10 nm Ti layer.

Metal electrodes were deposited by magnetron sputtering. The resulting structures used are square cells of $15\times15\ \mu m^2$.

The electrical measurements were carried out at room temperature using an HP 4155B semiconductor parameter analyzer for the current-voltage (I-V) measurements, and a Keithley 4200SCS semiconductor analyzer for the conductance-voltage (G-V) measurements.

RESULTS

The resistive switching mechanism in our RRAM devices was studied in a previous work [16], and was found to be valence change memory effect (VCM). The conductive path of the switching layer is formed due to oxygen ion migration and formation of conductive filaments made of oxygen vacancies [17]. These devices need an initial electroforming process in order to form the conductive filaments. Figure 2 shows the initial electroforming step (red color). In the beginning, the leakage current is below 1 pA. The CFs are formed at a voltage of about 2.8 V, and a current compliance of 100 μA was used during the electroforming process to prevent irreversible oxide breakdown. Several RS cycles were measured after the electroforming process, which are also displayed in Figure 2. Bipolar switching is obtained in these structures: LRS is obtained when applying positive voltages to the top electrode, and HRS is obtained when applying negative voltages. We can observe a very good repetitiveness.

In order to carry out the experiment, we need reliable devices. The endurance performance of the RRAM capacitors has been found to depend on the metal gate, but HfO_2/Ti stacks have demonstrated > 10^{10} endurance cycles [18]. To prove the endurance performance of our devices, we have applied voltage pulses cycles, as shown in Figure 3(a): +1 V pulses are applied to set the device into LRS, and -1.5 V pulses are applied to set the device into HRS. The state is read 5 ms after the set or reset pulses by applying -0.2 V pulses. The set, reset and read voltage pulses length is the minimum length available by our measurement equipment. Figure 3(b) shows the resistance measured at V_{READ} = -0.2 V. After 15000 measurement cycles, the RRAM device performance has not changed. The HRS/LRS resistance window is > 10× for all the measurements, and the HRS and LRS resistance values variability is very low.

After the good performance of the RRAM devices was checked, we connected two devices in anti-series configuration (CRS configuration), as shown in Figure 1, named device 1 and device 2. The structures were previously electroformed. Figure 4 shows several current-voltage RS cycles. We can observe two different series of results: the red color series show RS behavior expected for device 1, with set and reset voltages at positive and negative voltages respectively. However, the black color series show RS behavior expected for device 2, with set and reset voltages at negative and positive voltages respectively. We found the behavior observed depends on the resistivity state of both devices. In order to study the operation point of both devices, we added a voltage probe at the connection between the two devices. Figure 5 shows one RS cycle: the black line corresponds to the anti-series structure, the red line corresponds to the device 1, and the blue line corresponds to the device 2 of the structure. We have added some numbered points corresponding to the same operation point in order to illustrate the operation. Device 2 inside the anti-series structure remains in the LRS. For low top voltages, and when device 1 is in the HRS, very low current flows through the structure, so the voltage drops entirely across device 1. When device 1 switches to LRS, a higher current density flows through the structure, and the voltage drop across device 2 is now not negligible. An stretch-out in the I-V curve is observed, as we need higher top voltages to switch between HRS and LRS due to voltage drop across the two devices. Due to this stretch-out, the HRS/LRS resistance window slightly decreases. The characteristic represented in Figure 5 corresponds to the red color series in Figure 4. We have to point out that it is not possible to maintain both devices in the HRS: once a device switches to LRS, the voltage drops across the device that stays in the HRS, so this device would switch firstly.

An interesting feature is we are able to change between both series shown in Figure 4 by applying a higher voltage to the structure. This means we are able to select the polarity of the bipolar switching structure. This is shown in Figure 6. Both devices are in the LRS. A top voltage of about 1.5 V drives a voltage drop

across device 2 high enough to reset it. This transition takes place between points named 1 and 2. A redistribution of the voltages that drop across both devices takes place when device 2 resets, and now the voltage mainly drops across device 2 as its resistance value is much higher. At this point, a transition from the red line series to the black line series shown in Figure 4 has been carried out. As expected, the opposite transition would be obtained for high negative voltages (transition from the black to the red line).

It has been demonstrated that the resistive switching behavior also emerges when applying an ac small signal to the devices [19-20], In a previous work, we found conductance multilevels even when applying no dc bias to the sample [21]. We have measured the conductance-voltage (G-V) characteristic at 100 kHz for the anti-series structure, and Figure 7(a) shows the result. Again, we can distinguish two different results, if device 1 is blocked in LRS we observe the black lines, and if device 2 is the one blocked in LRS we observe the red line. The conductance gap between HRS and LRS at 0 V also appears in the anti-series structure. Figure 7(b) shows the process of changing from red to black series: when high enough voltage is applied to the top electrode, it can drive device 2 to the HRS. In fact, the feature that allows the transition between both series is similar to the process of write and erase of complementary resistive switching devices in crossbar arrays [22].

In the next experiment, we connected two devices (device 1 and device 2) in anti-parallel configuration, as shown in Figure 1. The structures were also previously electroformed. Figure 8 shows several current-voltage RS cycles. Again, we can observe two different series of results: the red color series show RS behavior expected for device 1, and the black color series show RS behavior expected for device 2. However, there are two main differences with the results obtained in the anti-series configuration: the set and reset voltages are not increased when connecting both devices, but the HRS/LRS resistance window is strongly reduced. In order to study the state of both devices, we used two current probes to measure the current that flows in both branches. In Figure 9, we have represented one RS cycle: the black line corresponds to the anti-parallel structure, the red line corresponds to the device 1 of the structure, and the blue line corresponds to the device 2. In order to illustrate the operation, some numbered points are displayed, and correspond to the same operation point. Device 1 inside the anti-parallel structure is now the one that remains in LRS, so the total current flowing inside the structure should always be higher than the LRS current. When device 2 is in HRS, the total current flowing is very close to the current flowing across device 1. However, when device 2 switches to LRS, the total current increases. For ideal identical structures, we would obtain an HRS/LRS resistance window $\approx 2\times$. The characteristic represented in Figure 9 corresponds to the black color series in Figure 8.

This configuration shows the same feature as the anti-series configuration: we are able to select the polarity of the switching structure. This has been represented in Figure 10. Device 2 was blocked in LRS. Device 1 can set at a top voltage of about 0.5 V. However, if the top voltage keep on increasing, device 2 can reset, so there has been a transition from the red line series to the black lines series shown in Figure 8. As in the previous configuration, it is not possible to maintain both devices in the HRS, in this case due to the set voltage is lower than the reset voltage, so once a device has been set, the device that stay in the HRS would switch the first.

CONCLUSIONS

In this work, we investigated the possibility of controlling the polarity of bipolar resistive switching structures. We demonstrate the control of the polarity in anti-series and anti-parallel structures based on TiN/Ti/HfO_2/W MIM capacitors. The performance of the MIM resistive switching capacitors was checked before connecting the capacitors to set up the anti-series and anti-parallel structures. In the case of the anti-series connection, we are able to control the polarity of the set and reset voltages by applying higher voltages to the structure. The current-voltage is stretched-out when compared with a single MIM capacitor and the HRS/LRS resistance window slightly decrease due to the top voltage applied to the structure is drop across two different capacitors. The process of changing the polarity of set and reset voltages is similar to the process of write and erase of complementary resistive switching devices in crossbar arrays. In the case of the anti-parallel connection, the polarity of set and reset voltages can also be controlled. However, in this configuration should not be used in memory applications because the HRS/LRS resistance window is strongly reduced due to the current in the structure is always higher than the LRS current, since at least one

of the capacitors is in the LRS. It neither should be used in neuromorphic computing applications because a big resistance window is needed to obtain multilevel devices. Of course, this anti-parallel configuration is not suitable as CRS for crossbar arrays due to the high current that these structures always show. Finally, we also proved the control of the polarity when measuring the ac conductance in these structures, so we still can measure the state of the device even without dc bias applied.

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FIGURES

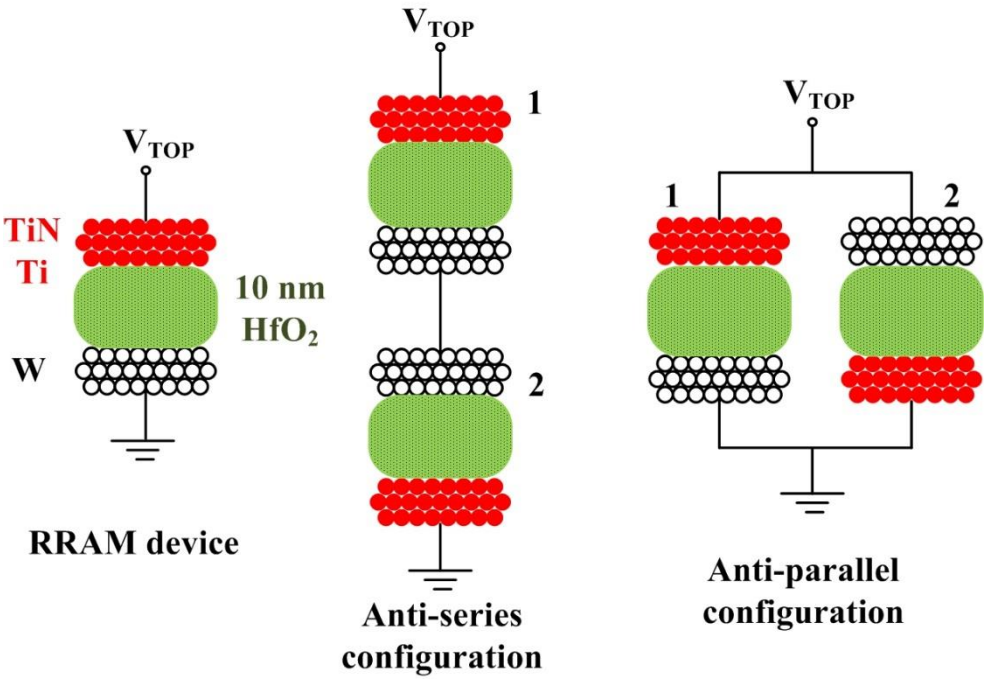


Figure 1: RRAM structures and the anti-series and anti-parallel configurations studied.

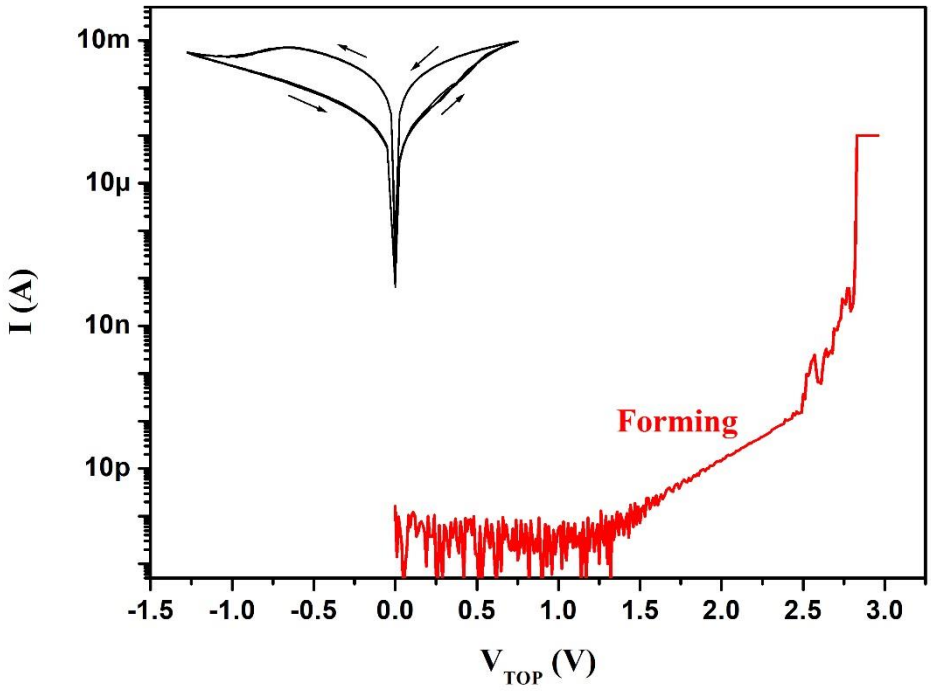
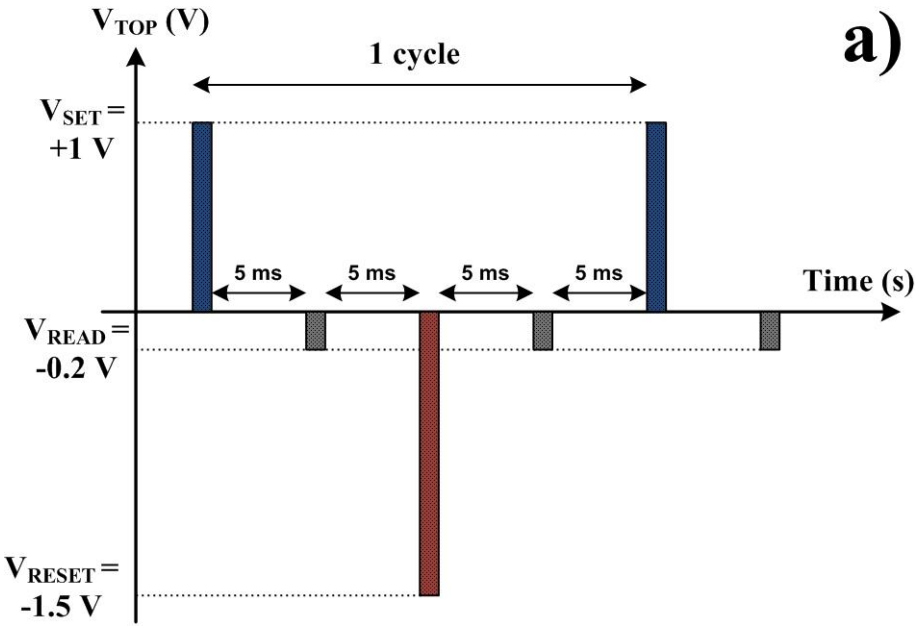


Figure 2: Several I-V resistive switching loops showing set and reset processes, and initial conductive filaments forming.



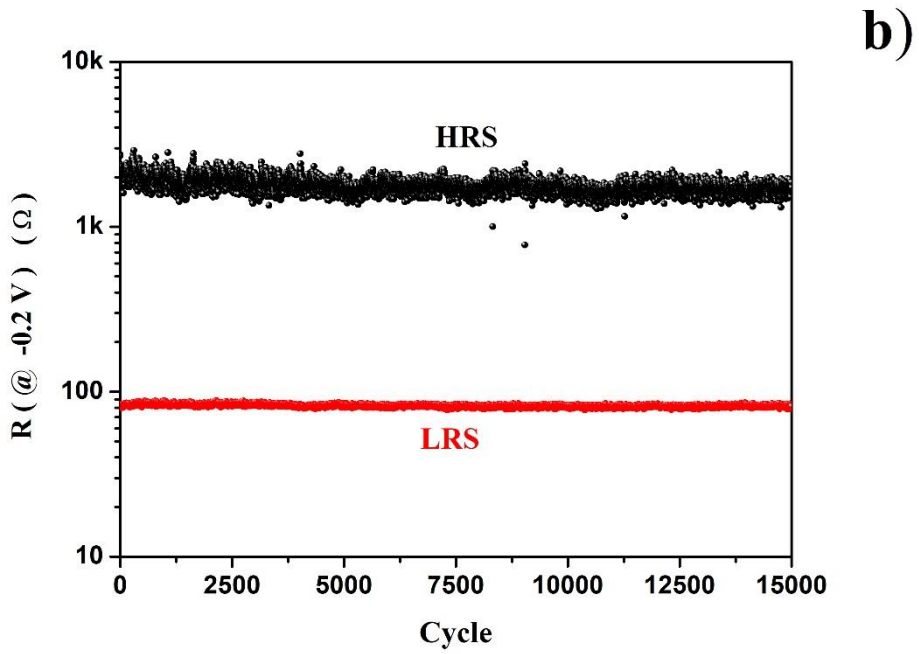


Figure 3: Voltage pulse sequence (a) and resistance values in the HRS and LRS states measured after 15000 cycles (b).

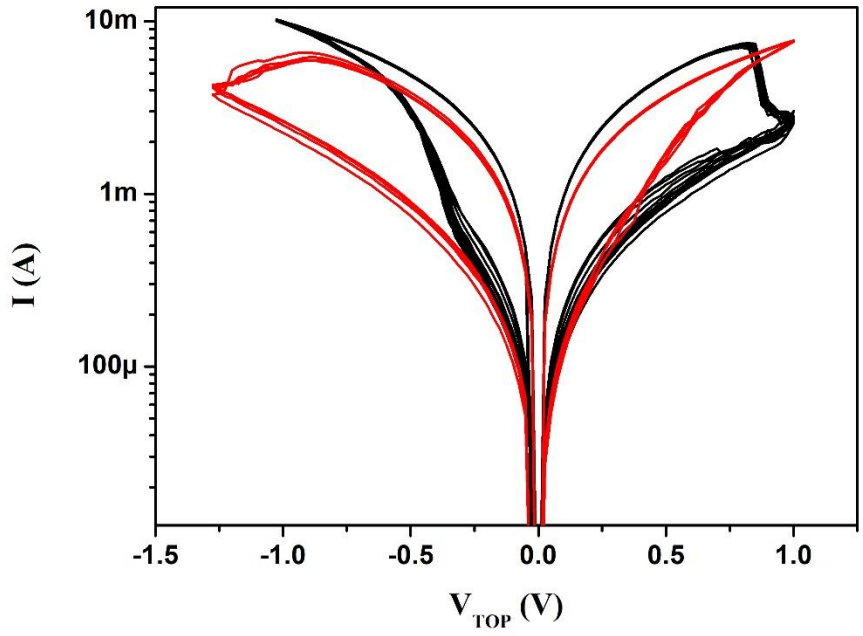


Figure 4: RS cycles measured in the anti-series configuration. Two different results series can be obtained (red and black colors).

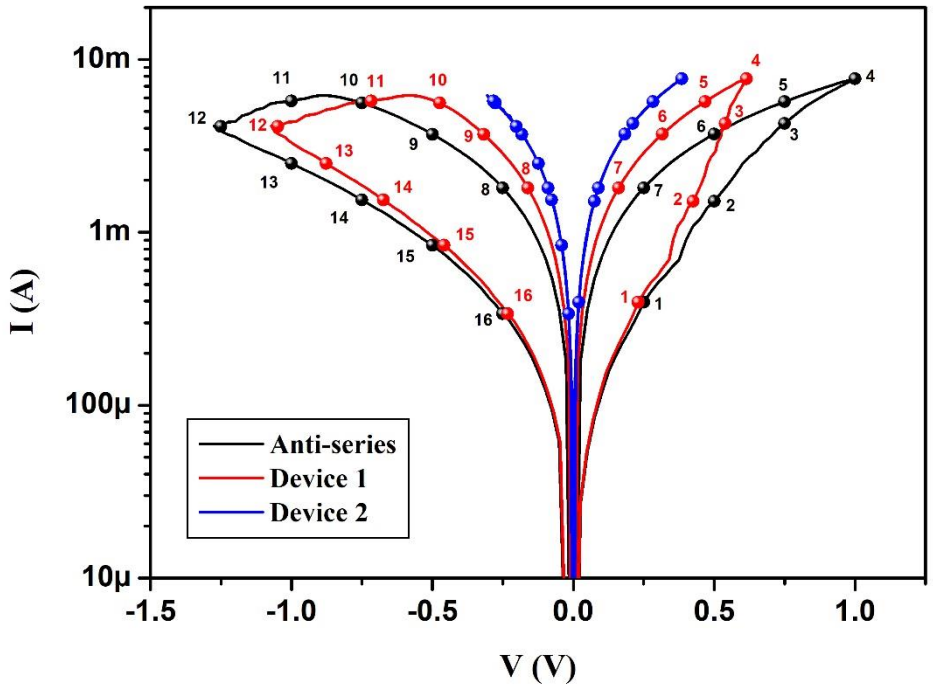


Figure 5: One RS cycle measured in the anti-series configuration. The black line corresponds to the operation of the anti-series structure, the red line corresponds to the operation of device 1, and the blue line corresponds to the operation of device 2.

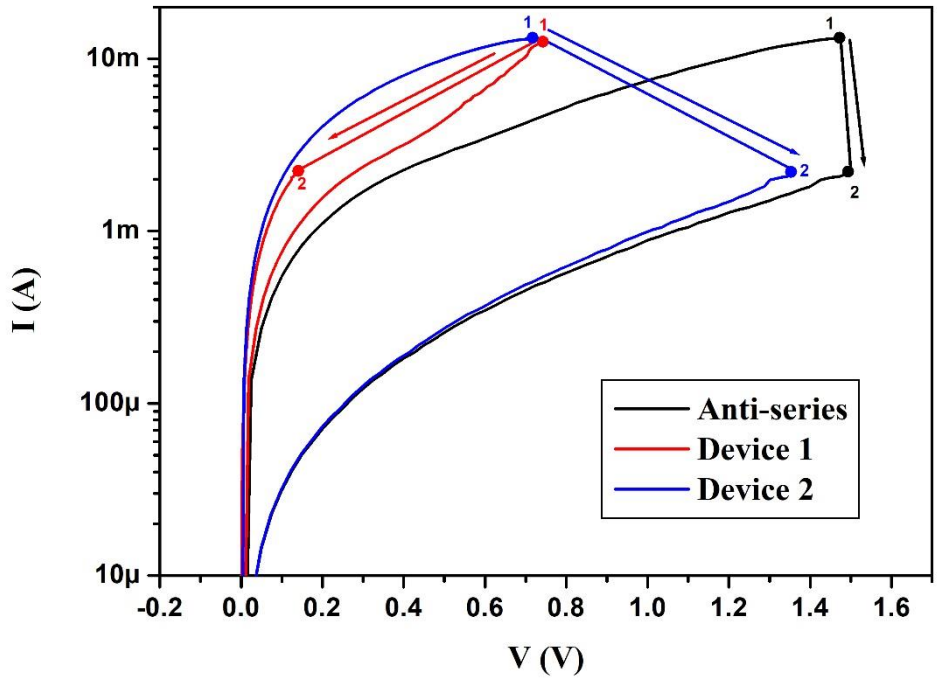


Figure 6: Changing between the two series process. High top electrode voltages are able to reset device 2, and a redistribution of the voltages that drop across both devices takes place.

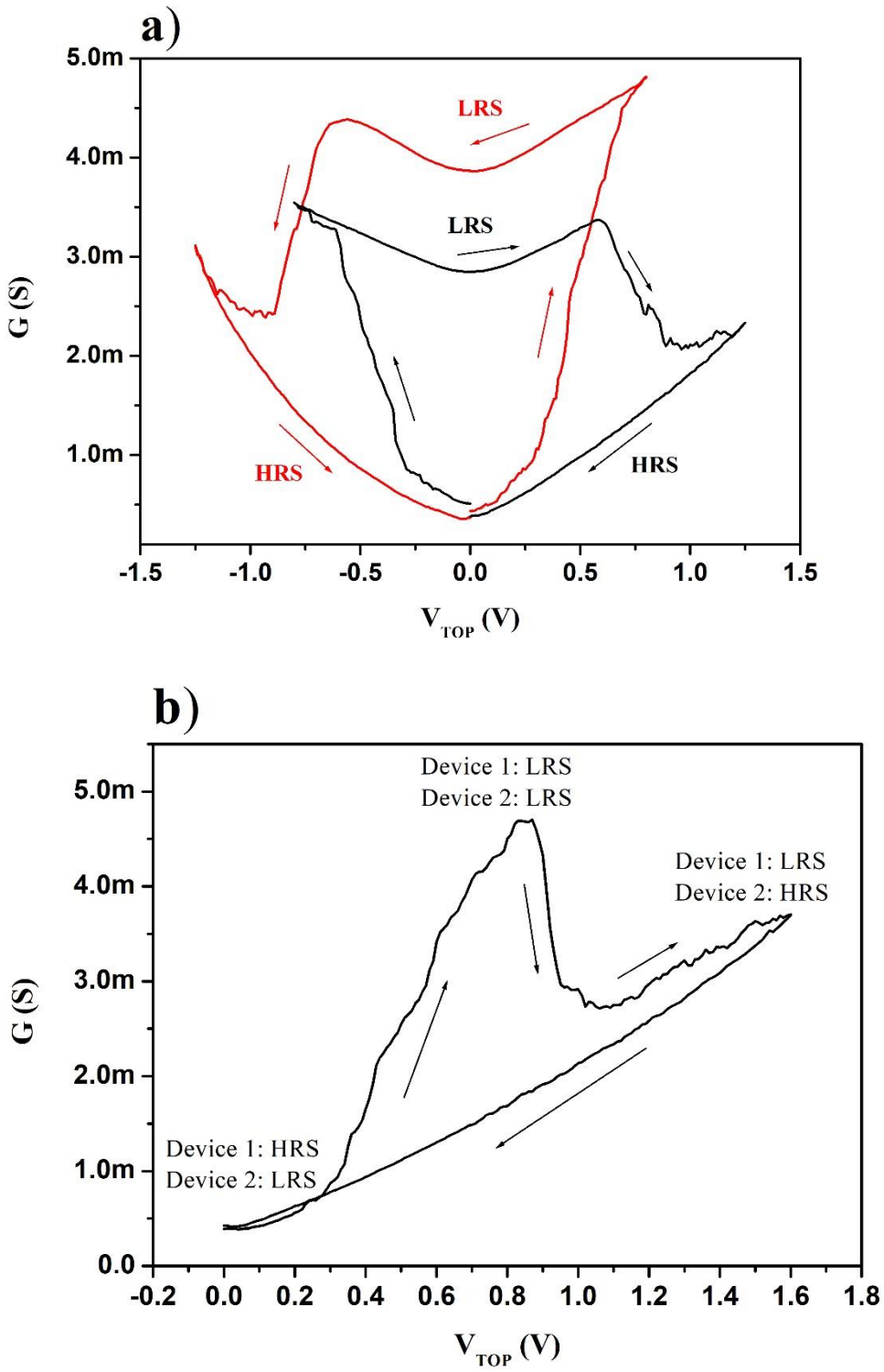


Figure 7: Conductance RS cycle measured in the anti-series configuration. Two different results series can be obtained (red and black colors) (a), and changing process between the two anti-series series (b).

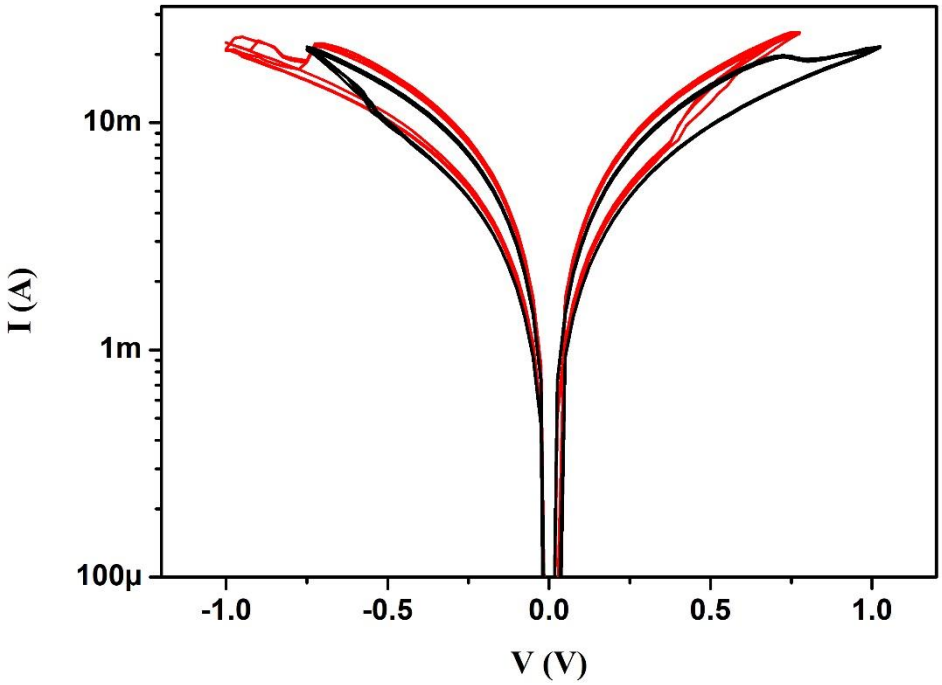


Figure 8: RS cycles measured in the anti-parallel configuration. Two different results series can be obtained (red and black colors).

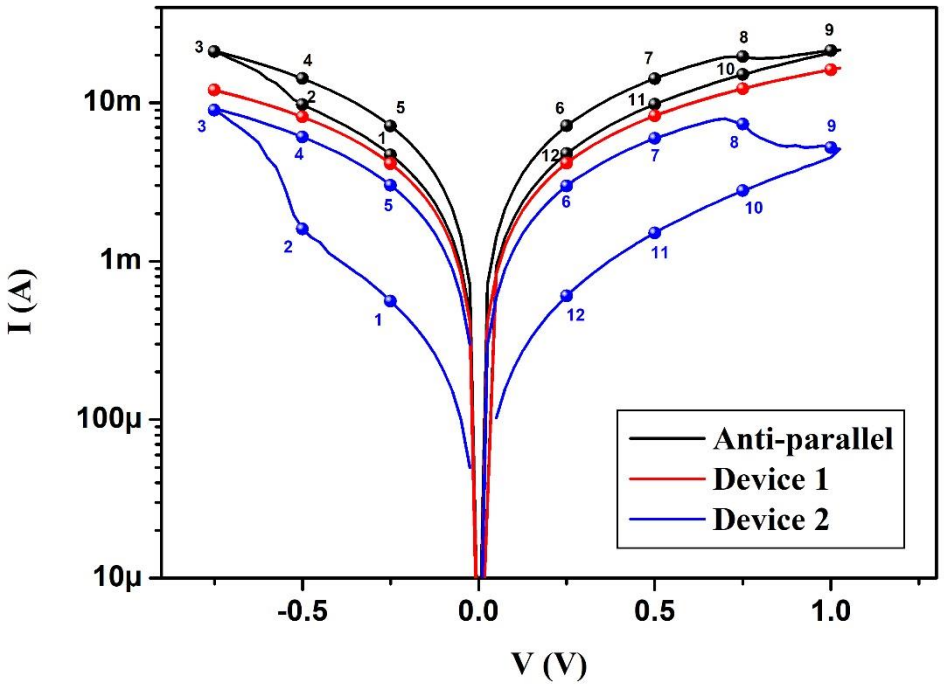


Figure 9: One RS cycle measured in the anti-parallel configuration. The black line corresponds to the operation of the anti-parallel structure, the red line corresponds to the operation of device 1 and the blue line corresponds to the operation of device 2.

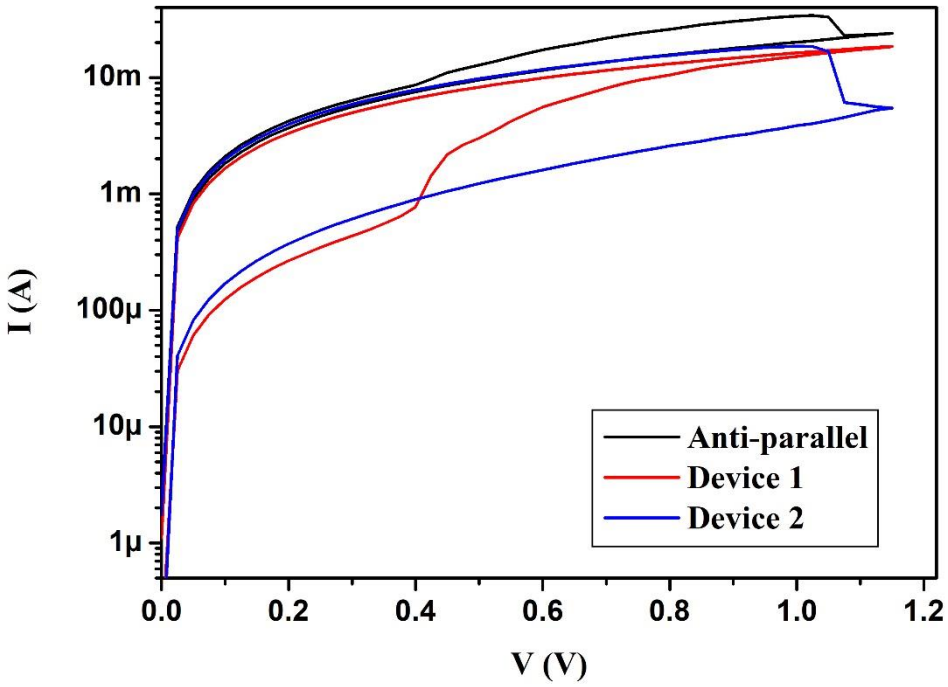


Figure 10: Changing between the two anti-parallel series process. High top electrode voltages are able to reset device 2, and device 1 is blocked in LRS.