

Study of the *set* and *reset* transitions in HfO₂-based ReRAM devices using a capacitor discharge

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ABSTRACT

In this work, we have studied the *set* and the *reset* transitions in hafnium oxide-based metal-insulator-metal ReRAM devices using a capacitor discharge. Instead of applying a conventional voltage or current signal, we have discharged a capacitor through the devices to perform both transitions. In this way, both transitions are shown to be controllable. An accumulative process is observed if we apply consecutive discharges, and, when increasing the capacitor voltage in each discharge, the transitions between both resistance states are complete. In addition, it has been shown that faster transitions require larger capacitor voltages.

1. Introduction

Resistive random-access memories (ReRAMs) are candidates for non-volatile memory technology. Their structure is simple and they exhibit a fast operation, good endurance, low power consumption and CMOS compatibility [1, 2]. Their operation is based on the resistive switching (RS) phenomenon, where a reversible resistance change takes place: a conductive filament (CF) between two metal electrodes can be formed and ruptured, obtaining two different resistance states, a low resistance state (LRS) and a high resistance state (HRS). In addition, these devices may exhibit tunable resistance states, which can be controlled by an electrical signal [3], since the CF dimensions can be electrically controlled. The analog-like multilevel operation is essential to implement artificial neuronal synapses in neuromorphic systems, as synaptic weight between two neurons can be electrically adjusted [4, 5]. Metal oxide-based ReRAM devices have been extensively studied, and specifically HfO₂-based devices were found to be highly scalable and robust, with ultrafast and low-energy consumption operation [6].

In this work, we study the *set* and *reset* transitions in HfO₂-based ReRAM devices. The transitions are important in both memory and in neuromorphic applications. In order to perform the study, we have used an external capacitor discharge through the devices. In a previous work we studied the switching transitions using voltage pulses [7], but the *set* transition could not be studied as power suddenly increased when keeping the voltage constant. We also used current pulses [8], but in this case the *reset* transition could not be studied, because power suddenly increased when keeping the current value constant. In the present work, both *set* and *reset* transitions are controllable. Power applied to the devices and the time the current flows through them have an equal impact: an increase in one of these parameters can balance a decrease in the other one. However, a minimum value in each of them is necessary to be able to perform a resistance change. An accumulative process has also been observed, so we can achieve HRS→LRS or LRS→HRS transitions by applying consecutive discharges. However, in order to perform a full transition between both conductance states, the current flowing through the devices has to be increased in each consecutive capacitor discharge.

2. Experimental

We studied the resistive switching phenomenon in TiN/Ti/HfO₂/W metal-insulator-metal devices. The hafnium oxide has a thickness of 10 nm, and was grown using the atomic layer deposition (ALD) technique at 225 °C. Tetrakis(dimethylamido)hafnium (TDMAH) was used as hafnium precursor and water was used as oxygen precursor. Nitrogen was used as both carrier and purge gas. Metal electrodes were deposited by magnetron sputtering. The bottom electrode consists of a 50 nm-W layer deposited on a 20 nm-Ti adhesion layer on a highly doped n-type silicon wafer. Electrical contact to the bottom electrode is made through the Al-metallized back of the silicon wafer. The top electrode consists of a stack of a 200 nm TiN layer and a 10 nm Ti layer. The resulting structures were square cells of 40 × 40 μm².

An HP 4155B Semiconductor Parameter Analyzer was used to perform the current-voltage (I-V) measurements. Fig.1 shows the electrical characterization setup used to perform the measurements based on a capacitor discharge. Two relays control the capacitor charge and discharge: when φ₁ is *off* and φ₂ is *on*, a Keithley 617 electrometer charges the capacitor, and when φ₁ is *on* and φ₂ is *off*, the capacitor is discharged through the device.

3. Results and Discussion

Our devices show bipolar resistive switching, with *set* and *reset* transitions at top positive and negative voltages, respectively. The resistive switching mechanism is valence change memory effect, so the conductive filaments are due to oxygen vacancy clusters [9]. Before the conductive filament is formed, a forming process is carried out using a voltage sweep. Fig. 2 shows several I-V resistive switching cycles.

When discharging the capacitor, an electrical current flows through the device. The current value can be expressed by:

$$i(t) = \frac{V_C^0}{R(t)} \cdot \exp\left(\frac{-t}{R(t) \cdot C}\right) \quad (1)$$

where $R(t)$ is the ReRAM resistance, V_C^0 is the initial capacitor voltage and C is the capacitance value.

First, we applied different capacitor discharges, changing the initial capacitor voltage (V_C^0), being the device in the HRS (*set* transition) or in the LRS state (*reset* transition). In the case of the *set* transition, the initial capacitor charge was always 1 nC, and in the case of the *reset* transition was always 8 nC (charged with negatives voltages).

The results are shown in Fig. 3, where the conductance value, G , was measured by applying a voltage of +0.1 V to the top electrode (this value was used in all our conductance measurements). The x -axis represents the initial power absorbed by the device $P_0 = V_C^0 \cdot i(t = 0)$ ($t = 0$ corresponds to instant in which the relay φ₁ is closed). The power needed for the LRS→HRS transition is higher than the one necessary for the LRS→LRS transition, as expected from the measured I-V characteristics.

Nevertheless, the change in resistance not only depends on P_0 but also on how long the power is absorbed by the device. According to Eq. 1, and defining the time constant parameter τ ($\tau(t) = R(t) \cdot C$), the higher the τ values the wider the current pulses. In order to modify the τ value with P_0 constant, C is changed while keeping the initial voltage V_C^0 constant. Fig. 4 shows the results obtained, being the device either in HRS (*set* transition) or in the LRS state (*reset* transition) before each capacitor discharge. The

1 initial power P_0 required to obtain the same change in conductance decreases for longer
2 capacitor discharges. This result agrees with Yu *et al.* [10], who observed that the
3 switching time in metal oxide ReRAM devices exponentially decreases as voltage pulses
4 amplitude increases. This dilemma (higher bias necessary for higher operation speed) has
5 already been reported [11]. However, a minimum discharge time is necessary to change
6 the conductivity state: for instance, using $P_0=14$ mW in the *reset* transition makes the
7 transition to start for τ values larger than about 0.1 μ s. But if the initial power is too low,
8 the transition could not even take place: for instance, 0.3 mW is not high enough to begin
9 a *set* transition regardless of the discharge time. So both power and discharge time can
10 limit the resistance change.

11 Regarding the *set* transition, the change in conductance reaches a saturation point when τ
12 value increases. When the conductive filament gets thicker, current can flow without
13 changing the CF structure. Of course, the conductance saturation value increases for
14 higher P_0 values, because the CF needs to be wider to be able to hold larger currents.
15 However, in the case of the *reset* transition the conductive filament is ruptured even for
16 $P_0=9$ mW. Yun *et al.* found the CF retraction in the *reset* transition in ReRAM devices is
17 due to the motion of oxygen ions with the help of an electric field and Joule heating [12].
18 When the CF gets thinner its resistance value increases, and the Joule heating should
19 increase for larger capacitor discharges, which helps the CF rupture.

20 The fact that longer discharges increase the conductance change can lead to an
21 accumulative effect. In the case of the *set* transition, we applied several consecutive
22 discharges. The device was first driven to the HRS, and then identical discharges, biasing
23 the capacitor with +0.75 V, were applied. Three different capacitance values were used,
24 and the results are shown in Fig. 5. After applying the first pulse, a larger conductance
25 change is observed for larger capacitance values, as expected from the results in Fig. 4,
26 since larger capacitances correspond to higher τ values. After the first pulse is applied,
27 the conductance value has increased, so when the following discharges are applied, P_0
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29 discharges take place, the conductance does not increase anymore. This can be explained
30 as follows: after a capacitor discharge is applied, not only the resistance value decreases
31 but also τ value decreases. The discharge time becomes so short that no change in
32 conductance is possible. We should use higher P_0 values in order to obtain a complete *set*
33 transition. For instance, Jang *et al.* obtained a complete *set* transition when applying
34 increasing voltage pulses [13]. Accordingly, we then applied consecutive but not identical
35 discharges: after each pulse is applied, the V_C^0 is increased, so the decrease in the τ value
36 can be balanced with a higher P_0 value. The results are shown in Fig. 6. The x -axis
37 represents the V_C^0 value of each consecutive discharge. We can observe a minimum V_C^0
38 value is needed (so a minimum P_0 value) to start the transition, which increases for low
39 capacitor values (so for low τ values). However, now the *set* transition can be fully
40 completed for consecutive capacitor discharges. Of course, higher V_C^0 values are
41 necessary for lower capacitor values in order to perform a complete transition.

42 We also studied the *reset* transition by using consecutive and identical capacitor
43 discharges. In this case, the device was first biased so it was in the LRS, but after a
44 discharge was applied, the device was not set again in the LRS. The capacitor was always
45 biased with -1.5 V. Three different capacitance values were also used, and the results are
46 shown in Fig. 7. In this transition the conductance value decreases for each discharge
47 applied, which means P_0 value also decreases. However, we can observe an accumulative
48 effect as conductance keeps decreasing for consecutive pulses. The reason is that now the
49 discharge time increases as discharges take place, so the decrease in P_0 value can be
50 balanced by a τ increase. We saw in Fig. 4 that the *reset* transition could be almost
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1 completed using low power values if τ value was high enough. However, after about 10
2 discharge cycles were applied, a larger number of cycles are necessary for a small
3 conductance change, so for very low power values, the conductance finally remains
4 almost constant. In the *set* transition, the limitation was due to the discharge length, but
5 now, in the *reset* transition the power is the limiting issue. As in the case of the *set*
6 transition, we have used consecutive but non identical discharges: the V_C^0 value is
7 increased after each discharge is performed. The results are shown in Fig. 8. Again, a
8 minimum V_C^0 value (i.e. a minimum P_0 value) is necessary to start the transition. This
9 minimum value increases for low capacitor values, because of their lower τ values. Now,
10 the V_C^0 increase balances the increment in $R(t = 0)$ values. The complete *reset* transition
11 is now possible.
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14 **4. Conclusions**

15 The use of a capacitor discharge through a ReRAM device has allowed us to study the *set*
16 and *reset* transitions between HRS and LRS states, as this operation enables controlling
17 the thickness of the conductive filament in HfO₂-based devices. The maximum power
18 depends on the initial capacitor voltage, and the time the current can flow through the
19 devices depends on the capacitor value. Both parameters can be independently controlled
20 in an easy way. We have observed a dilemma: the increase in one of these parameters is
21 able to balance the decrease in the other one. The use of high capacitor voltages means
22 short time current pulses are necessary, so obtaining high operation speed implies using
23 higher voltages. However, a minimum value of power and discharge time is required for
24 a resistance change, because if any of these values is not high enough, no resistance
25 change is observed at all. The use of a capacitor allows us to obtain short current pulses,
26 which is more difficult to obtain when using a current source. In this way, we have
27 observed that an accumulation process is possible when applying consecutive discharges:
28 we can obtain the same change in conductivity applying one longer discharge or several
29 shorter discharges. For identical capacitor discharges, this process is clearly not linear
30 and the conductance change is limited. In the *set* transition the limitation is due to a
31 discharge length decrease after each pulse is applied; in the case of the *reset* transition the
32 limitation is due to a power decrease after the application of each discharge. These
33 limitations can be avoided if we use different discharges: if consecutive discharges
34 increasing the capacitor voltage are applied, both transitions can be fully completed. This
35 could be an interesting issue for synaptic applications, although this operation has several
36 drawbacks, the main one being the time required for charging the capacitor and the fact
37 that turning *on* and *off* the relay devices is time consuming.
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45 **Acknowledgments**

46 This work was funded by the Spanish Ministry of Economy and Competitiveness and the
47 FEDER program through projects TEC2017-84321-C4-2-R and TEC2017-84321-C4-1-
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50 **References**

- 51 [1] Wang Z, Wu H, Burr G W, Hwang C S, Wang K L, Xia Q, Yang J J. Nat. Rev. Mater.
52 2020;5:173-95. <https://doi.org/10.1038/s41578-019-0159-3>
53
54 [2] Zidan M A, Strachan J P, Lu W D. Nat. Electron. 2018;1:22-9.
55 <https://doi.org/10.1038/s41928-018-0100-6>
56
57 [3] Castan H, Dueñas S, Garcia H, Ossorio O G, Domínguez L A, Sahelices B, Miranda
58 E, González M B, Campabadal F. J. Appl. Phys. 2018;124(15):152101.
59 <https://doi.org/10.1063/1.5024836>
60
61
62
63
64
65

- 1 [4] Chakraborty I, Jaiswal A, Saha A K, Gupta S K, Roy K. Appl. Phys. Rev.
2 2020;7:021308. <https://doi.org/10.1063/1.5113536>
3 [5] Woo J, Lee D, Koo Y, Hwang H. Microelectron. Eng. 2017;182:42-5.
4 <https://doi.org/10.1016/j.mee.2017.09.001>
5 [6] Bersuker G, Gilmer D C, Veksler D. in Advances in Non-Volatile Memory and
6 Storage Technology. 2nd ed. Woodhead Publishing, Elsevier. 2019;chap.2:35-102.
7 <https://doi.org/10.1016/b978-0-08-102584-0.00002-4>
8 [7] Garcia H, Ossorio O G, Dueñas S, Castán H. Microelectron. Eng. 2019;215:110984.
9 <https://doi.org/10.1016/j.mee.2019.110984>
10 [8] Garcia H, Dueñas S, OssorioOG, Castan H. IEEE J. Electron Devices Soc.
11 2020;8:291-6. <https://doi.org/10.1109/JEDS.2020.2979293>
12 [9] González-Cordero G, González M B, García H, Campabadal F, Dueñas S, Castán H,
13 Jiménez-Molinos F, Roldán J B. Microelectron. Eng. 2017;178:26-9.
14 <https://doi.org/10.1016/j.mee.2017.04.019>
15 [10] Yu S, Wong H-S P. IEEE Electron Device Lett. 2010;31(12):1455-7.
16 <https://doi.org/10.1109/LED.2010.2078794>
17 [11] Huang P, Liu X Y, Chen B, Li H T, Wang Y J, Deng Y X, Wei K L, Zeng L, Gao
18 B, Du G, Zhang X, Kang J F. IEEE Trans. Electron Devices 2013;60(12):4090-7.
19 <https://doi.org/10.1109/TED.2013.2287755>
20 [12] Yun H J, Ryu S Y, Lee H Y, ParkWY, Kim, S G. Ceram. Int. 2021;*in press*.
21 <https://doi.org/10.1016/j.ceramint.2021.02.231>
22 [13] Jang J W, Park S, Burr G W, Hwang H, Jeong Y H. IEEE Electron Device Lett.
23 2015;36(5):457-9. <https://doi.org/10.1109/LED.2015.2418342>
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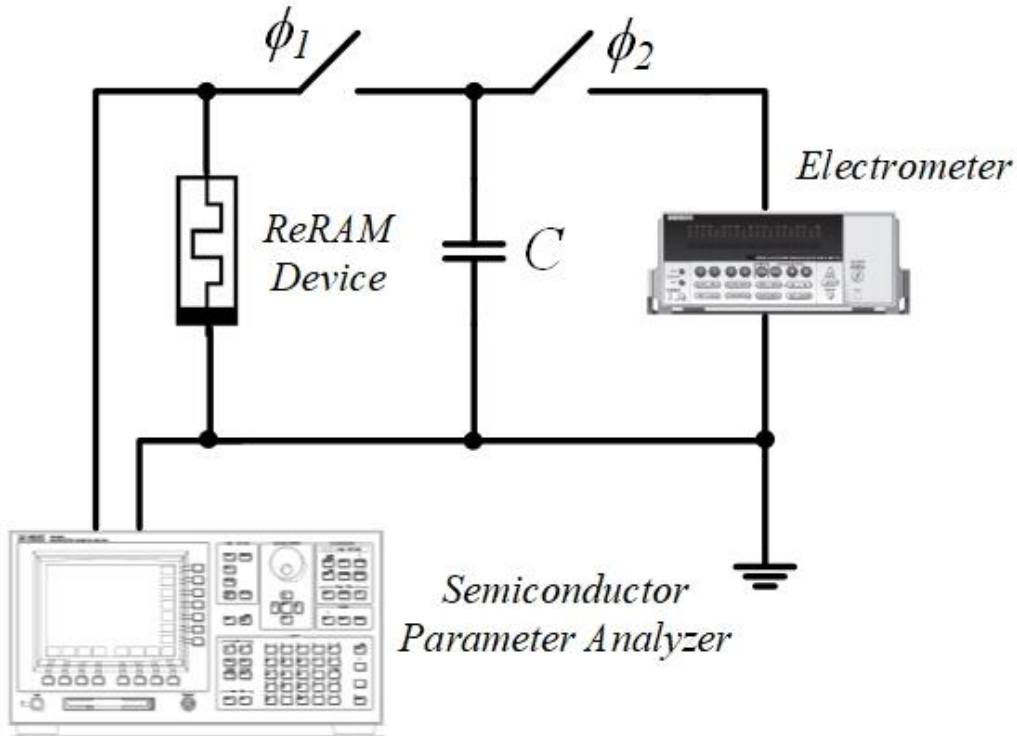


Figure 1: Electrical characterization setup used to perform the measurements based on a capacitor discharge.

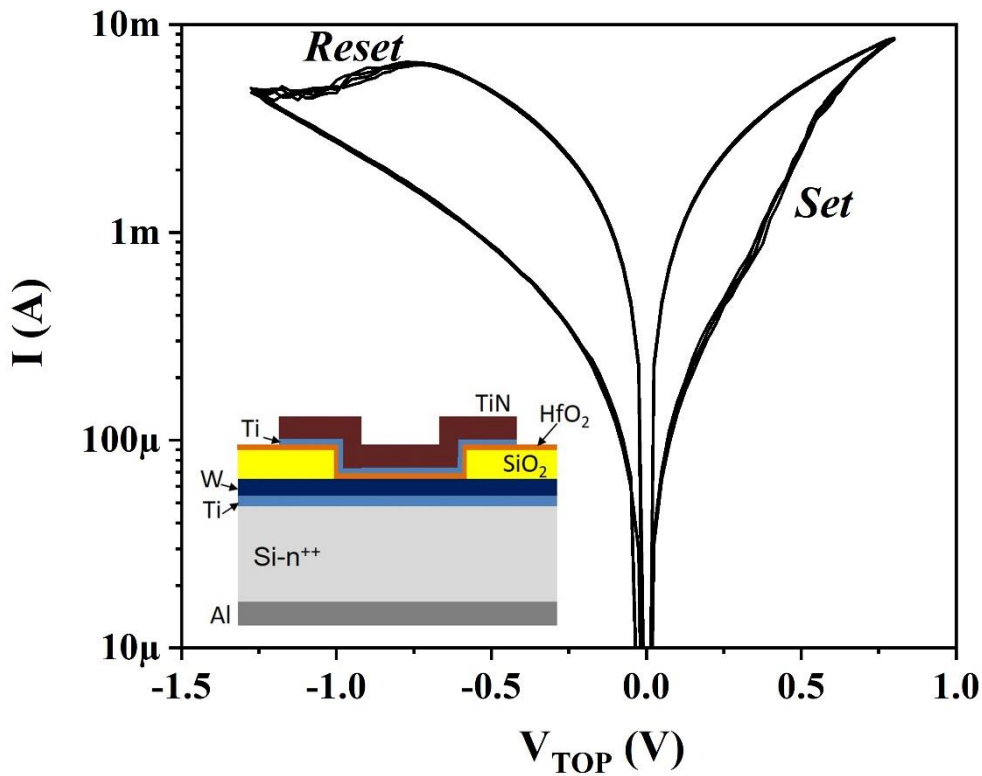


Figure 2: Current-Voltage cycles measured at room temperature and a cross-section image of our devices.

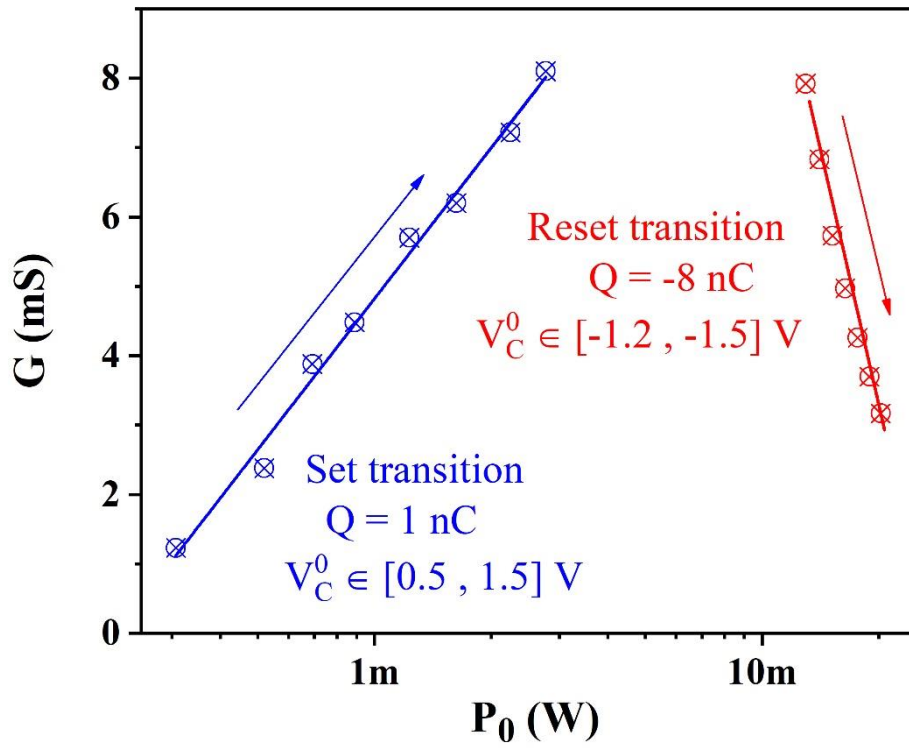


Figure 3: Conductance measured for the *set* and *reset* transitions obtained when discharging the capacitor with a constant charge and different initial voltages.

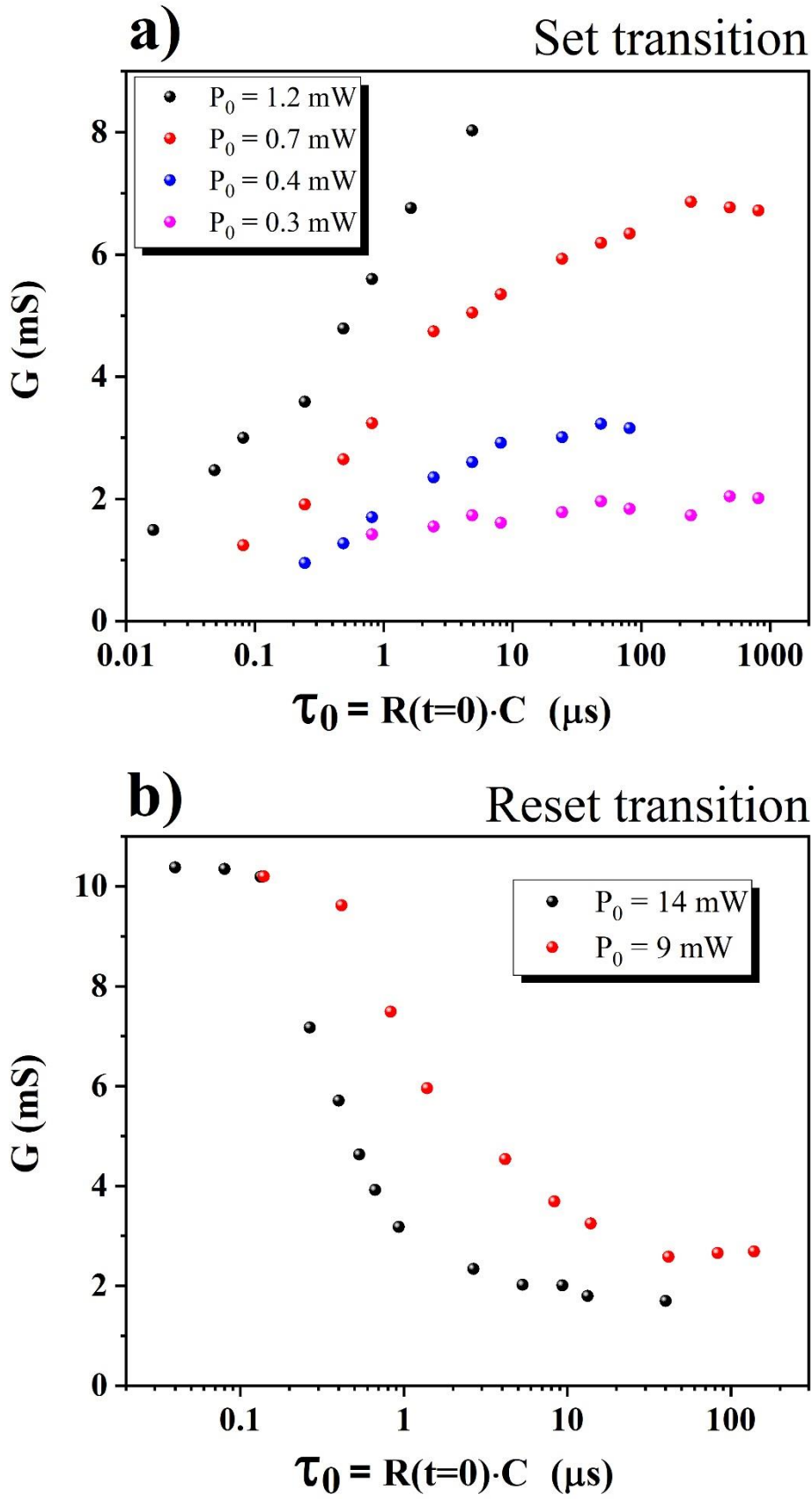


Figure 4: Conductance for the *set* (a) and *reset* (b) transitions obtained when keeping P_0 constant and varying τ_0 .

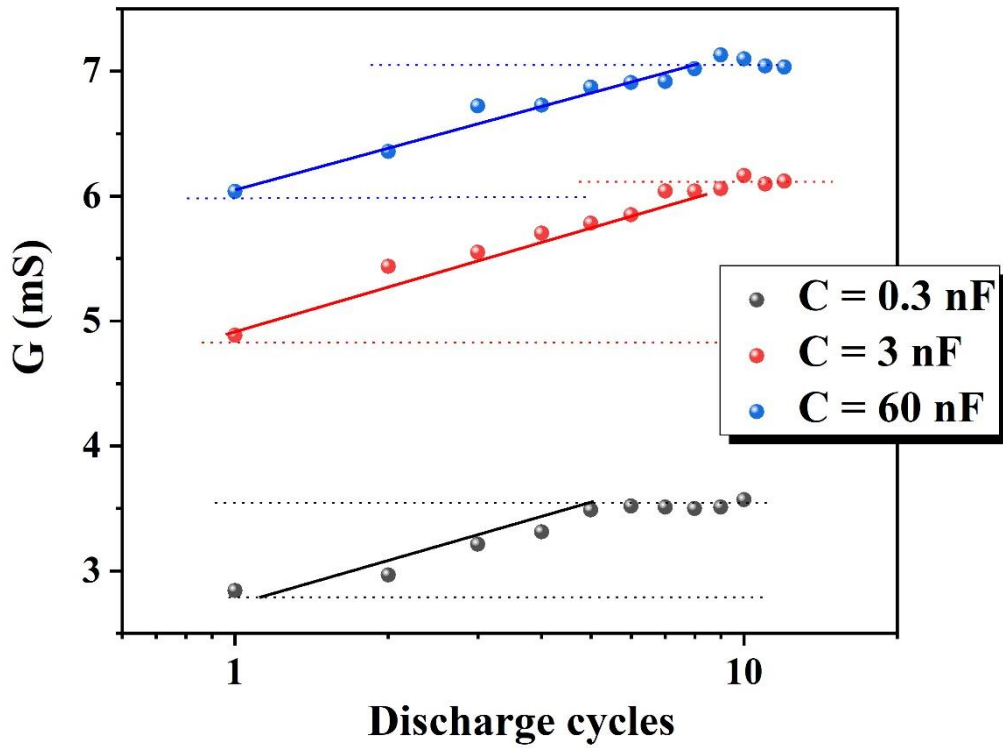


Figure 5: Conductance during the *set* transition obtained when applying consecutive and identical capacitor discharges.

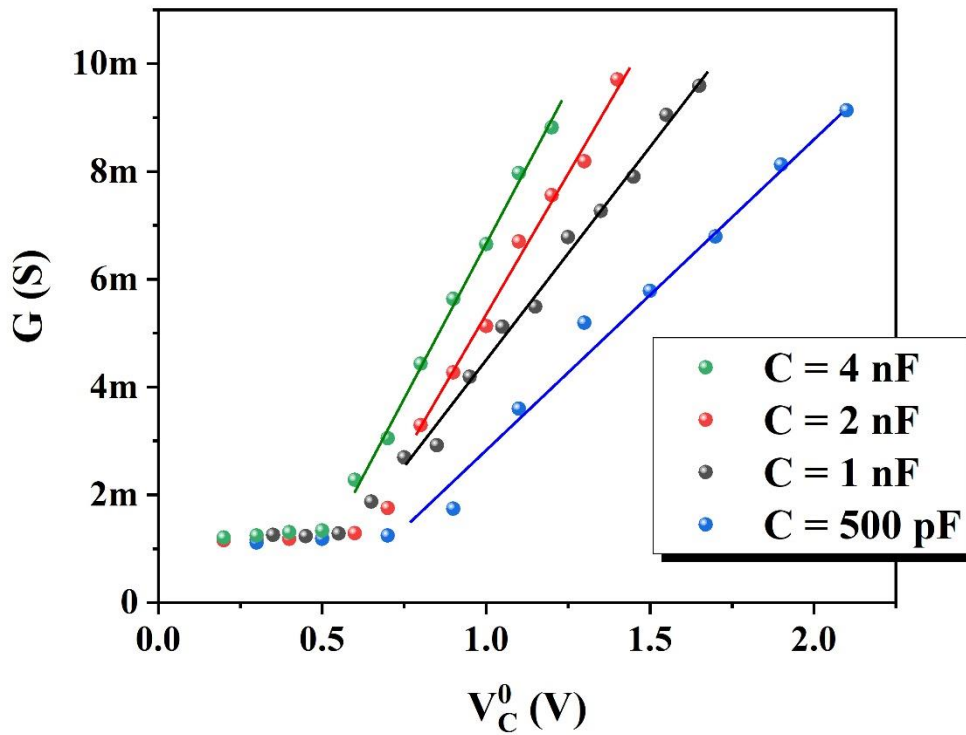


Figure 6: Conductance during the *set* transition obtained by consecutive capacitor discharges increasing the capacitor voltage.

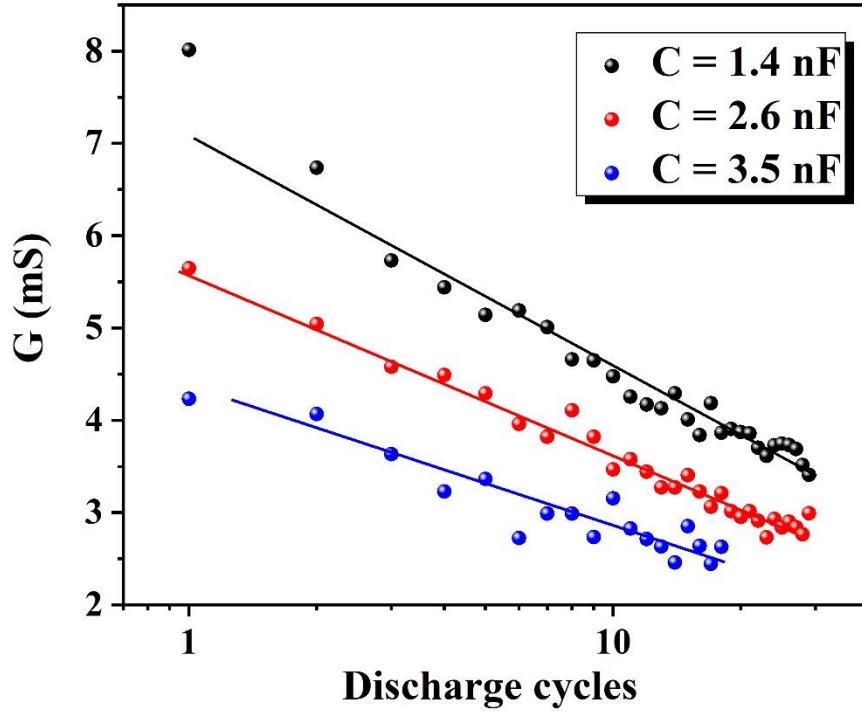


Figure 7: Conductance during the *reset* transition obtained when applying consecutive and identical capacitor discharges.

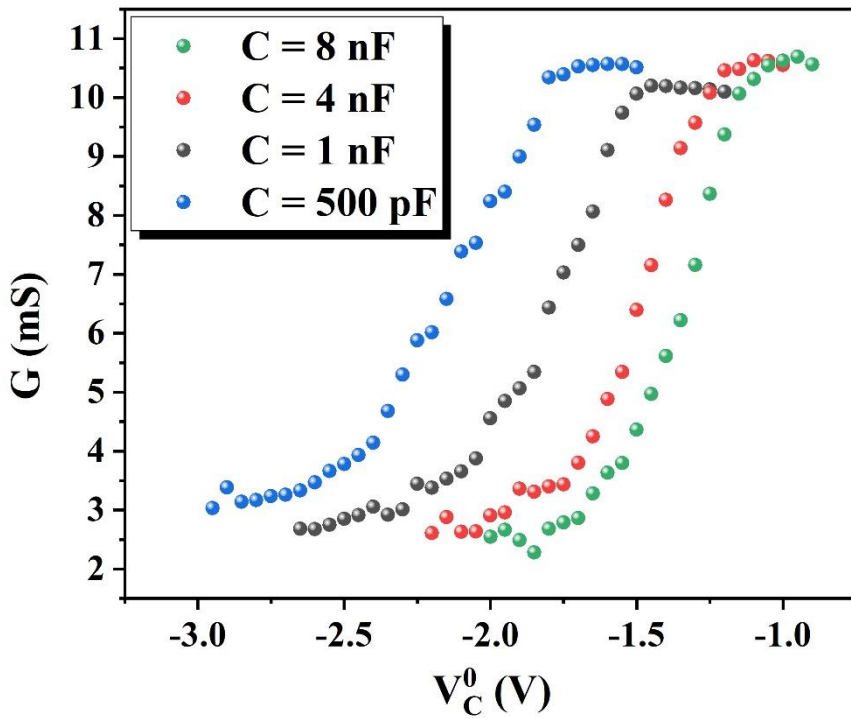


Figure 8: Conductance during the *reset* transition obtained by consecutive capacitor discharges increasing the capacitor voltage.

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In this work, we study the *set* and *reset* transitions in HfO₂-based ReRAM devices. The transitions are important in both memory and in neuromorphic applications. In order to perform the study, we have used an external capacitor discharge through the devices. In a previous work we studied the switching transitions using voltage pulses [7], but the *set* transition could not be studied as power suddenly increased when keeping the voltage constant. We also used current pulses [8], but in this case the *reset* transition could not be studied, because power suddenly increased when keeping the current value constant. In the present work, both *set* and *reset* transitions are controllable. Power applied to the devices and the time the current flows through them have an equal impact: an increase in one of these parameters can balance a decrease in the other one. However, a minimum value in each of them is necessary to be able to perform a resistance change. An accumulative process has also been observed, so we can achieve HRS→LRS or LRS→HRS transitions by applying consecutive discharges. However, in order to perform a full transition between both conductance states, the current flowing through the devices has to be increased in each consecutive capacitor discharge.

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48 effect as conductance keeps decreasing for consecutive pulses. The reason is that now the
49 discharge time increases as discharges take place, so the decrease in P_0 value can be
50 balanced by a τ increase. We saw in Fig. 4 that the *reset* transition could be almost
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1 completed using low power values if τ value was high enough. However, after about 10
2 discharge cycles were applied, a larger number of cycles are necessary for a small
3 conductance change, so for very low power values, the conductance finally remains
4 almost constant. In the *set* transition, the limitation was due to the discharge length, but
5 now, in the *reset* transition the power is the limiting issue. As in the case of the *set*
6 transition, we have used consecutive but non identical discharges: the V_C^0 value is
7 increased after each discharge is performed. The results are shown in Fig. 8. Again, a
8 minimum V_C^0 value (i.e. a minimum P_0 value) is necessary to start the transition. This
9 minimum value increases for low capacitor values, because of their lower τ values. Now,
10 the V_C^0 increase balances the increment in $R(t = 0)$ values. The complete *reset* transition
11 is now possible.
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14 **4. Conclusions**

15 The use of a capacitor discharge through a ReRAM device has allowed us to study the *set*
16 and *reset* transitions between HRS and LRS states, as this operation enables controlling
17 the thickness of the conductive filament in HfO₂-based devices. The maximum power
18 depends on the initial capacitor voltage, and the time the current can flow trough the
19 devices depends on the capacitor value. Both parameters can be independently controlled
20 in an easy way. We have observed a dilemma: the increase in one of these parameters is
21 able to balance the decrease in the other one. The use of high capacitor voltages means
22 short time current pulses are necessary, so obtaining high operation speed implies using
23 higher voltages. However, a minimum value of power and discharge time is required for
24 a resistance change, because if any of these values is not high enough, no resistance
25 change is observed at all. The use of a capacitor allows us to obtain short current pulses,
26 which is more difficult to obtain when using a current source. In this way, we have
27 observed that an accumulation process is possible when applying consecutive discharges:
28 we can obtain the same change in conductivity applying one longer discharge or several
29 shorter discharges. For identical capacitor discharges, this process is clearly not linear
30 and the conductance change is limited. In the *set* transition the limitation is due to a
31 discharge length decrease after each pulse is applied; in the case of the *reset* transition the
32 limitation is due to a power decrease after the application of each discharge. These
33 limitations can be avoided if we use different discharges: if consecutive discharges
34 increasing the capacitor voltage are applied, both transitions can be fully completed.
35 Finally, it is important to note that we have used this characterization setup only to study
36 the transitions between both resistance states. Although this setup could be an interesting
37 issue for synaptic applications, it is important to note that this operation had important
38 drawbacks: capacitors with high capacitance values could not be integrated due to area
39 consumption, the time required for charging the capacitor and the fact that turning *on* and
40 *off* the relay devices is also time consuming.
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48 **Acknowledgments**

49 This work was funded by the Spanish Ministry of Economy and Competitiveness and the
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52
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54 **References**

- 55 [1] Wang Z, Wu H, Burr G W, Hwang C S, Wang K L, Xia Q, Yang J J. Nat. Rev. Mater.
56 2020;5:173-95. <https://doi.org/10.1038/s41578-019-0159-3>
57
58 [2] Zidan M A, Strachan J P, Lu W D. Nat. Electron. 2018;1:22-9.
59 <https://doi.org/10.1038/s41928-018-0100-6>
60
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62
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- 1 [3] Castan H, Dueñas S, Garcia H, Ossorio O G, Domínguez L A, Sahelices B, Miranda
2 E, González M B, Campabadal F. J. Appl. Phys. 2018;124(15):152101.
3 <https://doi.org/10.1063/1.5024836>
- 4 [4] Chakraborty I, Jaiswal A, Saha A K, Gupta S K, Roy K. Appl. Phys. Rev.
5 2020;7:021308. <https://doi.org/10.1063/1.5113536>
- 6 [5] Woo J, Lee D, Koo Y, Hwang H. Microelectron. Eng. 2017;182:42-5.
7 <https://doi.org/10.1016/j.mee.2017.09.001>
- 8 [6] Bersuker G, Gilmer D C, Veksler D. in Advances in Non-Volatile Memory and
9 Storage Technology. 2nd ed. Woodhead Publishing, Elsevier. 2019;chap.2:35-102.
10 <https://doi.org/10.1016/b978-0-08-102584-0.00002-4>
- 11 [7] Garcia H, Ossorio O G, Dueñas S, Castán H. Microelectron. Eng. 2019;215:110984.
12 <https://doi.org/10.1016/j.mee.2019.110984>
- 13 [8] Garcia H, Dueñas S, OssorioOG, Castan H. IEEE J. Electron Devices Soc.
14 2020;8:291-6. <https://doi.org/10.1109/JEDS.2020.2979293>
- 15 [9] González-Cordero G, González M B, García H, Campabadal F, Dueñas S, Castán H,
16 Jiménez-Molinos F, Roldán J B. Microelectron. Eng. 2017;178:26-9.
17 <https://doi.org/10.1016/j.mee.2017.04.019>
- 18 [10] Yu S, Wong H-S P. IEEE Electron Device Lett. 2010;31(12):1455-7.
19 <https://doi.org/10.1109/LED.2010.2078794>
- 20 [11] Huang P, Liu X Y, Chen B, Li H T, Wang Y J, Deng Y X, Wei K L, Zeng L, Gao
21 B, Du G, Zhang X, Kang J F. IEEE Trans. Electron Devices 2013;60(12):4090-7.
22 <https://doi.org/10.1109/TED.2013.2287755>
- 23 [12] Yun H J, Ryu S Y, Lee H Y, Park WY, Kim, S G. Ceram. Int. 2021;47(12):16597-
24 602. <https://doi.org/10.1016/j.ceramint.2021.02.231>
- 25 [13] Jang J W, Park S, Burr G W, Hwang H, Jeong Y H. IEEE Electron Device Lett.
26 2015;36(5):457-9. <https://doi.org/10.1109/LED.2015.2418342>
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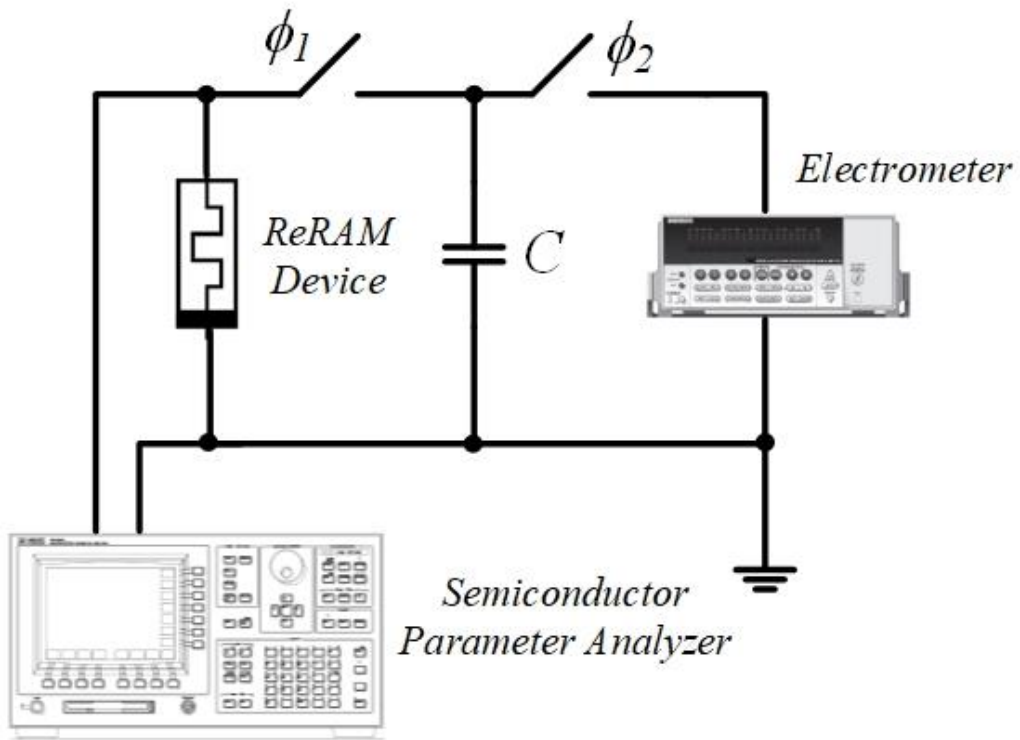


Figure 1: Electrical characterization setup used to perform the measurements based on a capacitor discharge.

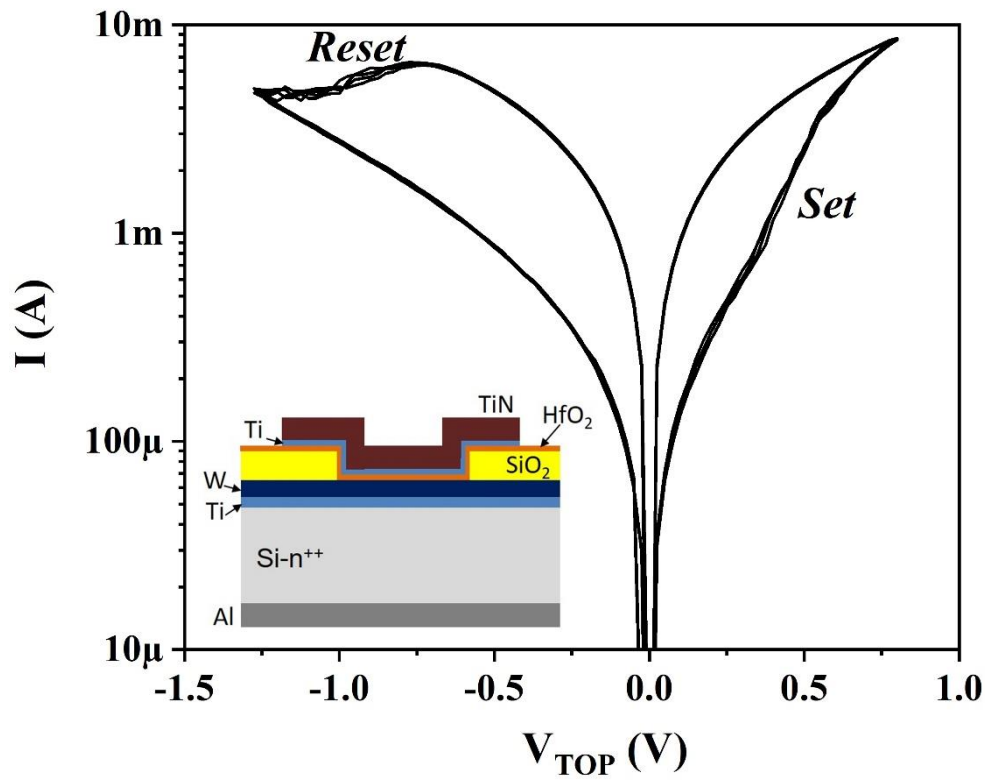


Figure 2: Current-Voltage cycles measured at room temperature and a cross-section image of our devices.

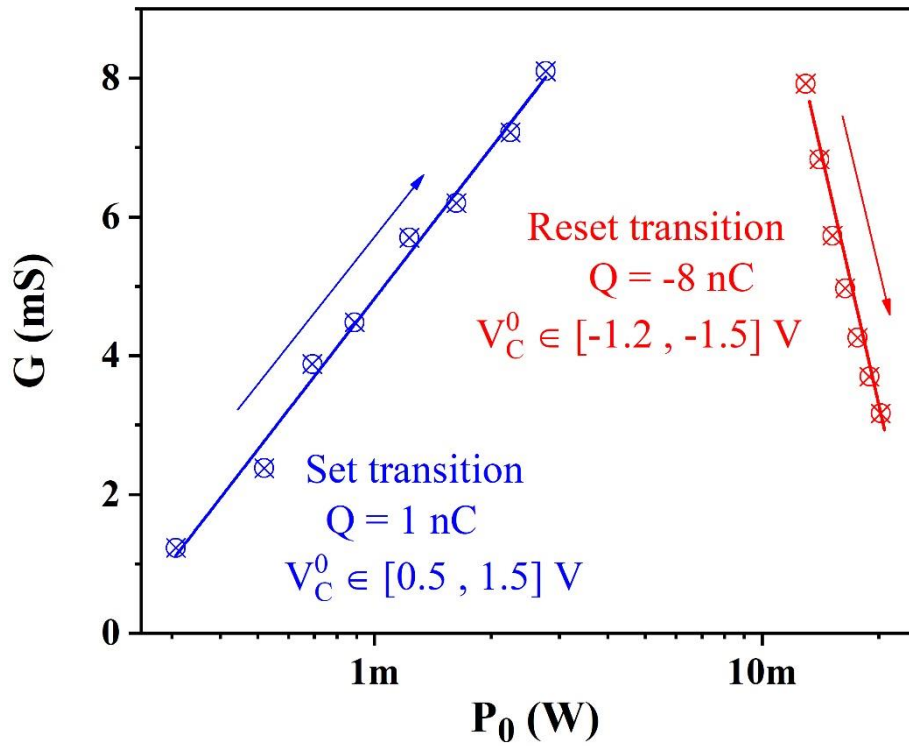


Figure 3: Conductance measured for the *set* and *reset* transitions obtained when discharging the capacitor with a constant charge and different initial voltages.

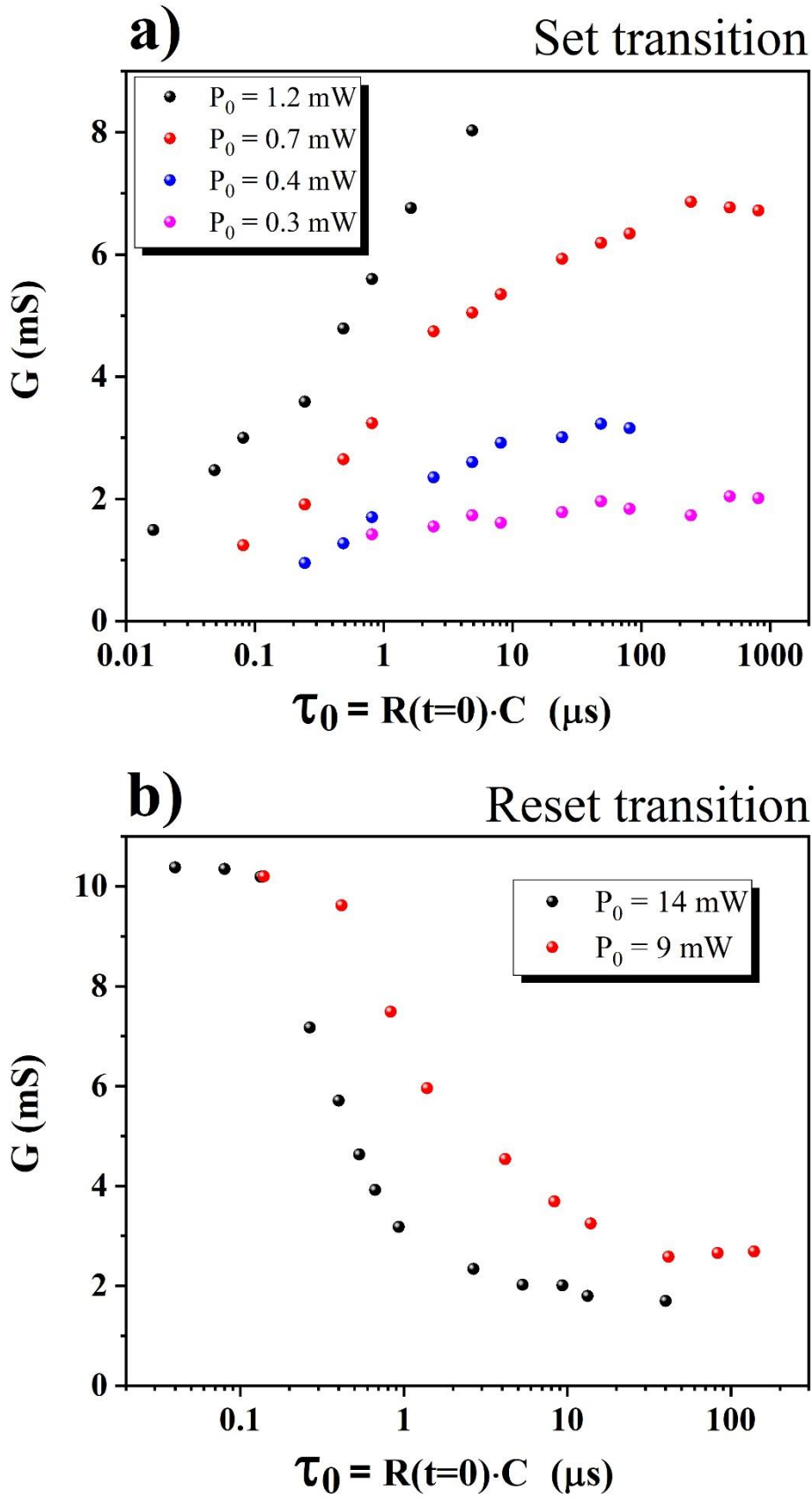


Figure 4: Conductance for the *set* (a) and *reset* (b) transitions obtained when keeping P_0 constant and varying τ_0 .

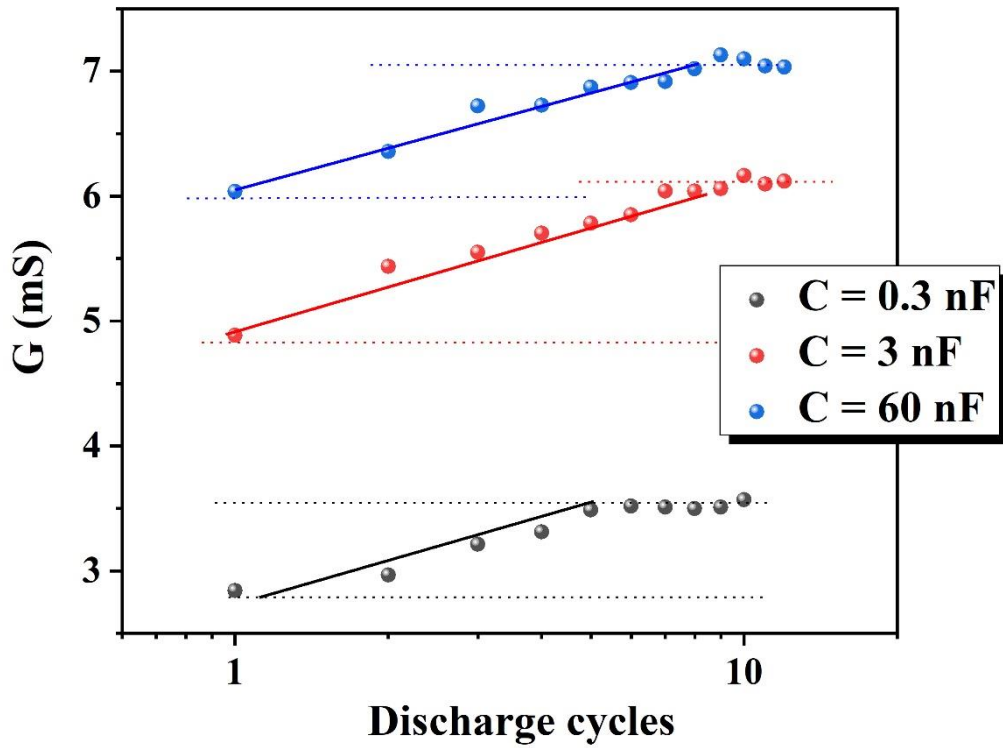


Figure 5: Conductance during the *set* transition obtained when applying consecutive and identical capacitor discharges.

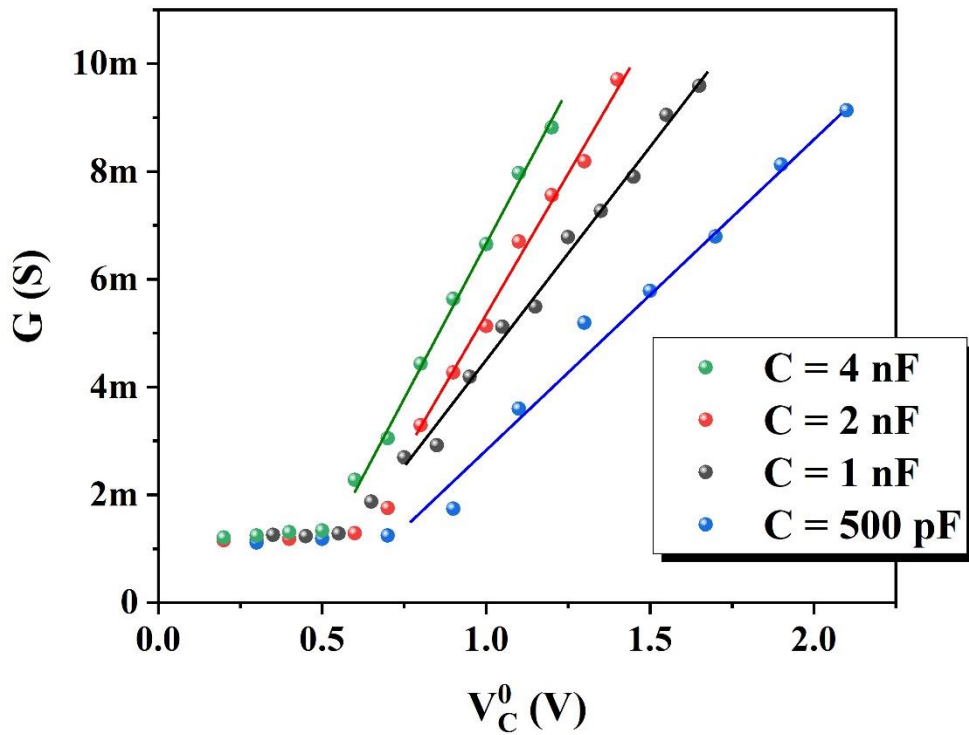


Figure 6: Conductance during the *set* transition obtained by consecutive capacitor discharges increasing the capacitor voltage.

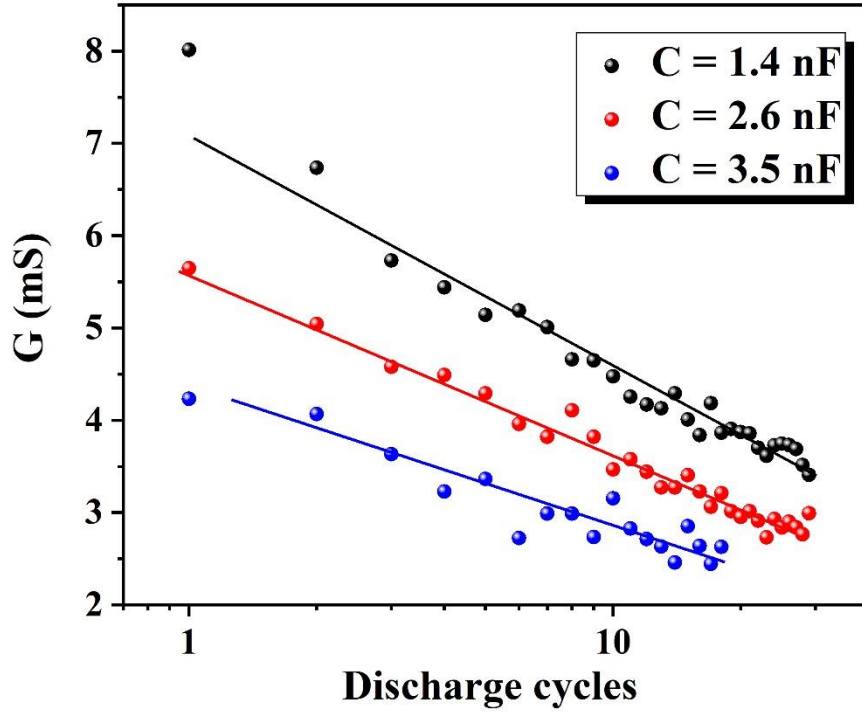


Figure 7: Conductance during the *reset* transition obtained when applying consecutive and identical capacitor discharges.

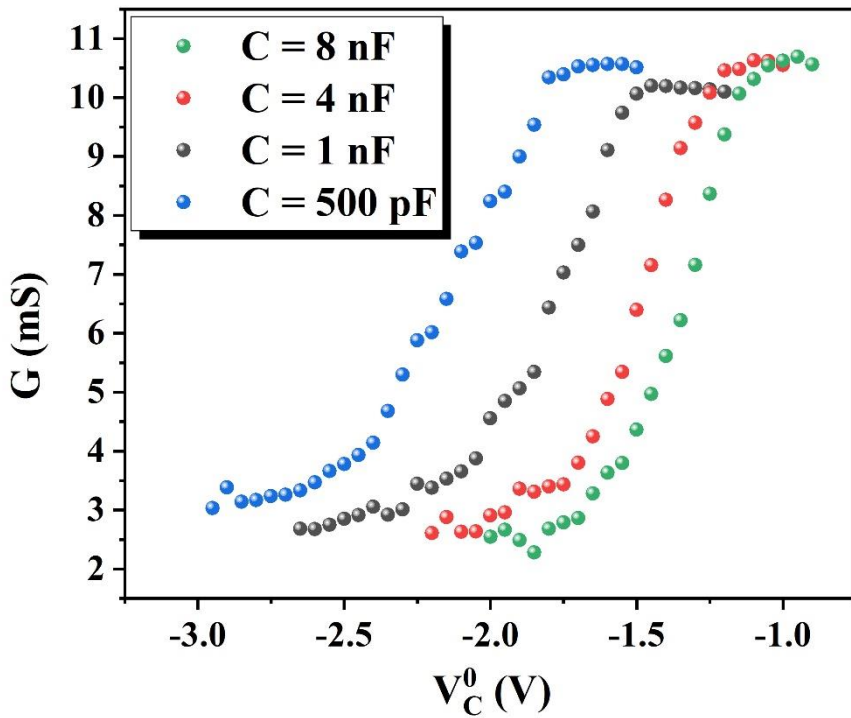
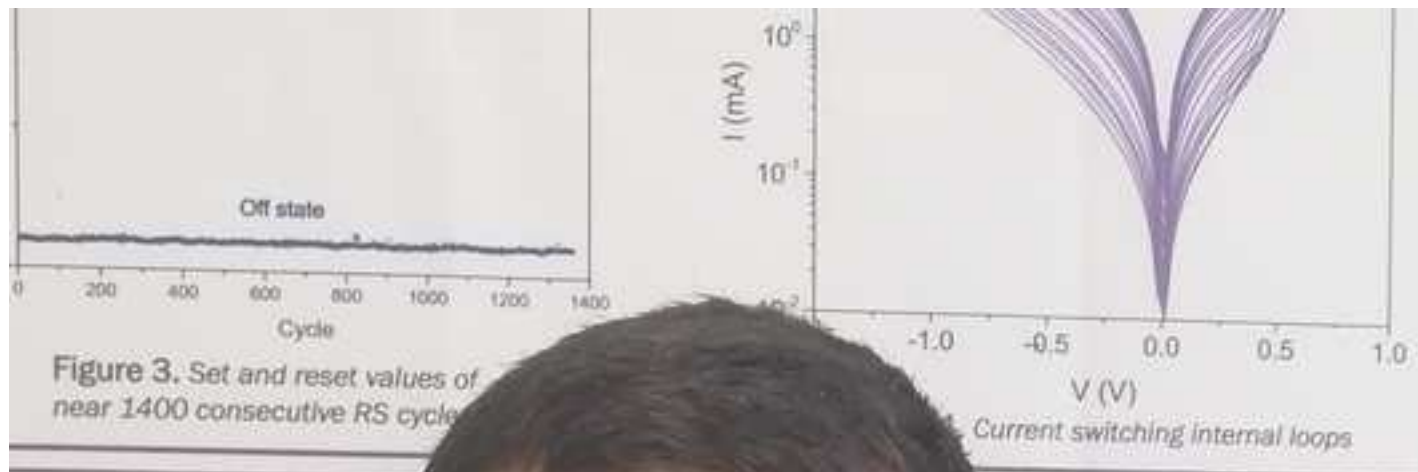


Figure 8: Conductance during the *reset* transition obtained by consecutive capacitor discharges increasing the capacitor voltage.

Héctor García was born in Valladolid (Spain) in 1979. He received the Bachelor and Ph.D. degrees in Physics from the University of Valladolid, Valladolid, Spain, in 2002 and 2006, respectively. In 2002, he joined the Department of Electronics, University of Valladolid. His current research interests include electrical characterization of semiconductors materials and devices, such as high-k dielectrics for logic and memory applications, solar cells, and ReRAM devices.



Declaration of interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Study of the *set* and *reset* transitions in HfO₂-based ReRAM devices using a capacitor discharge

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ABSTRACT

In this work, we have studied the *set* and the *reset* transitions in hafnium oxide-based metal-insulator-metal ReRAM devices using a capacitor discharge. Instead of applying a conventional voltage or current signal, we have discharged a capacitor through the devices to perform both transitions. In this way, both transitions are shown to be controllable. An accumulative process is observed if we apply consecutive discharges, and, when increasing the capacitor voltage in each discharge, the transitions between both resistance states are complete. In addition, it has been shown that faster transitions require larger capacitor voltages.

1. Introduction

Resistive random-access memories (ReRAMs) are candidates for non-volatile memory technology. Their structure is simple and they exhibit a fast operation, good endurance, low power consumption and CMOS compatibility [1, 2]. Their operation is based on the resistive switching (RS) phenomenon, where a reversible resistance change takes place: a conductive filament (CF) between two metal electrodes can be formed and ruptured, obtaining two different resistance states, a low resistance state (LRS) and a high resistance state (HRS). In addition, these devices may exhibit tunable resistance states, which can be controlled by an electrical signal [3], since the CF dimensions can be electrically controlled. The analog-like multilevel operation is essential to implement artificial neuronal synapses in neuromorphic systems, as synaptic weight between two neurons can be electrically adjusted [4, 5]. Metal oxide-based ReRAM devices have been extensively studied, and specifically HfO₂-based devices were found to be highly scalable and robust, with ultrafast and low-energy consumption operation [6].

In this work, we study the *set* and *reset* transitions in HfO₂-based ReRAM devices. The transitions are important in both memory and in neuromorphic applications. In order to perform the study, we have used an external capacitor discharge through the devices. In a previous work we studied the switching transitions using voltage pulses [7], but the *set* transition could not be studied as power suddenly increased when keeping the voltage constant. We also used current pulses [8], but in this case the *reset* transition could not be studied, because power suddenly increased when keeping the current value constant. In the present work, both *set* and *reset* transitions are controllable. Power applied to the devices and the time the current flows through them have an equal impact: an increase in one of these parameters can balance a decrease in the other one. However, a minimum value in each of them is necessary to be able to perform a resistance change. An accumulative process has also been observed, so we can achieve HRS→LRS or LRS→HRS transitions by applying consecutive discharges. However, in order to perform a full transition between both conductance states, the current flowing through the devices has to be increased in each consecutive capacitor discharge.

2. Experimental

We studied the resistive switching phenomenon in TiN/Ti/HfO₂/W metal-insulator-metal devices. The hafnium oxide has a thickness of 10 nm, and was grown using the atomic layer deposition (ALD) technique at 225 °C. Tetrakis(dimethylamido)hafnium (TDMAH) was used as hafnium precursor and water was used as oxygen precursor. Nitrogen was used as both carrier and purge gas. Metal electrodes were deposited by magnetron sputtering. The bottom electrode consists of a 50 nm-W layer deposited on a 20 nm-Ti adhesion layer on a highly doped n-type silicon wafer. Electrical contact to the bottom electrode is made through the Al-metallized back of the silicon wafer. The top electrode consists of a stack of a 200 nm TiN layer and a 10 nm Ti layer. The resulting structures were square cells of 40 × 40 μm².

An HP 4155B Semiconductor Parameter Analyzer was used to perform the current-voltage (I-V) measurements. Fig.1 shows the electrical characterization setup used to perform the measurements based on a capacitor discharge. Two relays control the capacitor charge and discharge: when φ₁ is *off* and φ₂ is *on*, a Keithley 617 electrometer charges the capacitor, and when φ₁ is *on* and φ₂ is *off*, the capacitor is discharged through the device.

3. Results and Discussion

Our devices show bipolar resistive switching, with *set* and *reset* transitions at top positive and negative voltages, respectively. The resistive switching mechanism is valence change memory effect, so the conductive filaments are due to oxygen vacancy clusters [9]. Before the conductive filament is formed, a forming process is carried out using a voltage sweep. Fig. 2 shows several I-V resistive switching cycles.

When discharging the capacitor, an electrical current flows through the device. The current value can be expressed by:

$$i(t) = \frac{V_C^0}{R(t)} \cdot \exp\left(\frac{-t}{R(t) \cdot C}\right) \quad (1)$$

where $R(t)$ is the ReRAM resistance, V_C^0 is the initial capacitor voltage and C is the capacitance value.

First, we applied different capacitor discharges, changing the initial capacitor voltage (V_C^0), being the device in the HRS (*set* transition) or in the LRS state (*reset* transition). In the case of the *set* transition, the initial capacitor charge was always 1 nC, and in the case of the *reset* transition was always 8 nC (charged with negatives voltages).

The results are shown in Fig. 3, where the conductance value, G , was measured by applying a voltage of +0.1 V to the top electrode (this value was used in all our conductance measurements). The x -axis represents the initial power absorbed by the device $P_0 = V_C^0 \cdot i(t = 0)$ ($t = 0$ corresponds to instant in which the relay φ₁ is closed). The power needed for the LRS→HRS transition is higher than the one necessary for the LRS→LRS transition, as expected from the measured I-V characteristics.

Nevertheless, the change in resistance not only depends on P_0 but also on how long the power is absorbed by the device. According to Eq. 1, and defining the time constant parameter τ ($\tau(t) = R(t) \cdot C$), the higher the τ values the wider the current pulses. In order to modify the τ value with P_0 constant, C is changed while keeping the initial voltage V_C^0 constant. Fig. 4 shows the results obtained, being the device either in HRS (*set* transition) or in the LRS state (*reset* transition) before each capacitor discharge. The

initial power P_0 required to obtain the same change in conductance decreases for longer capacitor discharges. This result agrees with Yu *et al.* [10], who observed that the switching time in metal oxide ReRAM devices exponentially decreases as voltage pulses amplitude increases. This dilemma (higher bias necessary for higher operation speed) has already been reported [11]. However, a minimum discharge time is necessary to change the conductivity state: for instance, using $P_0=14$ mW in the *reset* transition makes the transition to start for τ values larger than about 0.1 μ s. But if the initial power is too low, the transition could not even take place: for instance, 0.3 mW is not high enough to begin a *set* transition regardless of the discharge time. So both power and discharge time can limit the resistance change.

Regarding the *set* transition, the change in conductance reaches a saturation point when τ value increases. When the conductive filament gets thicker, current can flow without changing the CF structure. Of course, the conductance saturation value increases for higher P_0 values, because the CF needs to be wider to be able to hold larger currents. However, in the case of the *reset* transition the conductive filament is ruptured even for $P_0=9$ mW. Yun *et al.* found the CF retraction in the *reset* transition in ReRAM devices is due to the motion of oxygen ions with the help of an electric field and Joule heating [12]. When the CF gets thinner its resistance value increases, and the Joule heating should increase for larger capacitor discharges, which helps the CF rupture.

The fact that longer discharges increase the conductance change can lead to an accumulative effect. In the case of the *set* transition, we applied several consecutive discharges. The device was first driven to the HRS, and then identical discharges, biasing the capacitor with +0.75 V, were applied. Three different capacitance values were used, and the results are shown in Fig. 5. After applying the first pulse, a larger conductance change is observed for larger capacitance values, as expected from the results in Fig. 4, since larger larger capacitances correspond to higher τ values. After the first pulse is applied, the conductance value has increased, so when the following discharges are applied, P_0 value is increased and the cumulative effect can be observed. However, after some discharges take place, the conductance does not increase anymore. This can be explained as follows: after a capacitor discharge is applied, not only the resistance value decreases but also τ value decreases. The discharge time becomes so short that no change in conductance is possible. We should use higher P_0 values in order to obtain a complete *set* transition. For instance, Jang *et al.* obtained a complete *set* transition when applying increasing voltage pulses [13]. Accordingly, we then applied consecutive but not identical discharges: after each pulse is applied, the V_C^0 is increased, so the decrease in the τ value can be balanced with a higher P_0 value. The results are shown in Fig. 6. The x -axis represents the V_C^0 value of each consecutive discharge. We can observe a minimum V_C^0 value is needed (so a minimum P_0 value) to start the transition, which increases for low capacitor values (so for low τ values). However, now the *set* transition can be fully completed for consecutive capacitor discharges. Of course, higher V_C^0 values are necessary for lower capacitor values in order to perform a complete transition.

We also studied the *reset* transition by using consecutive and identical capacitor discharges. In this case, the device was first biased so it was in the LRS, but after a discharge was applied, the device was not set again in the LRS. The capacitor was always biased with -1.5 V. Three different capacitance values were also used, and the results are shown in Fig. 7. In this transition the conductance value decreases for each discharge applied, which means P_0 value also decreases. However, we can observe an accumulative effect as conductance keeps decreasing for consecutive pulses. The reason is that now the discharge time increases as discharges take place, so the decrease in P_0 value can be balanced by a τ increase. We saw in Fig. 4 that the *reset* transition could be almost

completed using low power values if τ value was high enough. However, after about 10 discharge cycles were applied, a larger number of cycles are necessary for a small conductance change, so for very low power values, the conductance finally remains almost constant. In the *set* transition, the limitation was due to the discharge length, but now, in the *reset* transition the power is the limiting issue. As in the case of the *set* transition, we have used consecutive but non identical discharges: the V_C^0 value is increased after each discharge is performed. The results are shown in Fig. 8. Again, a minimum V_C^0 value (i.e. a minimum P_0 value) is necessary to start the transition. This minimum value increases for low capacitor values, because of their lower τ values. Now, the V_C^0 increase balances the increment in $R(t = 0)$ values. The complete *reset* transition is now possible.

4. Conclusions

The use of a capacitor discharge through a ReRAM device has allowed us to study the *set* and *reset* transitions between HRS and LRS states, as this operation enables controlling the thickness of the conductive filament in HfO₂-based devices. The maximum power depends on the initial capacitor voltage, and the time the current can flow through the devices depends on the capacitor value. Both parameters can be independently controlled in an easy way. We have observed a dilemma: the increase in one of these parameters is able to balance the decrease in the other one. The use of high capacitor voltages means short time current pulses are necessary, so obtaining high operation speed implies using higher voltages. However, a minimum value of power and discharge time is required for a resistance change, because if any of these values is not high enough, no resistance change is observed at all. The use of a capacitor allows us to obtain short current pulses, which is more difficult to obtain when using a current source. In this way, we have observed that an accumulation process is possible when applying consecutive discharges: we can obtain the same change in conductivity applying one longer discharge or several shorter discharges. For identical capacitor discharges, this process is clearly not linear and the conductance change is limited. In the *set* transition the limitation is due to a discharge length decrease after each pulse is applied; in the case of the *reset* transition the limitation is due to a power decrease after the application of each discharge. These limitations can be avoided if we use different discharges: if consecutive discharges increasing the capacitor voltage are applied, both transitions can be fully completed. Finally, it is important to note that we have used this characterization setup only to study the transitions between both resistance states. Although this setup could be an interesting issue for synaptic applications, it is important to note that this operation had important drawbacks: capacitors with high capacitance values could not be integrated due to area consumption, the time required for charging the capacitor and the fact that turning *on* and *off* the relay devices is also time consuming.

Acknowledgments

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References

- [1] Wang Z, Wu H, Burr G W, Hwang C S, Wang K L, Xia Q, Yang J J. Nat. Rev. Mater. 2020;5:173-95. <https://doi.org/10.1038/s41578-019-0159-3>
- [2] Zidan M A, Strachan J P, Lu W D. Nat. Electron. 2018;1:22-9. <https://doi.org/10.1038/s41928-018-0100-6>

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- [4] Chakraborty I, Jaiswal A, Saha A K, Gupta S K, Roy K. *Appl. Phys. Rev.* 2020;7:021308. <https://doi.org/10.1063/1.5113536>
- [5] Woo J, Lee D, Koo Y, Hwang H. *Microelectron. Eng.* 2017;182:42-5. <https://doi.org/10.1016/j.mee.2017.09.001>
- [6] Bersuker G, Gilmer D C, Veksler D. in *Advances in Non-Volatile Memory and Storage Technology*. 2nd ed. Woodhead Publishing, Elsevier. 2019;chap.2:35-102. <https://doi.org/10.1016/b978-0-08-102584-0.00002-4>
- [7] Garcia H, Ossorio O G, Dueñas S, Castán H. *Microelectron. Eng.* 2019;215:110984. <https://doi.org/10.1016/j.mee.2019.110984>
- [8] Garcia H, Dueñas S, OssorioOG, Castan H. *IEEE J. Electron Devices Soc.* 2020;8:291-6. <https://doi.org/10.1109/JEDS.2020.2979293>
- [9] González-Cordero G, González M B, García H, Campabadal F, Dueñas S, Castán H, Jiménez-Molinos F, Roldán J B. *Microelectron. Eng.* 2017;178:26-9. <https://doi.org/10.1016/j.mee.2017.04.019>
- [10] Yu S, Wong H-S P. *IEEE Electron Device Lett.* 2010;31(12):1455-7. <https://doi.org/10.1109/LED.2010.2078794>
- [11] Huang P, Liu X Y, Chen B, Li H T, Wang Y J, Deng Y X, Wei K L, Zeng L, Gao B, Du G, Zhang X, Kang J F. *IEEE Trans. Electron Devices* 2013;60(12):4090-7. <https://doi.org/10.1109/TED.2013.2287755>
- [12] Yun H J, Ryu S Y, Lee H Y, Park W Y, Kim, S G. *Ceram. Int.* 2021;47(12):16597-602. <https://doi.org/10.1016/j.ceramint.2021.02.231>
- [13] Jang J W, Park S, Burr G W, Hwang H, Jeong Y H. *IEEE Electron Device Lett.* 2015;36(5):457-9. <https://doi.org/10.1109/LED.2015.2418342>

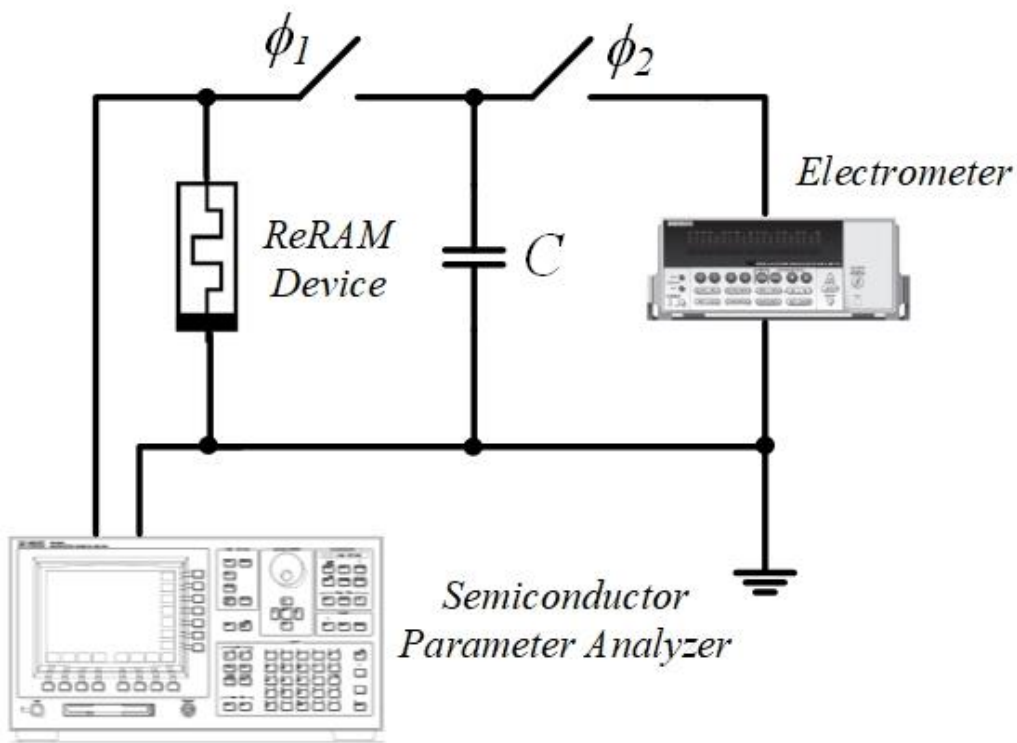


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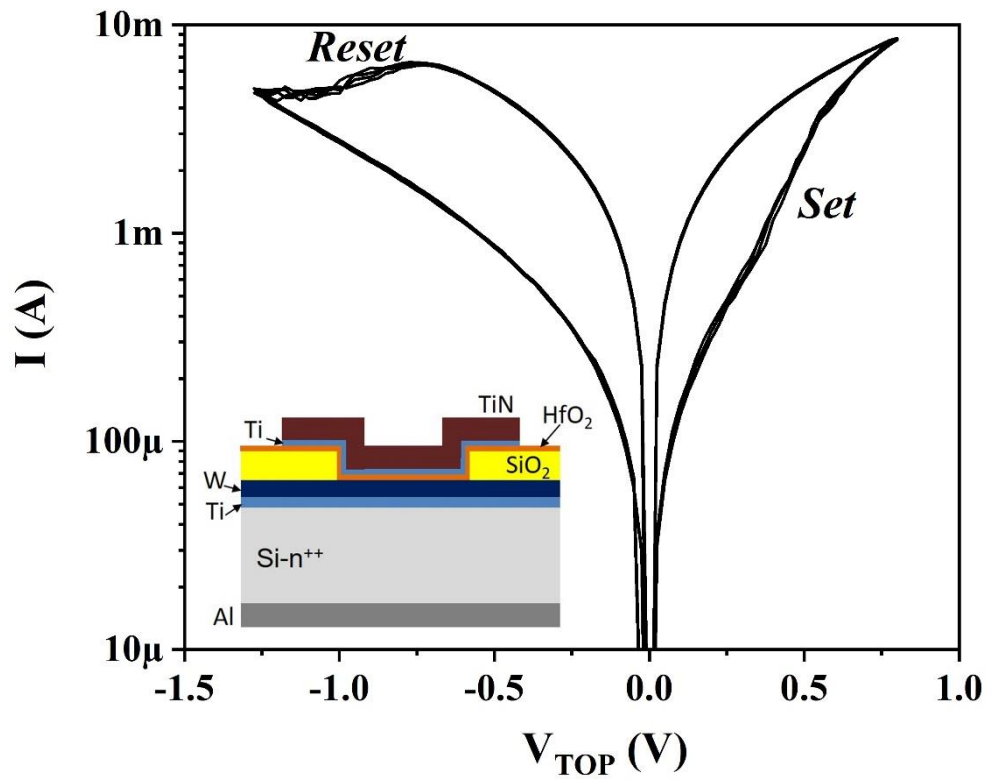


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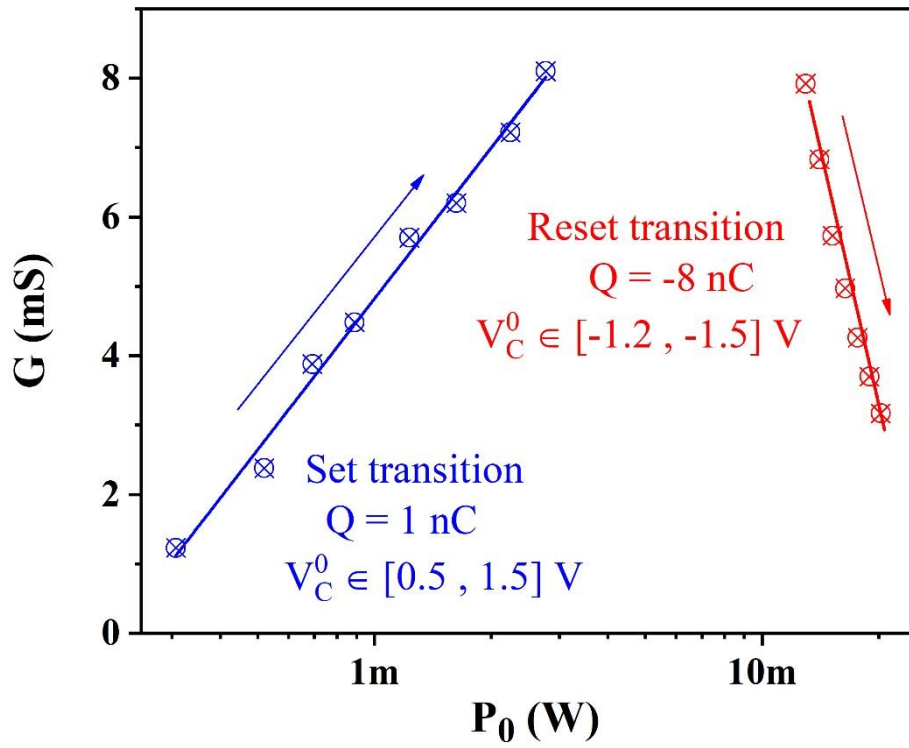


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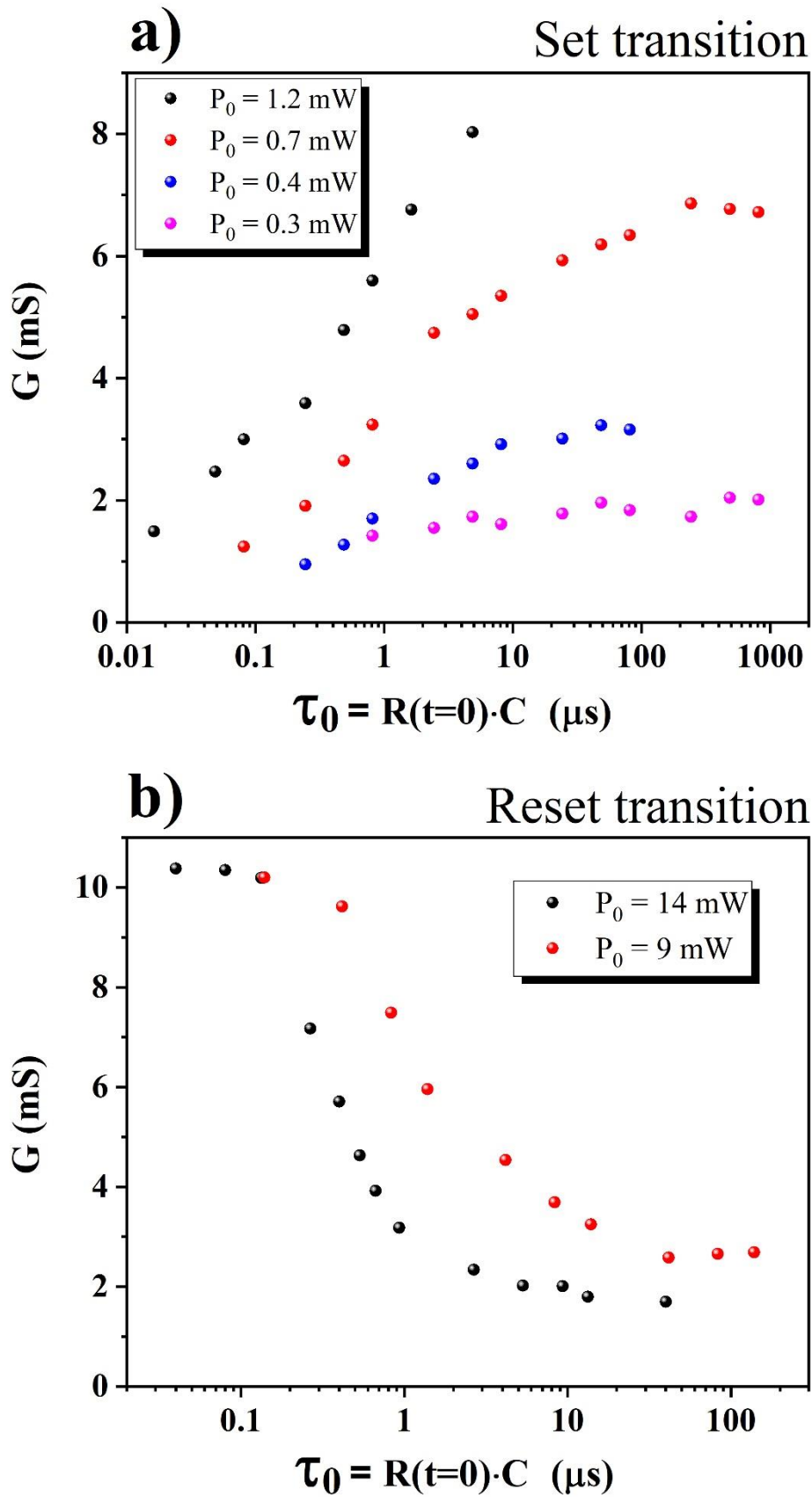


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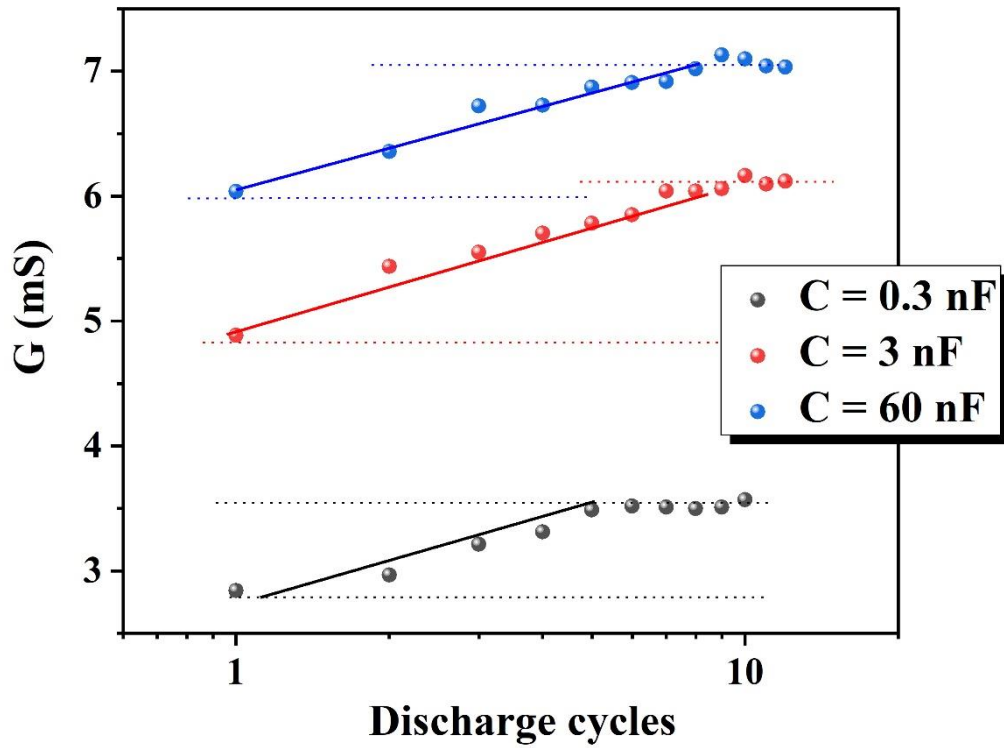


Figure 5: Conductance during the *set* transition obtained when applying consecutive and identical capacitor discharges.

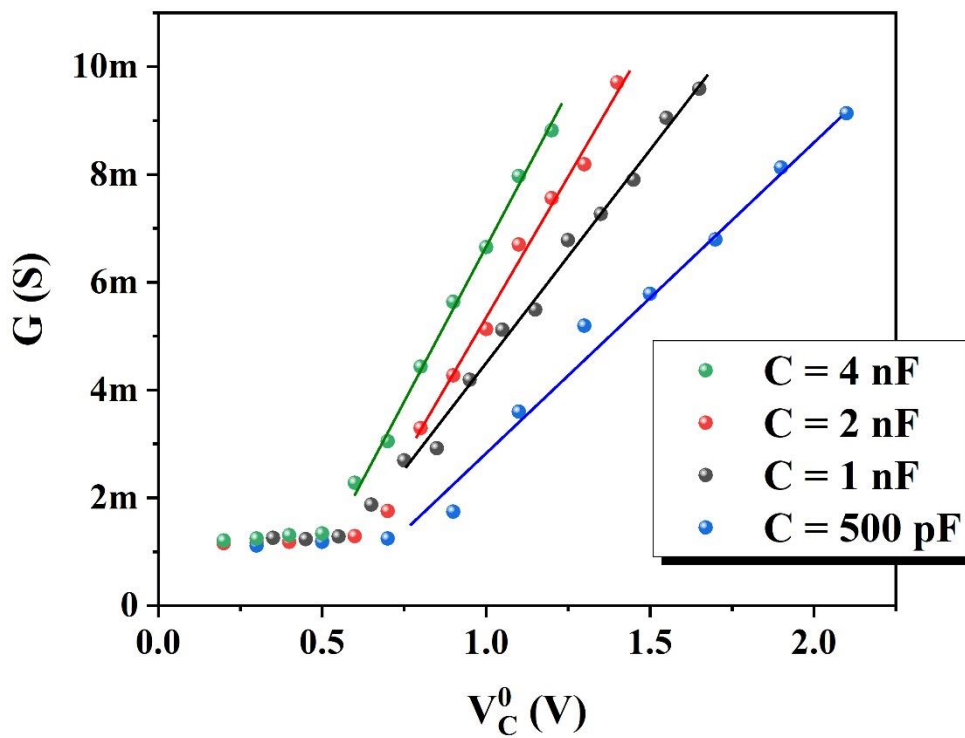


Figure 6: Conductance during the *set* transition obtained by consecutive capacitor discharges increasing the capacitor voltage.

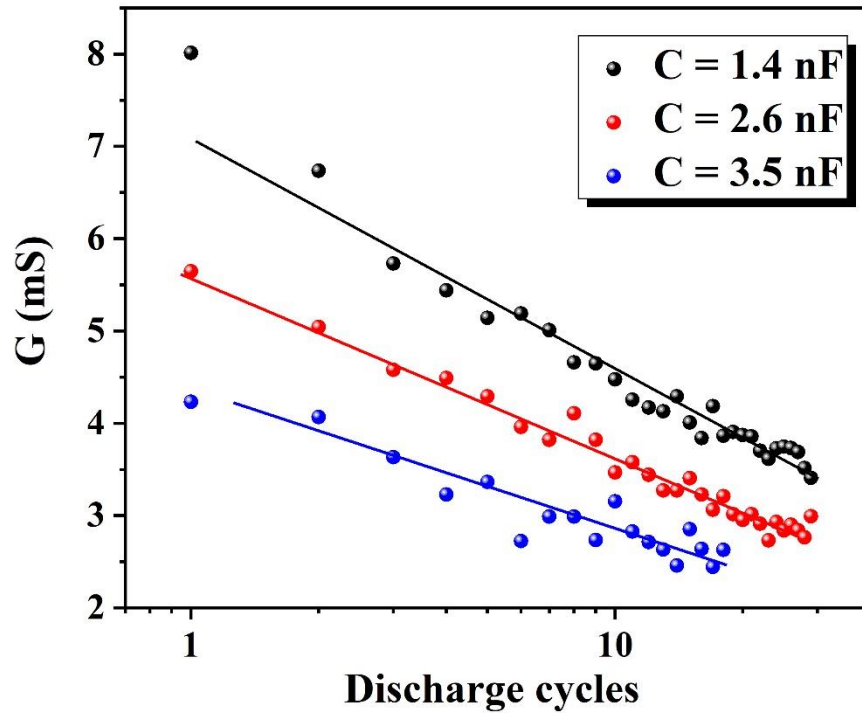


Figure 7: Conductance during the *reset* transition obtained when applying consecutive and identical capacitor discharges.

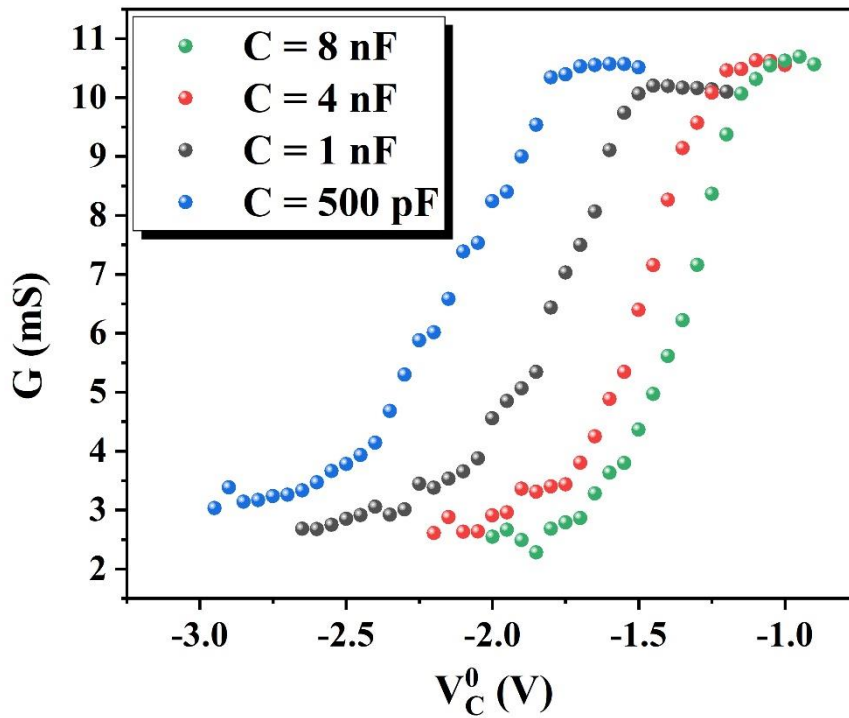


Figure 8: Conductance during the *reset* transition obtained by consecutive capacitor discharges increasing the capacitor voltage.