Advances in the development of high efficiency III-V multijunction solar cells on Ge|Si virtual substrates

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Abstract

Virtual Ge substrates fabricated by direct deposition of Ge on Si have become a pathway with high potential to attain high-efficiency III-V multijunction solar cells on Si. We study the development of III-V triple junction solar cells using two types of Ge|Si virtual substrates. The first uses a thick (2-5 μm) Ge layer grown by CVD, which acts as the bottom Ge subcell. The second, grown by low-temperature RT-PECVD, has a thickness of a few tens of nanometres, with the Si substrate acting as Si bottom cell. We discuss the challenges related to each design (formation of cracks, parasitic absorption in the Ge layer, dislocations, ...), present the theoretical design and show the experimental results obtained. Finally, an advanced approach using embedded porous Si layers as buffer layers for crack mitigation is also presented.

Introduction

State-of-the-art high efficiency III-V solar cells can be directly implemented on Ge|Si substrates, which is a major advantage as compared to other approaches to develop III-V solar cells on Si, which rely on thick graded buffers. To this end, two different Ge|Si template fabrication approaches are being assessed at IES-UPM. Firstly, multijunction solar cells with an active Ge bottom junction can be obtained with CVD-deposited Ge layers in the thickness range of 2–5 μm. The formation of cracks due to the difference in thermal expansion coefficients between Si and the rest of the materials requires designing the structures by minimizing the total epilayer thickness.

Secondly, the use of Ge layers in the range of a few tens of nm, deposited by RF-PECVD on Si, is an alternative route. In this case, the Si substrate will constitute the bottom subcell. The thin Ge helps prevent the formation of cracks, which is one of the main challenges in this technology. However, the parasitic light absorption within the Ge layer must be considered when designing the solar cell structure.

Finally, embedding a porous Si layer is also investigated as a way to achieve a compliant substrate to mitigate the formation of cracks in the structures.

In this work, we review the theoretical and experimental results obtained at IES-UPM on these design approaches, discussing their potential from the perspective of performance and technological challenges.

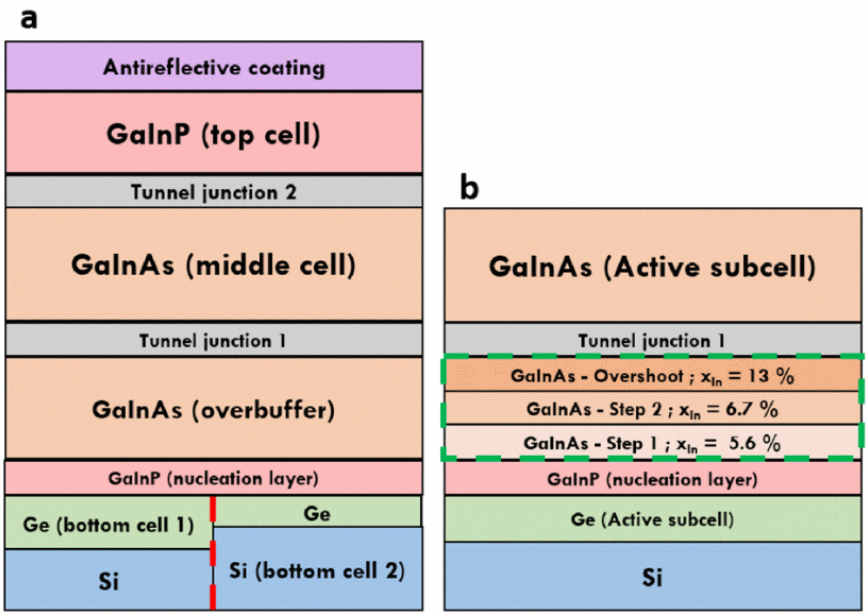

Figure 1.
(a) General structure of the triple-junction solar cells studied. The bottom cell can be the Ge or Si layers depending on the design being considered. (b) Design for thinned GaInAs/Ge 2JSC with increased indium content through a graded buffer (green dashed rectangle).

Methods

The theoretical analyses and fits to experimental data are primarily based on the Scattering Matrix Method to analyze the optical processes and on the Hovel model to calculate the photocurrents and recombination currents, as detailed elsewhere [1]–[2][3]. III-V structures are grown by metal-organic chemical vapor deposition (MOCVD) using standard precursors [3]. Thick Ge layers are deposited by reduced pressure chemical vapor deposition (RP-CVD) [3] and ultrathin Ge films are deposited by radio-frequency, plasma-enhanced chemical vapor deposition (RF-PECVD), using the process parameters explained elsewhere [4]. 0.1 cm^2 solar cells are manufactured using standard photolithography techniques and gold-based metal stacks, except for Si that uses a Pd/Ti/Pd/Al system (details in [1]).

III-V MJSC Designs

a) GaInP/GaInAs/Ge|Si with Active Ge Bottom Cell.

In this design, the function of the Ge layer of the Ge|Si virtual substrate is the bottom subcell (see Figure 1). Simulation studies indicated that the minimum thickness required in this Ge layer so as not to limit the photocurrent in the 3JSC is between 1 and 3 microns depending on the Ge|Si interface recombination velocity (see Figure 2a). Using Ge|Si templates with a 5 µm thick Ge layer, experimental triple-junction solar with promising carrier collection efficiencies in all subcells were demonstrated [2], [3]. However, the high TDD in the used templates drastically limited the voltage in these devices. Moreover, it was made apparent that the formation of cracks was a major challenge to tackle. Cracks appear when the critical thickness for their formation and/or propagation is surpassed. If this happens, sophisticated ways of reducing their formation or limiting their effect on the performance of the solar cells have been proposed, including the use of nanopatterning or geometrically controlling their formation [5], [6].

Alternatively, in our approach, the solar cell structure is redesigned to stay below the critical thickness for cracking. Firstly, the Ge layer is reduced from 5 to 3 μm, which should be sufficient to attain the required photocurrent (see Figure 2a). In addition, a theoretical study was conducted to assess the possibility of thinning the GaInAs middle cell, which was 3.5 μm thick in the original design. This requires lowering its bandgap (by increasing the indium composition) at the same time to compensate for the photocurrent reduction as the subcell is made thinner. In Figure 2b, the calculated J_{sc} of this subcell in the 3JSC is shown for a range of thicknesses and indium compositions. Around 8% of indium content seems to be suitable to reduce the layer to 1 μm. Of course, this bandgap reduction -due to indium increase-produces a voltage loss in the 3JSC but, if the material quality is maintained, the effect on the efficiency should be limited as compared to the overall benefits of using Ge|Si templates [1].

An 8% indium composition produces a 0.5% lattice-mismatch with Ge. To bridge the corresponding lattice constant difference, a compositionally graded buffer (CGB) is utilized (green dashed square in Fig. 1b). This CGB is designed ad-hoc so as not to add a significant thickness to the structure [1].

Figure 3 summarizes the EQE of the most representative experimental 3JSC solar cells designs in this approach, as compared to the case of standard Ge substrates. It can be observed that the growth on Ge|Si templates does not affect the EQE of the GaInP top cell significantly. However, the formation of cracks and the high TDD negatively impacts the carrier collection in the thick GaInAs subcell. The thinned structure with higher indium content in the GaInAs middle cell shows the expected bandgap shift in the middle cell, which allows maintaining the photocurrent despite its lower thickness. However, the GaInP top cell also shows a bandgap shift since it is lattice-matched to the GaInAs with increased indium content. This effect reduces the photocurrent in the GaInAs middle cell. To circumvent this problem, we propose either increasing the bandgap of the top cell using AIGaInP or using GaInP but thinning it to compensate for the bandgap shift described. The first option is illustrated in Figure 3 (EQE called optimized) with the projected EQE calculated for the case of using AIGaInP, showing that a high photocurrent like in the standard case can be obtained.

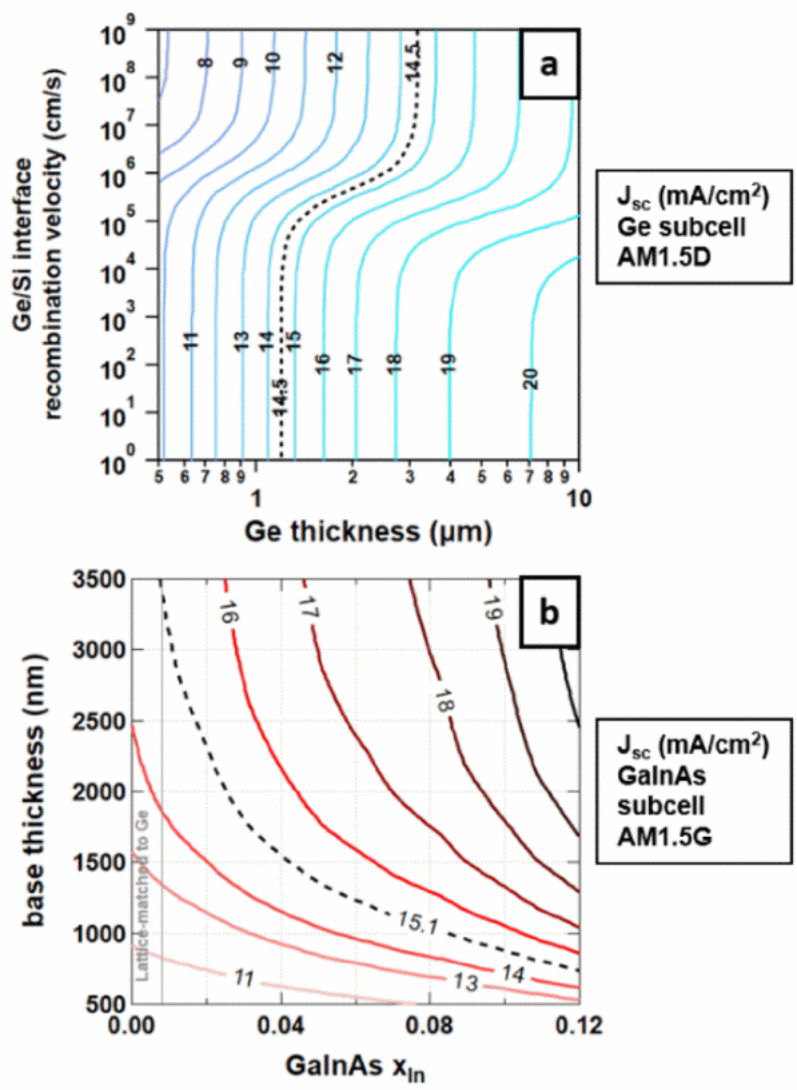

Figure 2.
Calculated contour plots for the designs using a thick Ge layer: (a) The Ge subcell Jsc vs the Ge/Si interface recombination velocity and the Ge thickness; (b) GaInAs subcell Jsc vs the indium content and the thickness (b). In each case, the black dashed contour corresponds to the Jsc of the standard design on Ge.

Concerning the voltage in these solar cell designs, Figure 4 shows the 1-sun J-V curves of the most representative devices for each case, compared to the standard design on Ge substrates. The design with the standard (thick) structure grown on Ge|Si shows the expected J_{sc} drop, due to the low collection efficiency in the GaInAs middle cell. The large V_{oc} drop observed is caused by the high TDD and cracking (see inset) in this design. The thinned design exhibits no cracking, as illustrated with the EL maps in the inset, and the effect of the TDD on the recombination current is lower, which allows a higher $V_{oc.}$ Finally, the thinned design with higher indium content shows a recovered $J_{sc,}$ although still not reaching the baseline values due to the effect of the bandgap shift in the top cell commented before. The lower bandgaps in the top and middle subcells reduce the V_{oc}, which is also affected by a higher dislocation density in the metamorphic GaInAs subcell [1].

In summary, the successive designs show the progress towards a crack-free and high-performance 3JSC. The most advanced thinned design is currently limited by the high

TDD in the Ge|Si templates used and by the non-optimized top cell. Our current efforts are focused on implementing optimized structures on lower TDD virtual substrates.

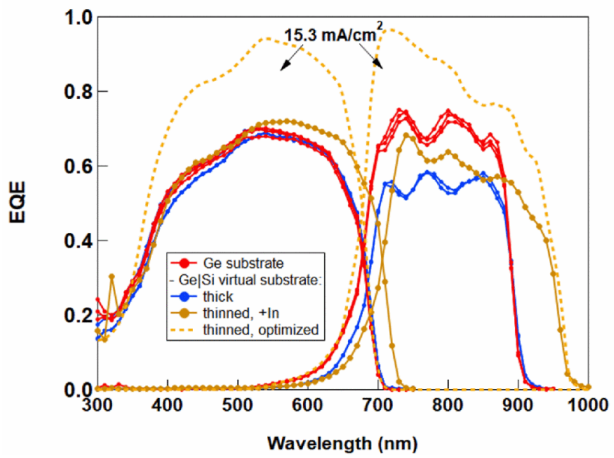

Figure 3.
EQE curve measurement of top and middle subcells of 3JSCs grown on Ge substrate and Ge|Si with different thicknesses and indium content (symbols). The dashed line is the theoretical projection of the advanced thin structure once the top cell bandgap is optimized and an ARC is used.

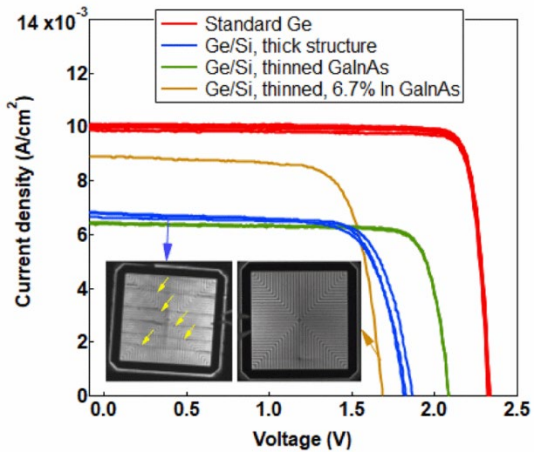

Figure 4.
(a) J-V curve measurement of 3JSCs grown on Ge substrate and Ge|Si with different thicknesses and indium content. The inset shows EL maps of cells exhibiting cracks (thick structure) and no cracks (thinned structure). Yellow arrows point to cracks.

b) GaInP/GaInAs/Ge|Si with Active Si Bottom Cell.

In this design the thickness is first reduced by using an ultrathin (20 nm) Ge layer in the Ge|Si virtual substrate. Now the bottom cell role is played by the Si substrate. The resulting configuration of subcell bandgaps requires to thin also the upper GaInP and GaInAs subcells to achieve current matching [7]. The thickness of the Ge layer, which influences the quality of the template, modifies the parasitic light absorption in this layer that determines the 3JSC design [8].

Our first experimental work aimed at demonstrating a GaInAs/Ge|Si 2JSC with an active Si bottom junction (see inset in Figure 5). The results for the 2JSC configuration with a 20-nm Ge layer are shown in Fig. 5. The EQE and J-V curves demonstrate a

functional 2JSC with no issues related to the Ge layer such as majority carrier barriers or parasitic junctions. The GaInAs EQE response is limited by a high TDD in this preliminary design. The Si bottom cell can be improved by using rear passivation and a reflector, as well as protecting the substrate from the diffusion of lifetime-killing impurities during the MOVPE process [9].

The J-V curves reveal the effect of the high TDD in the preliminary Ge|Si templates used: the V_{oc} is ~400mV lower than expected. The optimized templates under development are expected to enable a higher $V_{oc.}$ At any rate, these results demonstrate the viability of this approach based on ultra-thin Ge layers.

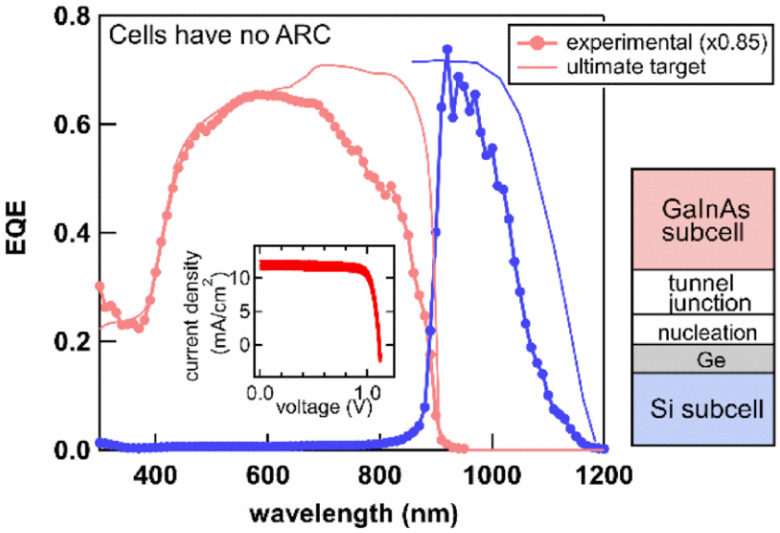

Figure 5.
EQE of GaInAs/Ge|Si 2JSC cells grown on ge|si templates with 20 nm thick Ge layers. A x0.85 factor is applied to the measurements to correct for the light trapping caused by surface roughness. The continuous line represents the target for improved material quality and a proper back reflector in the si subcell. The inset shows the uncalibrated light J-V curves.

c) Structures with Embedded Porous Silicon Layer.

The formation of cracks could also be mitigated by embedding a compliant layer in the structure [5]. This can be attained by inserting a porous Si at the Ge|Si interface of the virtual substrates under study. Previous works have attempted to achieve high-quality III-V structures by direct deposition on porous Si layers [10] or on a porous Si capped by a thin epitaxial Si layer [6]. We are investigating the formation of a compliant porous layer fabricated by anodization with a subsequent reconstruction of the surface by a thermal treatment, allowing a high-quality nucleation and growth of Ge and III-V layers on top. The geometry and density of the pores as well as the thickness of the reconstructed Si layer determine the compliance of the structure. Fig. 6 shows an advanced substrate design consisting of a porous bilayer, which enables a more efficient reconstruction of the surface that achieves an excellent morphology for epitaxial growth. In addition, we are developing surface protection methods based on electrochemical methylation, which prevent oxidation of the pore walls and facilitate an accurate structural and optical characterization of porous Si layers regardless of porosity [11]. The next steps will pursue determining the level of compliance of these structures by the formation of Ge|pSi/Si virtual templates and testing the growth of thick III-V structures on top. Mixed designs using compliant layers and thinned structures are expected to produce the best quality III-V multijunction solar cells on Si.

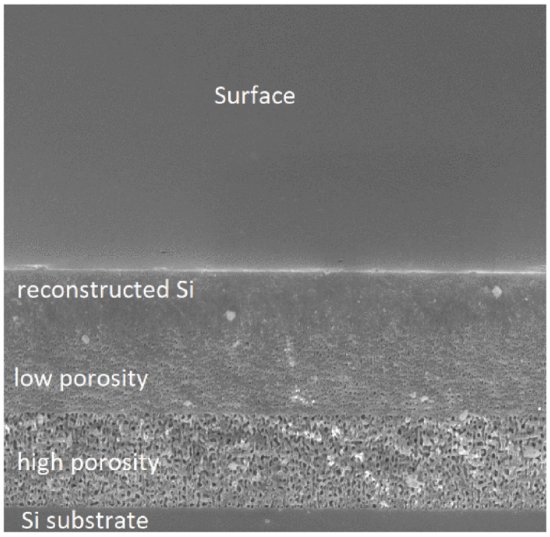

Figure 6.
Tilted cross-section (20°) of a porous Si bilayer with reconstructed surface ready for Ge deposition.

Conclusions

Two designs for the development of 3JSC on Ge|Si templates are proposed and investigated, and proof-of-concept solar cells are demonstrated. The design based on thick Ge layers acting as bottom subcell is particularly challenged by the formation of cracks. A redesign consisting of thinning the Ge layer and III-V structure is proposed and implemented, achieving a large reduction of crack formation. An alternative design based on ultra-thin Ge layers, with the Si substrate acting as bottom subcell this time, shows promise with functional solar cell devices and problems related to the intercalated ultra-thin Ge layer ruled out. In both cases, the performance obtained in the proof-of-concept devices is largely affected by the high **TDD** in the Ge|Si templates used. Better quality templates available are expected to contribute to drastic performance improvements in the ongoing developments. Finally, an advanced approach consisting of embedding a porous Si layer at the Ge|Si interface is being investigated as a means to achieve a compliant substrate to mitigate the formation of cracks. Reconstructed and smooth Si surfaces are attained by thermal annealing of the porous bilayers, ready for the application on Ge|Si virtual substrates.

ACKNOWLEDGEMENTS

This project has been funded by the Spanish Ministerio de Ciencia, Innovación y Universidades with the project RTI2018-094291-B-I00, Comunidad de Madrid with project MADRID-PV2 (S2018/EMT-4308), and the multiannual Agreement with Universidad Politécnica de Madrid in the line Stimulation of research for young doctors, in the context of the V PRICIT (Regional Programme of Research and Technological Innovation). V. Orejuela is funded by the Spanish Ministerio De Ciencia e Innovación (MICINN) through a **FPI** grant (PRE2019-088437). We also acknowledge technical support from J. Bautista and L. Cifuentes for device processing. S. Dadgostar was funded by JCYL and FEDER (Project VA283P18).

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