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Fault Ride-Through Enhancement of Grid Supporting Inverter-Based Microgrid Using Delayed Signal Cancellation Algorithm Secondary Control

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Abstract: The growing level of grid-connected renewable energy sources in the form of microgrids has made it highly imperative for grid-connected microgrids to contribute to the overall system stability. Consequently, secondary services which include the fault ride-through (FRT) capability are expected to be possessed characteristics by inverter-based microgrids. This enhances the stable operation of the main grid and sustained microgrid grid interconnection during grid faults in conformity with the emerging national grid codes. This paper proposes an effective FRT secondary control strategy to coordinate power injection during balanced and unbalanced fault conditions. This complements the primary control to form a two-layer hierarchical control structure in the microgrids. The primary level is comprised of voltage/power and current inner loops fed by a droop control. The droop control coordinates grid power-sharing amongst the voltage source inverters. When a fault occurs, the participating inverters operate to support the grid voltage, by injecting supplementary reactive power based on their droop gains. Similarly, under unbalanced voltage condition due to asymmetrical faults in the grid, the proposed secondary control ensures the positive sequence component compensation and negative and zero sequence components clearance using a delayed signal cancellation (DSC) algorithm and power electronic switched series impedance placed in-between the point of common coupling (PCC) and the main grid. While ensuring that FRT ancillary service is rendered to the main utility, the strategy proposed ensures relatively interrupted quality power is supplied to the microgrid load. Consequently, this strategy ensures the microgrid ride-through the voltage sag and supports the grid utility voltage during the period of the main utility grid fault. Results of the study are presented and discussed.

Keywords: microgrid; inverter; fault ride-through; voltage sag; delayed signal cancellation algorithm

1. Introduction

The introduction of renewable energy sources (RESs) based distributed generations (DGs) also known as distributed energy resources (DERs) into the modern electric power systems has raised significant challenges such as bidirectional power flow in the distribution system, stochastic generation nature of RESs, and distinctive fault current properties [1]. Microgrids (MG) are low-voltage mini-grids and their concept is projected years back to aggregate RESs, energy storage systems (ESS,) and loads to efficiently manage and control the DGs [2–4]. Consequently, MGs have served as a prospective platform where RESs are integrated into the modern-day distribution system with operational flexibility and controllability in either grid-dependent or autonomous modes [5]. In microgrids, controllable voltage

source inverters (VSI), are commonly used to interface various RESs such as photovoltaic (PV), wind, batteries, fuel-cells, and micro-turbines to enhance the control flexibility and ensure high quality of electric power in systems [6–9].

The system frequency, voltage, and power flow control for autonomous MG are determined by renewable energy sources. However, in grid-connected modes, the main grid imposes most of the supply standards [9]. In stand-alone operation, voltage and frequency are regulated using control schemes with multi-loop [8,10]. These control systems are usually implemented in any of these reference frames; synchronous direct-quadrature-zero coordinates, stationary alpha-beta-gamma coordinates, and natural three-phase coordinates [8,11]. In a distributed generation, inverter interfaces are typically connected in parallel [12] with appropriate power-sharing among them. Numerous control strategies have been proposed to achieve a suitable power (active and reactive) sharing, such as: average current control [13], master–slave control [14,15], and circular-chain-control [16]. A decentralized control technique frequently employed in the instance of inverters operated in parallel to avoid circulating currents is droop technique [17]. Droop control is extensively used in microgrids and relies on localized information to achieve decentralized control. This makes it a more appropriate power-sharing technique compared to various high bandwidth communication network-based techniques [6,18].

The inverter interface isolates the DGs and the wider main grid electrically; and nevertheless serves as an economical link to allow electrical energy transfer and ancillary services at the interface [19]. Several challenges are inherent owing to the sensitivity of the bidirectional flow of power between the microgrid and host utility grid [5]. In the event of voltage disturbances occasioned by faults in the host grid, studies infer the instant switching from grid-connected to islanded mode [20]. The total grid impedance up to the fault and the voltage at the point of fault occurrence have been identified in fault analysis as major factors affecting electrical faults in the grid [21,22]. The energy-generating units are expected to disconnect from the grid at the instance of voltage sags and reconnect just at the moment that the fault or disturbance is cleared. Therefore, MGs were not expected to provide additional services including low voltage or fault ride-through (LVRT/FRT) supports. Conversely, due to the growing penetration of the grid-interactive and high power capacity MGs, it is expected that they deliver a substantial quantity of power to the host grid when operational in grid synchronous mode. During fault or voltage sag, this will alleviate the potential instability by ensuring the active power delivery to local microgrid loads and reactive power support to the host grid. Avoiding the disconnection of high capacity MGs during grid fault or any disturbance forestalls potential network instabilities [23]. As a result, some developed countries have amended their respective grid codes to make provisions for rising RES capacity. Spain, Germany, and Denmark are among the foremost countries in 2004, 2006, and 2008 that already issued the FRT/LVRT requirements for DERs connected to the grid [24,25]. Spanish code requirement is displayed in Figure 1 accordingly. Even though these requirements are projected for the high-voltage grid, they are however valid for low-voltage grid due to similar concepts [18].

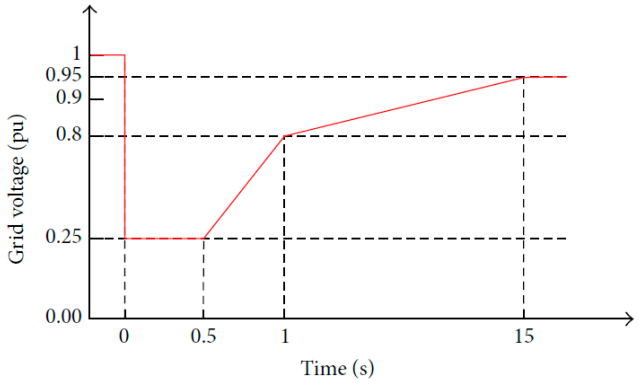

Figure 1. FRT/LVRT curves defined by Spanish grid code [26].

The power quality (PQ) of a grid-connected DG, as well as that of load connected, is degraded during the period of disturbance such as a fault in the host grid [27]. Supporting PQ schemes—such as static synchronous compensators (STATCOMs), unified power quality conditioner (UPQCs), and dynamic voltage restorers (DVRs)—have played tremendous roles in FRT capability enhancement of the of DER systems [28–30]. Similarly, several innovative FRT control strategies and schemes have been proposed in [26,31,32]. Zamani et al. [33] recommend a scheme for the control of an inverter interfaced RES for performance enhancement of the host grid during disturbances and faults. In Kou and Wei [32], certain considerations on various grid code requirements for MGs interconnection and operation were made, which recommends LVRT capabilities for MGs and provision of additional services under faults. By these recommendations, grid-connected MG is required to ride-through balanced and unbalanced sags in grid voltage as expressed in FRT voltage profile. However, interruption followed by a transition into autonomous operation is only permitted when fault persists [20]. Fault current limiters (FCLs) are utilized in minimizing the contribution to the fault current level of the DGs to improve FRT [34]. References [35,36] suggested different types and modified superconducting FCL; flux-coupling-type, resistive type to enhance the microgrids, wind turbines, solar photovoltaic and other DGs FRT capabilities. The FCL potential to enhance FRT is well established in works of literature [37,38]. FCL is positioned between a microgrid and main network and as such, overall FRT is achieved for all of the microgrid DERs [39]. A supplementary controller for voltage is suggested in [40] for the FRT control of inverters based DGs. This controller is expected to be superimposed with numerous available voltage control schemes with minimum adjustments. These modifications, therefore, do not necessarily need to alter the initial configuration of these existing controllers. Towards realizing the numerous microgrid control and operation requirements, a hierarchical control has been proposed in [41,42] with fundamental control goals which include voltage control, local power allocation among distributed energy units, frequency regulation and power control (active and reactive) under synchronization with host grid [6]. A rapid fault detection system plays a crucial role in enhancing the effects of these several strategies.

To meet the anticipated FRT requirements, control schemes and topologies for the grid-supporting MG need to be developed. This work aims at developing a secondary control scheme for the FRT/LVRT enhancement of a droop controlled grid supporting inverter-microgrids using delayed signal cancellation and stationary reference frame control for the reactive power injection and fault current limitation. To satisfy numerous requisites of operation and control in a microgrid, the secondary LVRT control stipulates set-points for the primary control that consists of the droop, power and current loops. These two levels form a hierarchical control structure. The strategy requires no mode switching and enables the inverter-interfaced MG to ride through faults or transient disturbances on the host utility grid. The need for resynchronization of microgrid with the main grid as proposed in seamless transition method [43–46] after fault clearance is completely unnecessary and shedding of local loads is avoided. In a grid supporting system, the active and reactive power is controlled to meet local load requirement and the surplus MG power is simultaneously delivered to the main grid. Active power and reactive power are controlled through frequency regulation and voltage regulation respectively, such that local power-sharing among constituent inverters is not compromised in any way.

Acceptable power quality for the local loads during fault duration is ensured with the inclusion of a properly sized anti-parallel IGBT-diode switched inductance. It is noteworthy that as a result of high R/X ratio in low voltage distribution feeder line, injecting reactive power under faults may not substantially contribute to the recovery of voltage. Hence this work has been able to deploy a properly sized anti-parallel IGBT-diode switched inductance at the PCC of the MG with the grid to reduce R/X ratio and effectively support the voltage under grid disturbance. This provides protection and alleviates the effects of fault especially on the local sensitive loads of the microgrid. Consequently, a direct theoretical framework has been provided for the determination of the value of this switched inductance. Furthermore, this arrangement counteracts the effect of grid disturbances by limiting transient overcurrent throughout grid faults. This is enhanced by the introduction of a secondary

control block that regulates the active power and reactive power exchange between the host grid and the microgrid in conformity with the stipulated utility grid standard.

To ensure the efficient and prompt responsiveness, a fault detection procedure built on a delayed signal cancellation (DSC) algorithm is implemented to detect the fault instantly in less than 0.05 s. The DSC algorithms apply the concept of PLL and therefore enhanced with fast detection of the positive sequence and negative sequences [47–49]. In [40], an LVRT strategy is proposed which implements the wavelet-based fault detection technique as given in [50,51]. The voltage disturbance detection method based on wavelet transform can detect the faults within 3.12 ms. The DSC technique is efficient for faster convergence and detects faults within 0.1515 ms under various unbalanced voltage conditions has been validated in several works of literature [52–55] using simulations and experiments. DSC determines the fault interval at which active and reactive power references are adjusted appropriately. Lastly, DSC is used in giving adequate information for the control of the PCC voltage and this ensures quality power delivery to the microgrid loads irrespective of the transients on the main grid. The simulation results reveal the performance and effectiveness of the proposed scheme in enhancing LVRT/FRT requirements of Spanish code.

The rest of this paper is organized thus: Section 2 presents the modelling of a grid supporting MG system whose aim is to actively partake in grid voltage and frequency regulations via the control of active power and reactive power supplied to the AC grid; Section 3 describes the proposed secondary FRT control of voltage with the description of DSC; Section 4 discusses the power flow in a grid support system and presents the how to determine the value of IGBT-diode switched reactor; and Section 5 shows the detailed results of simulation of the proposed strategies under symmetrical disturbance and asymmetrical disturbance on the grid.

2. Grid Supporting Microgrid Modeling

The grid-supporting inverter fits the control and hardware topology most typical of three-phase VSI utilized in interfacing numerous DERs. It is intended to fill a variety of roles and can export power at any specified power factor, when connected to weak grids, stiff grids and to a low-inertia RES dominated microgrid. Figure 2 is a grid-interactive inverter system whose output is connected to a stiff host grid. Its model can be derived in a synchronously rotating reference frame by using the PLL phase angle. The innermost loop controls the filter inductor current, following current references and removing cross-coupled terms caused by the reference frame transformation. The outer loop specifies the current references corresponding to required or specified active power and reactive power references. The VSI and the LC filter constitute the power processing unit. The output is interfaced to the grid via the LC filters where the L is the coupling inductor with C as the shunt capacitor. The entire system reference is the common reference frame where the dynamics of each constituent generating unit are transformed using the angular frequency ω. Subsequently, the decoupling of the active and reactive power is done through Park transformation (*abc-dq*).

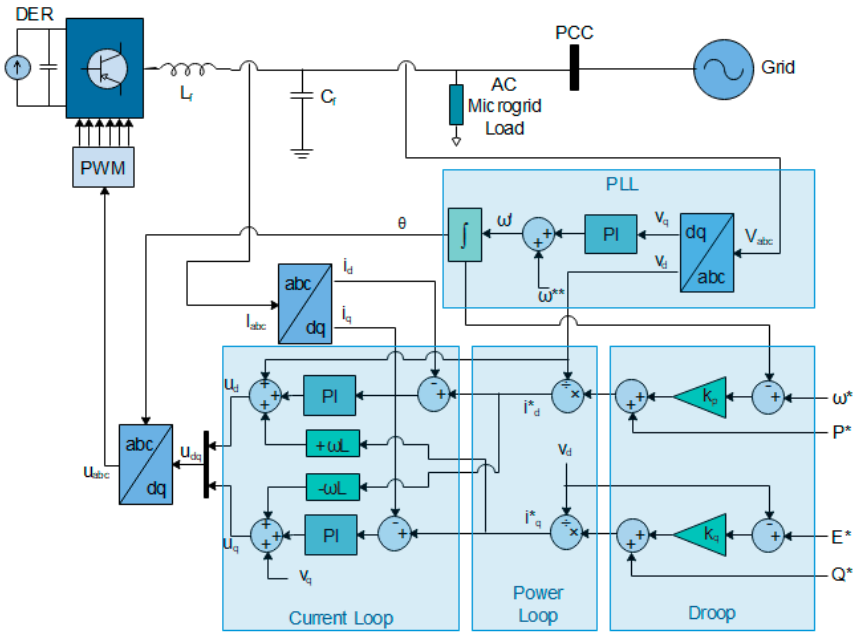

Figure 2. Grid-connected inverter interfaced DER primary control consisting droop, voltage, and current control loops.

2.1. Output LC Filter

The two most widely used passive filters are the LC and LCL filters. LC filters are deployed in a situation where a local load exists between the inverter and the host grid while the latter is employed where there is nonexistence of local loads [56]. The LC filter attenuates the output voltage ripple and limits the high-frequency ripple current of power electronic switches [57]. The LC filter circuit equations are derived from the synchronous reference frame. Figure 2 shows filter inductance L_f and shunt capacitance C_f. The grid impedance or transformer leakage inductance or both serve as coupling inductor [58]. The LC filter arrangement depicted is used for the grid-connected inverter with local load in between. This work focuses on the parallel operation of inverter-based microgrid with a local load while in grid supporting mode. Consequently, the LC filter is used in inverter output considering the presence grid impedance between the microgrid and the host grid. The cut-off frequency f_c of the LC filter is given by

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

The voltage/power loop and current control loop are designed in such a way to eliminate high frequencies as a result of disturbances by providing adequate damping for the output LC filter [9].

2.2. Grid Synchronization

The AC grid voltage parameters; voltage magnitude, grid frequency, and phase angle of an inverter-based MG are key to accurate and dynamic control of active power and reactive power injected. Therefore, a precise estimation of these aforementioned parameters has a significant effect on the inverter general performance. Furthermore, continuous parameter sampling and AC grid condition monitoring are required to dynamically decide the appropriate and optimal mode of operation. The inverter-based microgrid synchronization using PLL ensures appropriate response during normal and abnormal AC main grid condition [10]. The phase angle and frequency of the main grid is closely tracked by the synchronous reference frame PLL using Equation (2).

$$T_{abc-dq} = \begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ \sin(\omega t) & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2}$$

Equation (2) transforms a three-phase instantaneous voltage from the natural *abc* reference frame to a rotating synchronous *dq* reference frame by Park (*abc-dq*) transformation. In the *dq* reference frame, the Equation (3) shows an angular position, which is regulated via the feedback loop driving the voltage quadrature component v_q to zero.

$$\theta' = \int \omega' = \int \left(\omega * + \left(k_p + \frac{k_i}{s} \right) \times v_q \right) \tag{3}$$

By the synchronization arrangement, ω' is estimated frequency of the AC grid while the rated reference frequency ω* signifies PLL's feed-forward which enhances the phase estimation θ' dynamics and this is achieved by integrating ω'.

2.3. Primary Control

Different microgrids with a wide-ranging array of operation and control objectives; grid-forming, grid-feeding, grid-supporting, require sets of well-coordinated and designed control schemes to guarantee effectual operation especially in the dynamic state [10]. The power-sharing, voltage/power, and current controllers locally regulate the output variables of the inverter with high-performance bandwidth to ensure prompt response time in a dynamic state. In the hierarchical control architecture, these three different loops all constitute primary control level that ensures microgrid stability.

The focal objective of the primary level of control is controlling the active power and reactive power interaction and export between DERs and host AC grid as voltage sources being controlled by the current [59]. The positive sequence control loops regulate the active power contributed by every constituent inverter interfaced DER. This active power supply is maximized under a symmetrical grid situation subject to the available active power potential in case of RES-based DG system. However, under asymmetrical grid voltage situations, the negative and zero sequence control loops regulate the reactive power delivery. DGs supply the obtainable active power from the maximum power tracking system in normal grid conditions. A percentage of total active power generated, together with the entire reactive power, is supplied to meet microgrid load demand, while the remaining percentage of the active power generated is directly provided to the main utility grid consumption.

2.3.1. Droop-Based Power Control

The effective distribution and allocation of required power among the inverter-based DERs of a given microgrid is implemented by a droop control scheme. Droop emulates frequency and voltage regulation of a typical synchronous generator at the inverter output. Several power sharing control schemes—such as average current-sharing, master–slave, and droop—have been significantly employed to control parallel-connected inverter-based DERs. In microgrids, parallel-connection of inverters are known to improve the overall performance and reliability even with the failure of a constituent parallel inverter [60–62]. Propitiously, droop controls have been generally acknowledged as the most effective power-sharing scheme due to flexibility and nonexistence of significant communication networks between parallel-connected inverters [17,63]. Furthermore, various techniques have also been proposed in the literature to improve the performance of droop and grid-connected inverters at high RES penetration [64,65]. The injected active power by a particular constituent inverter into a reference bus is largely dependent on α which denotes angle of power. However, reactive power is significantly influenced by the voltage amplitude [17]. The droop characteristics equations of both frequency and voltage as they relate to the active power and reactive power respectively are written as

$$\begin{aligned} \omega &= \omega^* - k_p(P^* - P_m) \\ E &= E^* - k_q(Q^* - Q_m) \end{aligned} \tag{4}$$

where k_p and k_q are the coefficients of the frequency and voltage droops of the inverter, respectively. Similarly, P* and Q* are active and reactive power references, respectively. Furthermore, the measured

output of active power and reactive power are signified by P_m and Q_m, respectively. Also, ω^* signifies the set-point frequency while E^* is the rated set-point amplitude of the voltage. Hence, voltage magnitude and frequency are set by the coefficients of the voltage and frequency droops specified for the active power and reactive power. In Equation (4), droop control shares every load change among inverters by adjusting the frequency by the specified coefficient of frequency-active power droop. In a grid-supporting VSI, the measured active power and reactive power P_m and Q_m at any point in time are computed using the measured output three-phase current and voltage transformed to the equivalent direct-quadrature components as depicted in Equation (5) at the fundamental frequency of ω^*

$$\begin{aligned} P_m &= \tfrac{3}{2}\left(v_d i_d + v_q i_q\right) \\ Q_m &= \tfrac{3}{2}\left(v_d i_q - v_q i_d\right) \end{aligned} \tag{5}$$

With the frequency droop gain, the frequency is determined and integrated for setting the phase. Therefore, the dynamic features and inertia characteristics of conventional generators are mimicked with incorporated negative feedback. Similarly, with a voltage droop gain, the voltage magnitude is determined which is equivalent to a d-axis output voltage reference. In other words, the control ensures the magnitude reference of the output voltage is in line with the d-axis voltage component of the reference frame while zero voltage q-axis component reference is maintained [9].

2.3.2. Power/Voltage Loop Control

Both loops for voltage/power and current regulation are used to set the final reference for the voltage used as the input of the pulse width modulation (PWM) of the VSI. The PLL stipulates the reference voltages (v^*_d and v^*_q) of direct-quadrature axes based on its synchronization with the grid. Consequently, the voltage/power loop control uses the v^*_d and v^*_q to generates the references currents (i^*_d and i^*_q) for the direct-quadrature axes components using the measured active power and reactive power as given in the Equations (4) and (5) and shown in Figure 2. This control can also be realized with a PI control scheme such that the controller output is given by

$$\begin{aligned} i^*_d &= \left(k_{pv} + \tfrac{k_{iv}}{s}\right)\left[v^*_d - v_d - v_{dp}\right] \\ i^*_d &= \left(k_{pv} + \tfrac{k_{iv}}{s}\right)\left[v^*_d - v_q - v_{dp}\right] \end{aligned} \tag{6}$$

where k_{IV} and k_{PV} are the integral gain and proportional gain of the voltage PI control respectively. The v_{dp} is the drop in voltage due to the grid or virtual impedance.

However, in a grid supporting VSI that operates in the role of a typical current source, the voltage control loop is regarded as power control loop such that the references, i^*_d and i^*_q, generated are computed using the output of the droop power-sharing P_m and Q_m such that

$$\begin{aligned} i^*_d &= \tfrac{2}{3}\tfrac{P_m}{v^*_d} \\ i^*_q &= -\tfrac{2}{3}\tfrac{Q_m}{v^*_q} \end{aligned} \tag{7}$$

In the absence of any disturbance or fault at the AC side of the VSI, this control loop regulates the active and reactive power to ensure the transfer of power from DC to AC side of the VSI. Under this balanced voltage condition, the voltage v_d is constant and the active power is regulated by adjusting the current i_d. Similarly, the reactive power regulated through the current i_q control. Therefore, the active power and reactive power transferred to the AC side is determined by making P_m and Q_m the subjects of the formulas in terms of stationary quantities in Equation (7) [66].

2.3.3. Current Loop Control

Loops for voltage/power and current regulation simultaneously play the roles of setting the final reference for the voltage used as the input of the PWM of the VSI. Furthermore, according to the

current references, i^*_d and i^*_q, generated by the loop of voltage control, the loop of current control generates reference voltage (u_d and u_q) of direct-quadrature-axes for the PWM. This control is realized using a PI controller such that the controller output is expressed as

$$\begin{aligned} u_d &= \left(k_{pi} + \frac{k_{ii}}{s}\right)\left[i^*_d - i_d\right] + v_d + (\omega L) \times i^*_q \\ u_q &= \left(k_{pi} + \frac{k_{ii}}{s}\right)\left[i^*_q - i_q\right] + v_q - (\omega L) \times i^*_d \end{aligned} \tag{8}$$

where k_{ii} and k_{pi} denote integral and proportional gains of the current control loop respectively. The direct-quadrature axes components v_d and v_q of the voltage signify the feed-forward quantities while $+(\omega L)i^*_q$ and $-(\omega L)i^*_d$ signify the cross decoupled quantities. The feed-forward and cross decoupled quantities are employed to accomplish independent d–q axis current controls. Lastly, L in the cross-decoupled quantities is the output filter inductor.

3. Proposed LVRT/FRT Scheme

Faults are usually unbalanced and the grid codes are less strict in asymmetrical fault cases (phase to ground and line to line) unlike strict regulations imposed under the symmetrical (three-phase) disturbance. However, certain limitations are imposed which include the prohibition of the grid absorption of both active power and reactive power in the event of fault as stipulated by the Spanish P.O.12.3 document [67,68]. Consequently, the unbalance in the grid can be promptly eliminated alongside current limiting by inhibiting grid active power absorption and supporting grid voltage recovery by contributing an appropriate reactive current. The microgrid topology used for the purpose of this paper is shown in Figure 3.

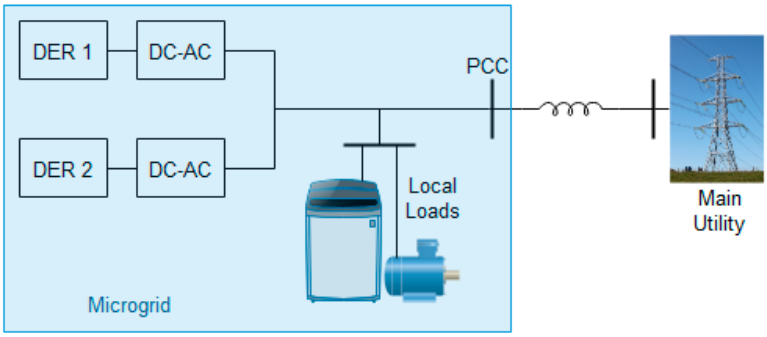

Figure 3. Topology of the MG examined.

3.1. Secondary Voltage Control

This study uses Spanish grid code guidelines [26,69] in developing the FRT/LVRT secondary control. These documents released by the government stipulates that grid-connected DGs should ride-through at least 0.2 pu grid voltage drop lasting for 500 milliseconds. However, these DER are permitted to disconnect from the grid when the voltage drops versus the time are outside the FRT curve. Moreover, DERs are demanded to inject a stipulated reactive power quantity defined by the reactive power support capability to support voltage sag as depicted in Figure 4. However, an insignificant amount of reactive power support is expected during voltage sag that falls above 90%. In essence, the Spanish grid code specifies a certain amount of reactive current/power (per unit) injection based on the percentage voltage drop. Equation (9) clearly explains the aforementioned side by side with Figure 5.

$$Q_{ref} = \begin{cases} \left(\frac{93}{70} - \frac{6}{7} \cdot \frac{V_g}{V_N}\right) Q_N, & V_g \le 0.5 V_N \\ \left(\frac{57}{100} - 6 \cdot \frac{V_g}{V_N}\right) \cdot Q_N, & 0.9 V_N \ge V_g > 0.5 V_N, \\ \left(1 - \frac{1}{5} \cdot \frac{V_g}{V_N}\right) \cdot Q_N, & V_g > 0.9 V_N \end{cases} \tag{9}$$

where V_N signifies the rated grid voltage at nominal value, reactive power Q_N corresponds to the rated reactive current of the inverter and reactive power reference Q_{ref} corresponds to the required reactive current that will be injected of the microgrid. The reference required signal of reactive current is obtained in the same degree with the depth of voltage sag on the grid, through the proposed secondary control loop. Once this voltage falls below 0.9 of the nominal value, the secondary control scheme will instantly commence reactive current/power support as shown in the Equation (9). The injection of reactive power/current is systematically regulated to ensure the restoration of voltage above 0.9 of the nominal value, instead of exactly 0.9 V_N. The immediate detection of faults in systems is crucial in enhancing the overall reliability, productivity, and safety, hence the Clarke transformation of the measured grid voltage is done using Equation (9) and shown in Figure 4. The magnitude is conditioned using a first-order low pass filter and subsequently monitored. The essence of this is to prevent and unnecessary activation of the anti-parallel IGBT-diode switching arrangement for the inductance. With this, fault occurrence and clearance are detected with 0.05 s as shown in the results.

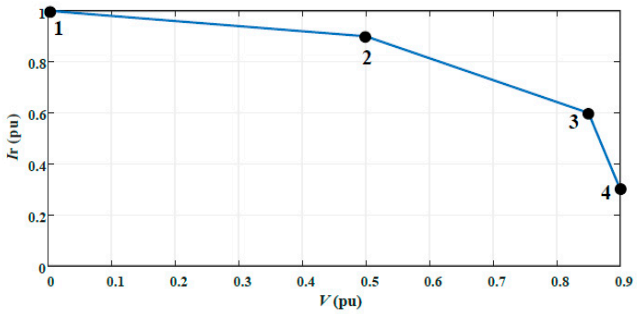

Figure 4. Reactive currents injection/absorbed during faults, according to Spanish network code P.O. 12.2 Spanish grid code requirements [45].

3.2. DSC Algorithm for Unbalance Detection and PCC Voltage

To avoid exceeding the limit, the PCC voltage magnitude control is put in place to buffer and avoid exceeding the limit of grid code prescript and acceptable range (0.9–1.1 pu). The values of its symmetrical components are obtained to implement an effective unbalanced grid voltage compensation. Towards actualizing the aforementioned, delayed signal cancellation (DSC) as depicted in Figure 5, is deployed to detect the presence of symmetrical components and obtain their values accordingly.

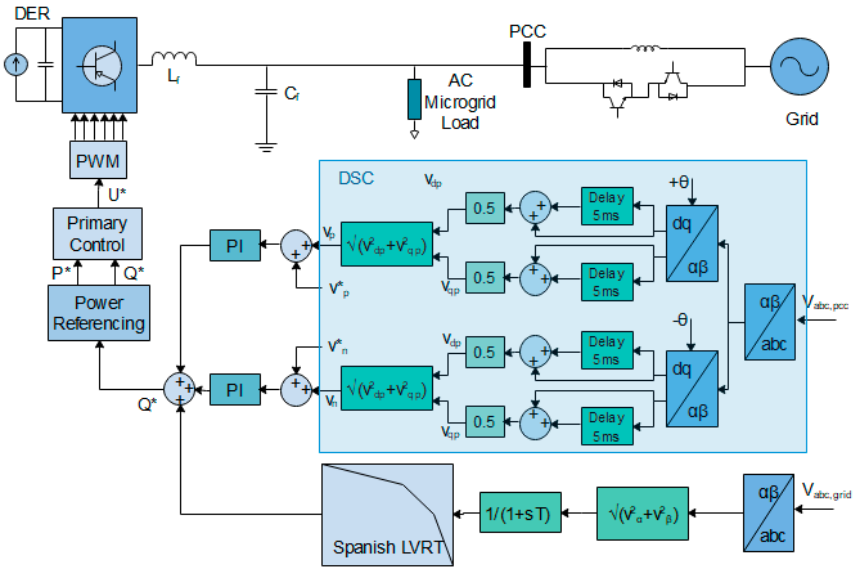

Figure 5. Proposed FRT control scheme.

The algorithm for DSC is centered on the three-phase voltage measurement and subsequent decomposition into their commensurate symmetrical components [66]. Primarily, the voltages measured in phase are denoted in stationary reference frame using the Clarke (*abc*-$\alpha\beta$) transformation.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \frac{\sqrt{3}}{3} & -\frac{\sqrt{3}}{3} \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{10}$$

In line with the resultant stationary reference frame above, two opposite rotations are executed using the phasor measured angle of the host grid voltage (θ and $-\theta$). This angle θ matches the same provided at the output of the phase-locked loop.

The positive component implies

$$\begin{bmatrix} v_{dp} \\ v_{qp} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{11}$$

The negative component implies

$$\begin{bmatrix} v_{dn} \\ v_{qn} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{12}$$

The values obtained for v_{qp} and v_{qn} are subsequently kept for half a period in two independent data buffers. Lastly, the positive component and negative component final samples are obtained and immediately kept in the two buffers at a time equivalent to half a period. The components and their additions are expressed in Equations (13)–(16):

The positive component implies

$$v_{dp}(k) = \frac{1}{2} \cdot \left[v_{dp}(k) + j \cdot v_{dp}\left(k - \frac{f_s}{4 \cdot f_g} \right) \right] \tag{13}$$

$$v_{qp}(k) = \frac{1}{2} \cdot \left[v_{qp}(k) + j \cdot v_{qp}\left(k - \frac{f_s}{4 \cdot f_g} \right) \right] \tag{14}$$

The negative component implies

$$v_{dn}(k) = \frac{1}{2} \cdot \left[v_{dn}(k) + j \cdot v_{dn}\left(k - \frac{f_s}{4 \cdot f_g} \right) \right] \tag{15}$$

$$v_{qn}(k) = \frac{1}{2} \cdot \left[v_{qn}(k) + j \cdot v_{qn}\left(k - \frac{f_s}{4 \cdot f_g} \right) \right] \tag{16}$$

The second term samples in Equations (13)–(16) are equivalent to the first term components and however, they are shifted a fourth of period and this shifting is depicted by j multiple of the second terms. Once the sequence components of the PCC voltage are obtained in direct-quadrature coordinates at the instance of grid fault using Equations (13)–(16), the two PCC voltage-independent control system operates to restore to normal sequence references. Positive sequence control aims to bring back the PCC voltage positive sequence level to its rated value. Hence, the error, in this case, is utilized in regulating the reactive power Q_p injected into the grid while considering power electronic switch thresholds. Similarly, the PCC voltage negative sequence control restores quadrature component to the zero references of normal condition. This balances and buffers the further PCC voltage unbalance introduced through reactive power injection into the grid.

The microgrid voltage at the local load point of connection with the PCC is therefore controlled by the control scheme using the DSC to independently adjust both positive component and negative component in conformity with their respective sequence references. Thus, the microgrid voltage for

the DERs and local sensitive loads relatively enhanced regardless of the voltage sag experienced in the main grid. Therefore, active power is uninterruptedly delivered to the microgrid sensitive load while delivering ancillary voltage support service to the main grid. The independent controls of the voltage at the point of common coupling of the microgrid to the main grid is expressed in the Equation (17).

$$\begin{aligned} Q_p &= \left(k_{pp} + \frac{k_{ip}}{s}\right)\left[v_p^* - \sqrt{v_{dp}^2 + v_{qp}^2}\right] \\ Q_n &= \left(k_{pn} + \frac{k_{in}}{s}\right)\left[v_n^* - \sqrt{v_{dn}^2 + v_{qn}^2}\right] \end{aligned} \tag{17}$$

The aggregate reactive power injection from the microgrid through the PCC to the utility grid for ride-through and reactive power support implies

$$\Delta Q = Q_p + Q_n + Q_{req} \tag{18}$$

4. Power Flow and Switched Reactor

4.1. Voltage Source Inverter and Grid Interactive Power Flow

In inverter grid supporting mode, there is power interaction with host grid which involves power exchange. The equivalent power flow diagram between the inverter-based microgrid and the host grid is shown in Figure 6, where v_i signifies the VSI voltage and v_g represents the grid voltage. Similarly, the inherent impedances of the inverter and its filter circuit are lumped together as Z_i while the grid impedance is represented as Z_g. The load current and impedance are signified by I_L and Z_L. These aforementioned impedances are typically inductive owing to the significant output inductance of the VSI. Nevertheless, this inverter impedance can be greatly influenced by the type of control strategy employed [70], and grid impedance is highly resistive in low-voltage distribution feeder lines [71]. Similarly, the impedance (resistance and inductive reactance) of the grid is significantly present and taken into consideration in microgrids located at a long distance away far from the host grid. Consequently, this work put into consideration the line impedance of the grid. In line with the stipulation of the grid codes, only reactive current is injected all through the period of voltage sag. Consequently, the resulting compensating voltage is relatively in phase with the grid voltage.

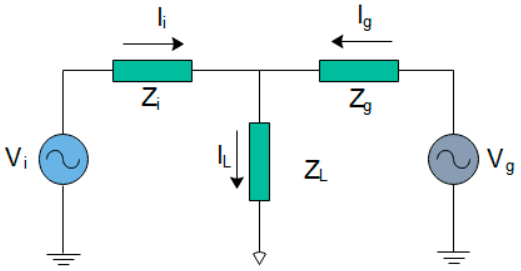

Figure 6. Power flow diagram between the inverter and host grid.

4.2. Switched Inductance: Sizing and Switching

A microgrid is to ensure required uninterrupted supply of quality power to the local sensitive loads besides fulfilling FRT requirement of reactive power support in the event of disturbance on the main grid. In this work, this is ensured by ascertaining that all the sections in the microgrid are supplied with a constant voltage at a regular frequency. The proposed scheme in Figure 5 shows the implementation of this requirement through an additional reactive power injection. The VSI injects a significantly high amount of reactive power in supporting the utility grid and sustain microgrid load voltages since the grid impedance is usually low [72]. However, the aforementioned secondary control based LVRT schemes are significantly limited in voltage sag compensation. To tackle this problem, a PCC voltage moderation scheme based on PI control using the DSC positive and negative

is introduced. Furthermore, under a strong (stiff) main grid connection, independent control of the point of common coupling voltage and by extension microgrid voltage is not sufficient for good power quality since the host grid imposes the voltage. Thus, control strategies may not be able to effectively restore the network voltage especially at the PCC [73,74]. Hence, a switched inductance is inserted in series at the PCC to the main network during a voltage disturbance to increase the network impedance to independently regulate the microgrid voltage irrespective of the host grid condition. Thus, sustaining the PCC voltage at the rated magnitude.

The appropriate sizing and switching of this inductance ensure sustained microgrid voltage irrespective of a host grid disturbance. The inductance size is estimated in relation to the voltage sag in the worst-case scenario which must be compensated at PCC. It also depends on the expected current flow through the inductance under voltage sag. The balance between microgrid generated power (active and reactive) and the local load consumption determines the current flow (magnitude and phase angle) through the inductance during grid disturbance. In the proposed strategy of this work, during the grid fault, the total microgrid generated active power is commensurate with the rated local load capacity to limit the amplitude of the current flow into the main grid. However, excess active power may still be supplied to the main grid due to varying load demand and this affects the inductance size. To estimate required value for the series inductance, the load demand is assumed to be zero and the rated load power is assumed generated and supplied to the host grid. The phasor diagram of this estimation is presented in Figure 7, where V_g represents the phase voltage of the host grid, V_{mg} represents phase voltage within the microgrid. Similarly, X_n signifies needed switched inductive reactance while I_n signifies current flow across X_n. The inverter voltage is therefore given by

$$V_{in}^2 = (I_i X_n \cos\theta)^2 + \left(V_{mg} + I_i X_n \sin\theta\right)^2 \tag{19}$$

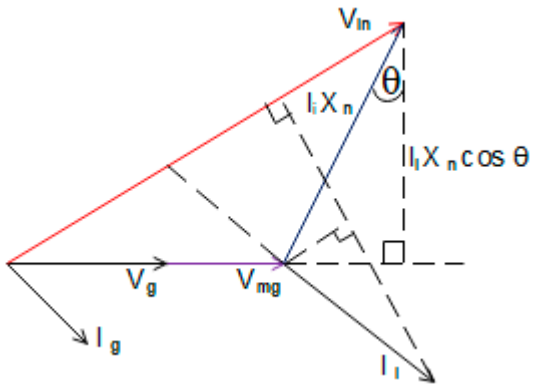

Figure 7. Phasor diagram of reactive current injection under transient condition.

Consequently, the value of the series inductance is determined by solving the quadratic equation generated by making the X_n the subject of the formula in Equation (18). It is therefore given as

$$X_n^2 + \left[\frac{2V_{mg}\sin\theta}{I_i}\right]X_n + \left[\frac{V_{mg}^2 - V_{in}^2}{I_i^2}\right] = 0 \tag{20}$$

The inverter current I_i is in phase with the current flowing through the switched inductance X_n, hence angle θ is calculated from

$$\theta = \cos^{-1}\left[\frac{P_{rated}}{S_{\max}}\right] = \cos^{-1}\left[\frac{I_d}{\sqrt{I_d^2 + I_q^2}}\right] \tag{21}$$

In a typical low voltage distribution lines, the resistive component (R) is high [10,75] and therefore the R/X ratio is considerably reduced with series incorporation of a comparatively sizable inductance. Hence, the addition of an extra inductance may cause a depreciation in voltage regulation, particularly within the microgrid. Therefore, the inductance is only inserted during a main grid voltage disturbance by the operation of the anti-parallel IGBT-diode switches in Figure 5. A fault condition or disturbance leading to voltage sag at the grid is detected by the fault detection. This simultaneously generates alternating pulses for the switching on of the anti-parallel switches and uses the Clark transformation in detecting fault using a low pass filter. Then the switching pulses are off once a fault is detected and the voltage sag is observed in 0.0001515 s. Thus, the inductive reactance is introduced swiftly devoid of any adverse influence on the effectiveness of the FRT control strategy.

4.3. Active Power Referencing and Fault Current Limiting

In a grid supporting inverter without a local load, the active power set-point is zero under fault for effective limiting the active current magnitude and jack up the reactive current within the apparent power limit. This by extension limits the fault current observed at the PCC. However, under normal operating conditions, maximum power point tracking (MPPT) output imposes the active power reference instantaneously at a 100 per cent power factor. The presence of disturbance within the host grid thereby leading to voltage sag or swell causes the reactive power reference to be evaluated based on

$$Q^*_{new} = Q^* + \Delta Q \tag{22}$$

where Q^* represents the reference of the reactive power of the inverter before voltage sag and ΔQ already specified in Equation (17). By the control strategy proposed, the reactive power needed is commensurate to the depth of percentage voltage drop. Consequently, the active power and the reactive power generated from the DER and injected through inverter must be realistic such that it conforms to the complex power equation as well as preventing inverter overloading. The grid codes stipulate grid reactive power support by all connected generating units however, it is also important inverter ensure a continuous supply of active power to the microgrid sensitive load irrespective of grid conditions. Therefore, due to the reactive power (current) injection, the active power (current) injection is limited. Thus, the reference P^* for the inverter active power is computed using the Equations (23).

$$P^* = \begin{cases} \sqrt{(S^*_{\max})^2 - (Q^*_{new})^2} & if \quad \sqrt{(P^*)^2 + (Q^*_{new})^2} > S_{rated} \\ P^* & else \end{cases} \tag{23}$$

where P^* signifies the active power reference of the inverter before voltage sag and S_{rated} represents the maximum tolerance in which the active reference limit triggers and S_{max} represents the inverter maximum complex power specified by the manufacturer. The maximum complex power confines the references of active power and reactive power within its value as shown in Equation (23).

5. Results and Discussions

The effectiveness of this FRT approach proposed is investigated on a grid-connected microgrid system consisting of two DERs and local load, as depicted in Figure 2. Various types of faults are simulated on the main grid and are switched on at time t = 1.3 s and assumed to be automatically cleared at t = 1.8 s. The common types of power system faults are the triple-phase to ground (L-L-L-G), double line to ground (L-L-G), single line to ground (L-G), and line-to-line faults (L-L). These faults lead to different degrees and types of voltage sag within the grid and at the PCC of grid supporting microgrids. In simulating the grid faults, the fault resistances of 0.7 Ω, 0.5 Ω, and 0.3 Ω are used to produce 70%, 60%, and 50% voltage sags at constant ground resistance of 0.001 Ω and snubber resistance of 1000 Ω. The simulations were performed in MATLAB/Simulink/SimPower software. Two inverter-based distributed energy resources DER 1 and DER 2 are used to form microgrid energy

sources. DERs 1 and 2 feed a local microgrid load of 10 kW with a power factor of 0.90. The excess power generated in the microgrid by these DERs is distributed into the main utility grid while the DERs also participate in the frequency and voltage regulations through their respective droops in the primary control. Installed at the PCC is a step-up transformer of 0.400/11 kV phase to phase rms through which the excess generation is supplied to the host grid. The other parameters used in the simulations are shown in Tables 1–4.

Table 1. Inverter electrical parameters.

Parameters	Descriptions	Values
kVA_1	DER 1 rated power	12 kVA
kVA_2	DER 2 rated power	6 kVA
V_{abc}	Voltage (phase-phase)	400 V
V_{dc}	DC bus voltage	1100 V
f	Frequency	50 Hz
C	LC filter capacitance	2.31 µF
L	LC filter inductance	11 mH

Table 2. Inverter primary and secondary control parameters.

Parameters	Descriptions	Values
ω_{cut}	Cut-off angular frequency	100π
E	Single-phase voltage reference	330 V
$K_{p\,I}$	Direct-quadrature current loop P gain	100
$K_{i\,I}$	Direct-quadrature current loop I gain	1000
$K_{p\,PCC+-}$	Positive sequence and negative sequence P gain	0.0125
$K_{i\,PCC+-}$	Positive sequence and negative sequence I gain	2

Table 3. Grid synchronization and parameters.

Parameters	Descriptions	Values
f_{min}	PLL minimum frequency	45 Hz
$K_{p\,PLL}$	Regulator P gain	180
$K_{i\,PLL}$	Regulator I gain	3200
$K_{d\,PLL}$	Regulator D gain	1

Table 4. Switched IGBT-diode inductance parameters.

Parameters	Descriptions	Values
L_r	Reactor inductance	0.005
R_{on}	Switch internal resistance	0.001
R_s	Switch snubber resistance	0.00001

The DER inverters are modeled in detailed states and selection of control parameters done by SimScape closed-loop auto-tuner which computes a linearized approximation of the nonlinear dynamic system models. Figure 8 below gives the responses of the model while putting into consideration the dynamics of the inner power/voltage control loop, current control loop, and detailed model parameters. The power set points of the modelled grid-supporting systems are changed in three steps at times 1.0 s and 1.5 s. These values are 4 kVA, 12 kVA, and 20 kVA at unity power factor to validate the response of inverter and portray typical grid supporting system. The corresponding dynamic responses in active power, voltage, current, and frequency are shown to validate the detailed model used in the simulation. The strategy implemented in the simulations can be deployed for low voltage ride-through of a solar PV based grid-connected microgrids and can be used for the interface FRT control of large scale grid-connected battery energy storage systems.

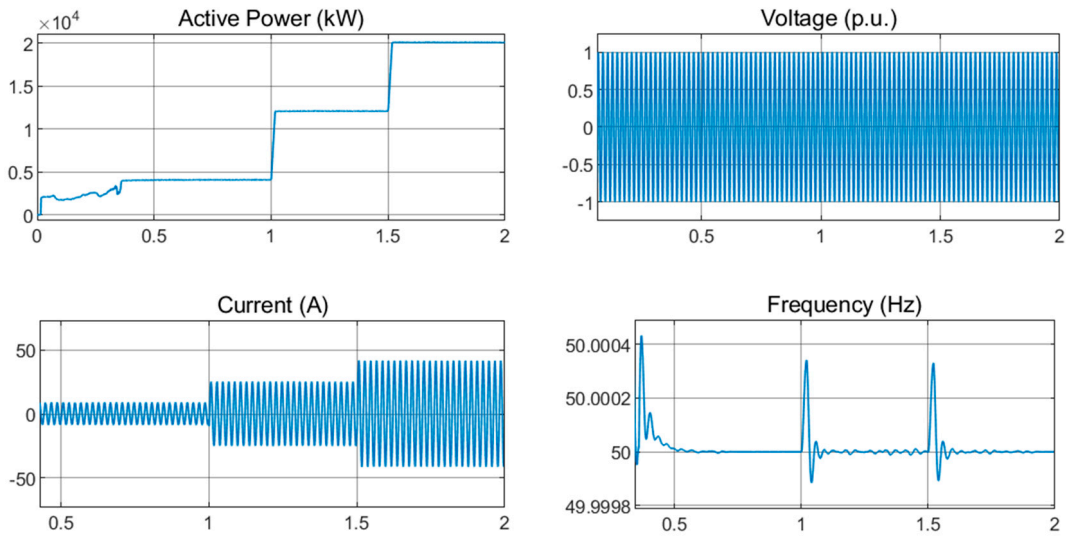

Figure 8. DER active power, voltage, current, and frequency under changing power set-points.

5.1. Symmetrical Fault

Figure 9 shows the pulses generated in each of the phases for the control of the IGBT-diode switches. This shows that the fault is detected within 0.0001515 s in all phases for the activation of the FRT scheme and of course the switching of the inductor. These pulses activate the switching operation of the IGBT-diode-based switch and properly change the operating mode of the switching control system at fault inception and fault clearing instants.

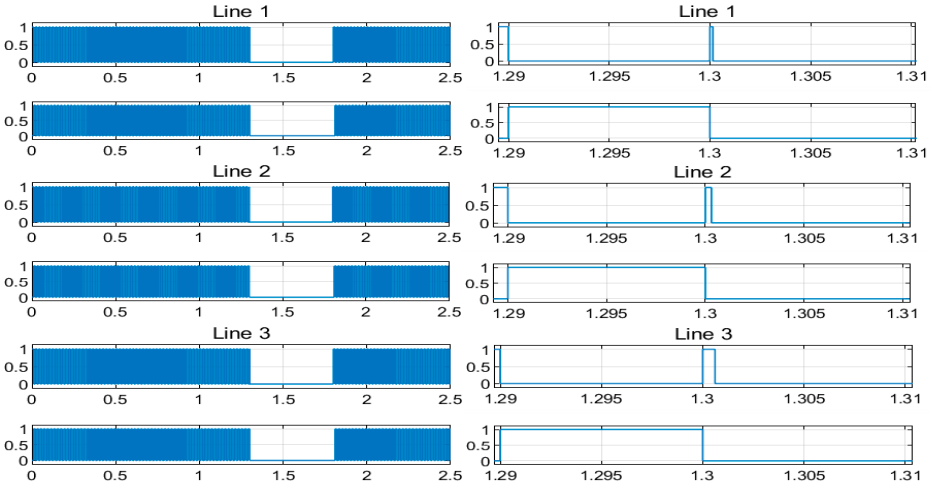

Figure 9. Pulses generated in all three-phases under L-L-L-G.

For balanced voltage sag, the main grid fault; triple-phase to ground is used to simulate voltage sag of 50% in evaluating the proposed strategy. The extent of the voltage sag on the main grid is shown in Figure 10, which prompts a corresponding rise in the current amplitude.

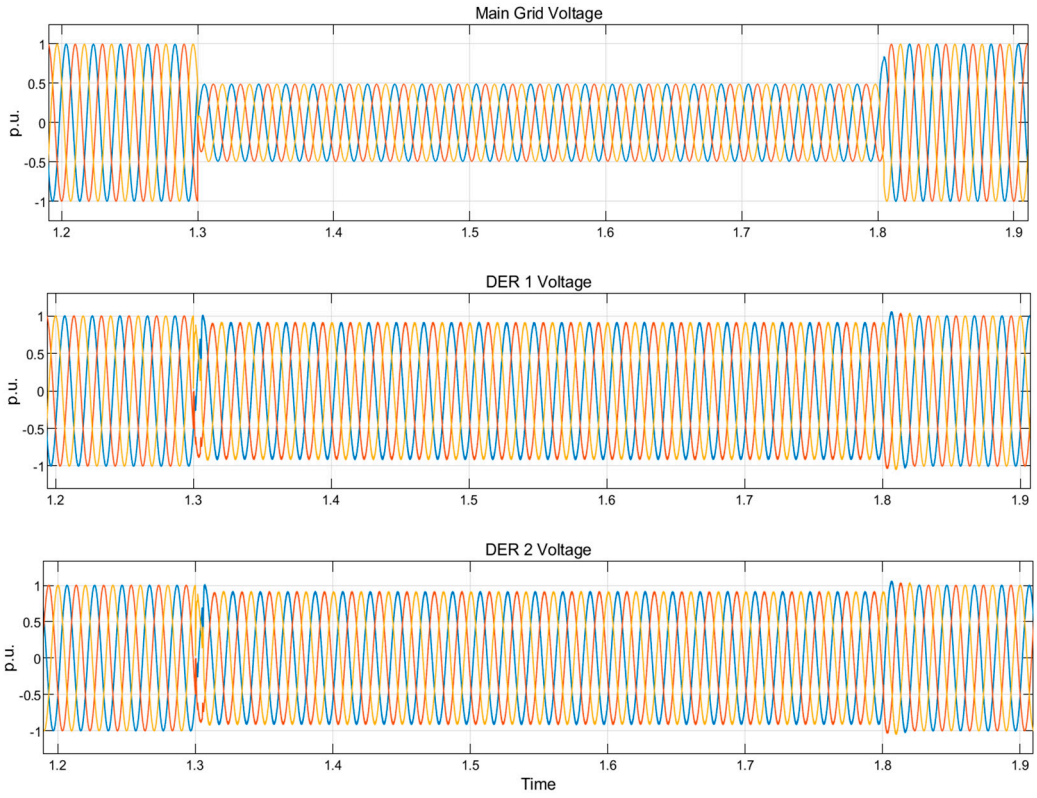

Figure 10. Voltages in the grid and microgrid at grid voltage sag of 50% produced by L-L-L-G fault.

The prompt current amplitude limitation is provided by the secondary power reference embedded in the FRT scheme of the secondary control in each of the DER as shown the Figure 5 and depicted by the Equations (9) and (23). The active and reactive current references are changed instantaneously at fault inception. Similarly, these references are properly restored immediately fault condition is over with appropriate tuning of the kp and ki gains of the proportional–integral controllers. Thus, Figure 10 reveals a smooth transition from pre-fault to fault and subsequently, from fault to post-fault condition. Therefore, the output current of DERs' LC filter is appropriately limited as shown in Figure 10. Consequently, the 50% voltage sag percentage observed at the PCC to the grid is improved to 93.32% in the microgrid.

The voltage sag on the main utility is detected at the PCC in at 0.0001515 s which is less than half of the first cycle of fault occurrence. This implies that the fault is detected in 1.3001515 s as shown in the positive half cycle and 1.300 on dot in the negative half cycle. Consequently, the FRT scheme fault mode operation is activated with simultaneous switching of the IGBT-diode switched reactor in series with all the phases for balanced transient conditions and series with only the affected phase in unbalanced conditions. The grid voltages for all the balanced conditions of voltage sag resulting in 50% voltage sag are shown in Figure 10. The implementation of the FRT schemes for DERs of the microgrid ensured that the microgrid voltage is compensated for the effective running of the microgrid irrespective of the main grid transient condition. The voltage in the microgrid is improved to 93.32% under 50% sags measured at the PCC.

The fault current limiting ability of this secondary control with an appropriate selection of the gains of the PI controller, the DER 1 and DER 2 contribute to the main grid voltage reactive power support based on their kVA ratings. Figure 11 presents the output current waveforms of the DERs on 50% voltage sag at the PCC. The DER output currents are properly limited and no significant distortion is observed in the signals of DER output voltage and current. Thus, it is clear that the inverter currents are appropriately limited in the first cycle after fault inception at 1.3 s, as shown in Figures 10 and 11. The delay of 0.00016 after the fault for the activation of the proposed control is

short and insignificant. However, overcurrent produced between 1.30000 and 1.30016 s cannot damage the inverter semiconductor switches. Furthermore, grid faults technically appear across the filter capacitor and the transient current overshoot at fault inception vanishes almost instantaneously and is therefore ignored. It must be noted that the current overshoot at the instance of transient disturbance is completely attenuated whenever the VSI based DER is tied to an electrically weak grid far from the inverter installation.

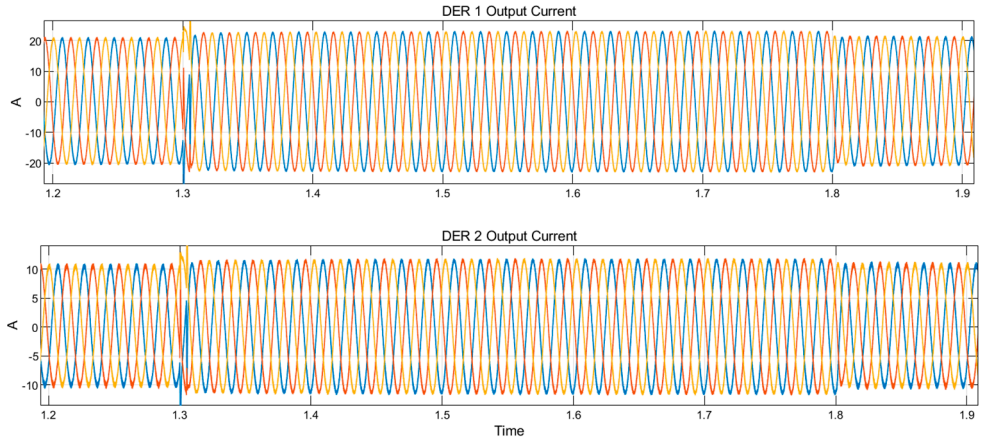

Figure 11. Current waveforms in the microgrid at grid voltage sag of 50% produced by L-L-L-G fault.

Following EN50160 standard, the THD of output voltage waveforms of any generating unit must not exceed 8% [76]. Consequently, the THDs (before, during and after fault clearance for various fault types causing 70%, 60%, and 50% voltage sags) of DER voltage signals and output current waveforms are revealed in Table 5. The THD is measured using fast Fourier transformation analysis in MATLAB. The excellent signal quality as signified in the low THDs of the DER voltages and output current is an indication of efficient performance of the FRT scheme put in place in this work. The microgrid voltages as observed demonstrate high-quality waveforms, output DER voltage, and current. The voltage harmonics are relatively negligible with reference to the current harmonics. The low THD recorded indicates great power factor, high efficiency, and small peak current. This reveals the effectiveness of this proposed FRT strategy at the secondary control and conformity with the IEC 61000-3-2 standard [77].

Table 5. Total harmonic distortion (THD) of voltage and current waveforms of the DERs.

Voltage Sag	DER	Signal	Total Harmonic Distortion (%)		
			Pre-Fault	Fault	Post-Fault
70%	1	Voltage	0.33	1.17	0.33
		Current	2.01	2.15	1.99
	2	Voltage	0.33	1.17	0.33
		Current	3.94	1.50	3.67
60%	1	Voltage	0.32	1.20	0.33
		Current	2.06	2.06	2.09
	2	Voltage	0.32	1.20	0.33
		Current	3.78	3.64	3.74
50%	1	Voltage	0.32	1..25	0.33
		Current	2.06	2.05	2.01
	2	Voltage	0.32	1.25	0.33
		Current	3.78	3.37	3.84

In compliance with the grid codes, the FRT control arrangements ensure the delivery of a commensurate reactive power in supporting grid voltage sag, thereby effecting DERs ride through of disturbances. Consequently, the changeover from grid synchronous to the islanded mode of operation is avoided. The microgrid voltage is kept within the range of operation (0.9–1.1 Spanish grid code) to guarantee continuous delivery of active power to the sensitive local microgrid loads as shown in Figures 12 and 13. The increase in the reactive power requirement limits the inverter active power reference generation to conform to complex power limit imposed by the FRT scheme and VSI ratings.

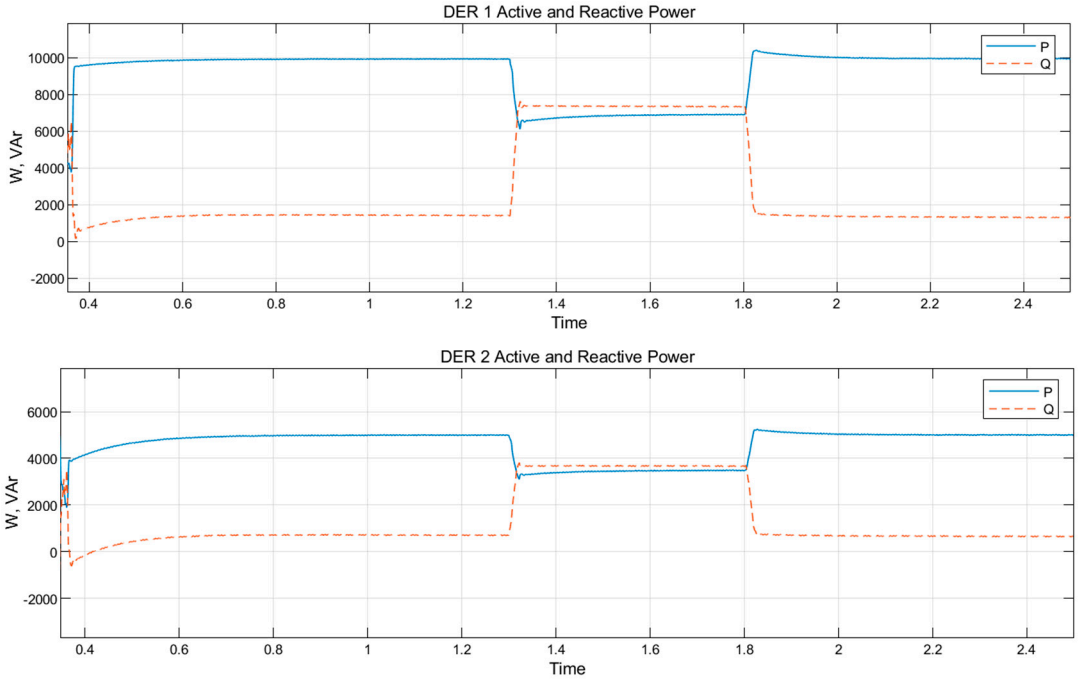

Figure 12. Power supplied by DER 1 and DER 2 under voltage sag of 50% produced by L-L-L-G fault.

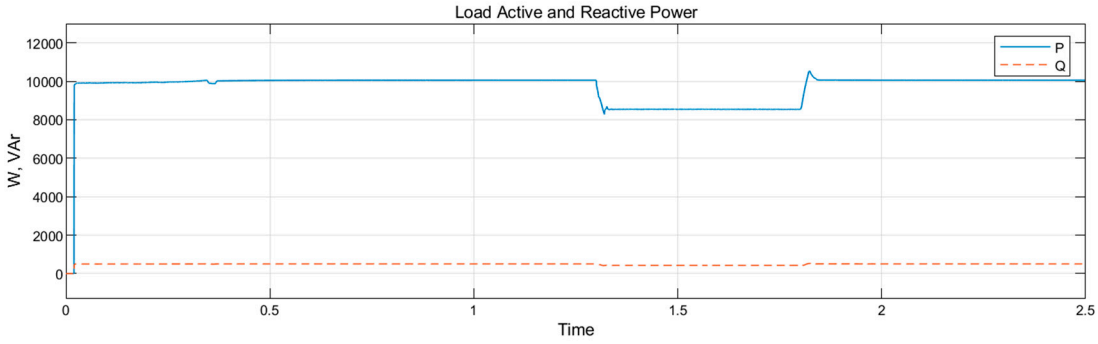

Figure 13. Power supply to local microgrid load under voltage sag of 50% produced by L-L-L-G fault.

Under the fault period, the increased generation of the reactive power ensures that the microgrid voltage is regulated to an acceptable magnitude. Immediately, the fault clearance is effected at the time t = 1.8 s, FRT scheme senses the rise in main grid voltage to an acceptable range of 0.90–1.10 at the PCC. Thus, the reactive power injection is reduced based on the degree of voltage rise. Similarly, Figure 11 shows the increase in reactive power injected as well as a proportional steep decline in active power. The implementation of this FRT control with the DSC algorithms track the main grid disturbance using the voltage sag sensed at the PCC. The FRT strategy limits active and reactive references in both DERs as required to cause microgrid voltage improvement without significant distortion to the DER output current and voltage waveforms.

The aggregate active power supply by DERs is limited as a result of voltage sag occasioned by grid fault. The DERs are controlled to firstly inject an active power amount that meets the local load demand and therefore reduces the active power injection into the faulted main utility grid. Throughout voltage sags, the decreased grid voltage magnitude and the 'off' switching of the IGBT-diode AC reactor limit active power transmitted to the grid. The amplitude of fault current is limited and the microgrid voltage is improved for the transfer of active power to the local load. For intense voltage sag, generated active power is limited to the rated value of the local load. Any time there is an excess generation, the surplus is supplied to the faulted grid. However, in the acute incidence of grid voltage sag to the tune of 20% or less, no active power can be generated for the local microgrid load and main grid load. Consequently, DER reactive power generation is maximized in supporting the voltage of the host grid in compliance with Spanish grid codes. For instance, under 20% grid voltage drop, the corresponding power generations by the two DERs are shown in Figure 14.

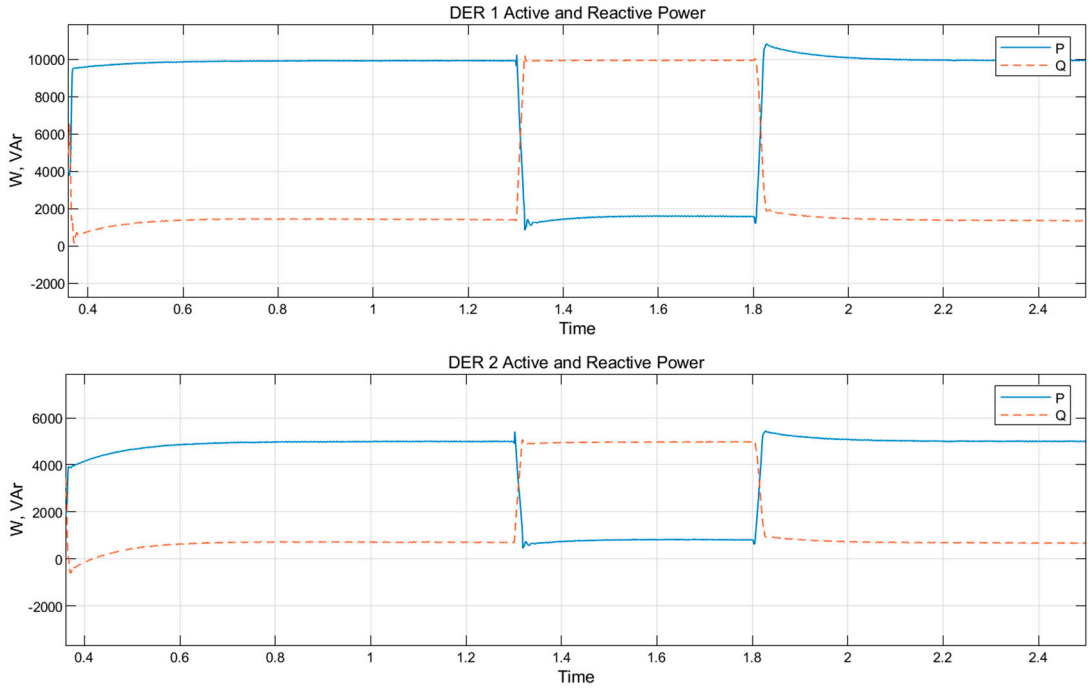

Figure 14. Power generated under a voltage sag of 20% produced by L-L-L-G fault.

5.2. Asymmetrical Fault

Single phase-to-ground faults are the most common in typical distribution systems [78,79]. The other asymmetrical faults include the line to line and double line to ground. The efficacy of the proposed control strategy is also tested under the unbalanced grid conditions listed above. This unbalanced fault is simulated in Line 1 (color blue) between t = 1.30 and t = 1.80. Under a single L-G fault, the grid voltage and DER voltage and current are shown in Figures 15 and 16. No significant distortion appears in the DER 1 and 2 output voltage waveform and current waveform. The FRT control with the IGBT switched AC reactor effectively compensated for the unbalance sags in voltage magnitude. The three-phase voltage within the microgrid as indicated by the DER 1 and DER 2 appear with relatively balanced values compared to the grid voltage unbalance.

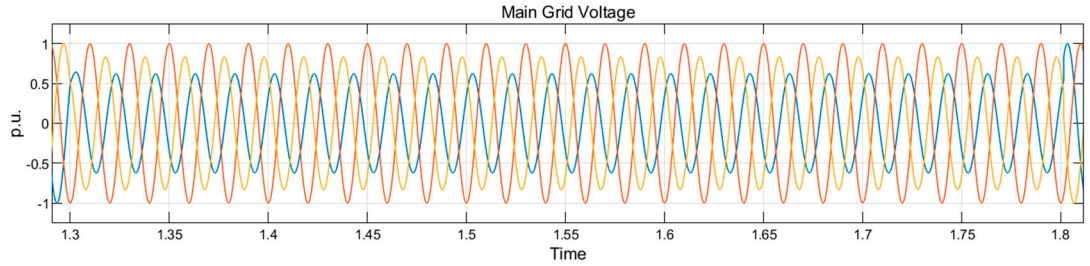

Figure 15. Grid voltages under L-G fault on the main grid.

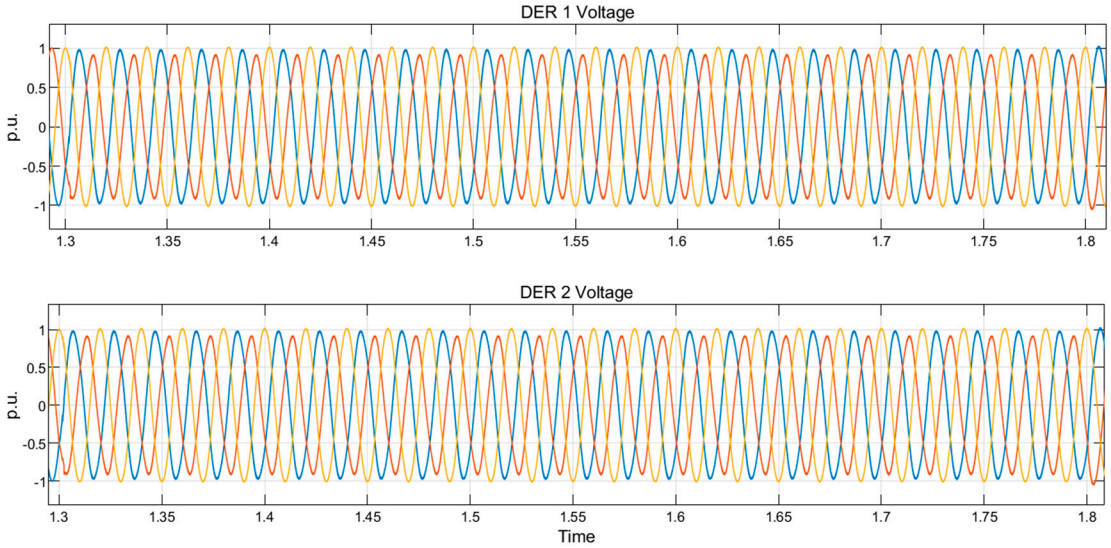

Figure 16. Microgrid voltages under L-G fault on the main grid.

During an unbalanced transient leading to an unbalanced voltage sag within the grid, the voltage unbalances at the PCC are evaluated from the phase to phase voltages V_{ab}, V_{bc}, and V_{ca}. Applying NEMA (National Equipment Manufacturer Association in the United States of America) voltage unbalance definition which is given as the ratio of maximum deviation from the mean phase to phase voltage to mean of phase to phase voltages, the unbalance within the grid under L-G fault is calculated. Similarly, the unbalance calculated for other types of asymmetrical faults are given in Table 6. The proposed control actively compensated the unbalance in line to line voltages by reducing the unbalance to relatively negligible percentages.

Table 6. Voltage unbalance measured under asymmetrical faults.

Fault Type	Voltage Unbalance	
	Grid	Microgrid
L-G	24.14%	4.44%
L-L-G	24.31%	7.13%
L-L	35.36%	12.20%

Similar to the case of balanced voltage sag occasioned by a symmetrical transient disturbance on the main grid, the Figures 16–19 further affirm the effectiveness of the proposed FRT secondary control in riding through faults, compensating unbalance voltage sag and improving microgrid voltage, limiting the amplitude of current, and ensuring local load power demand are met. Irrespective of the main grid unbalance condition, the microgrid voltage balance is relatively maintained within limit and currents limited to ensure uninterruptible supply to the local load most importantly before exporting excess generation to the main grid.

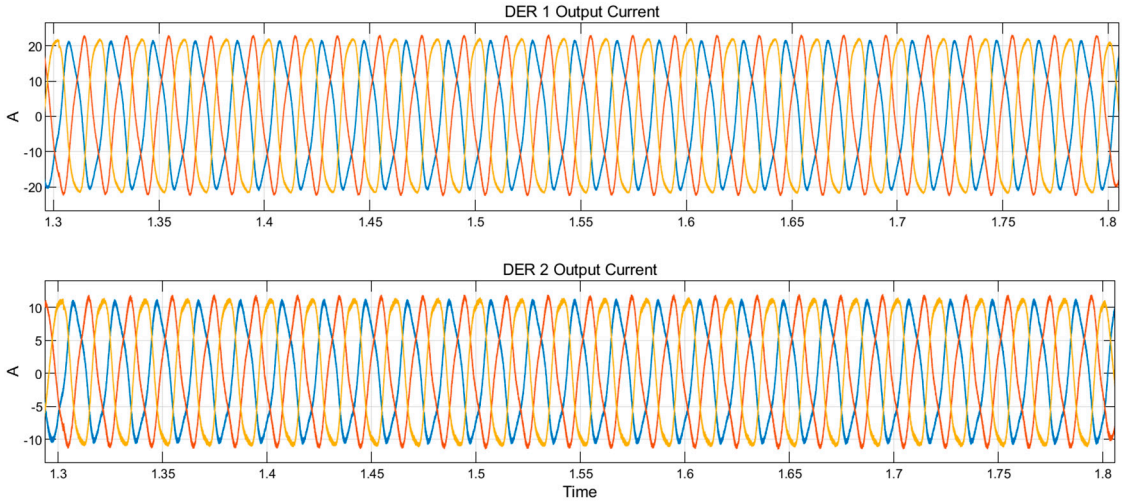

Figure 17. Grid and microgrid current under L-G fault on the main grid.

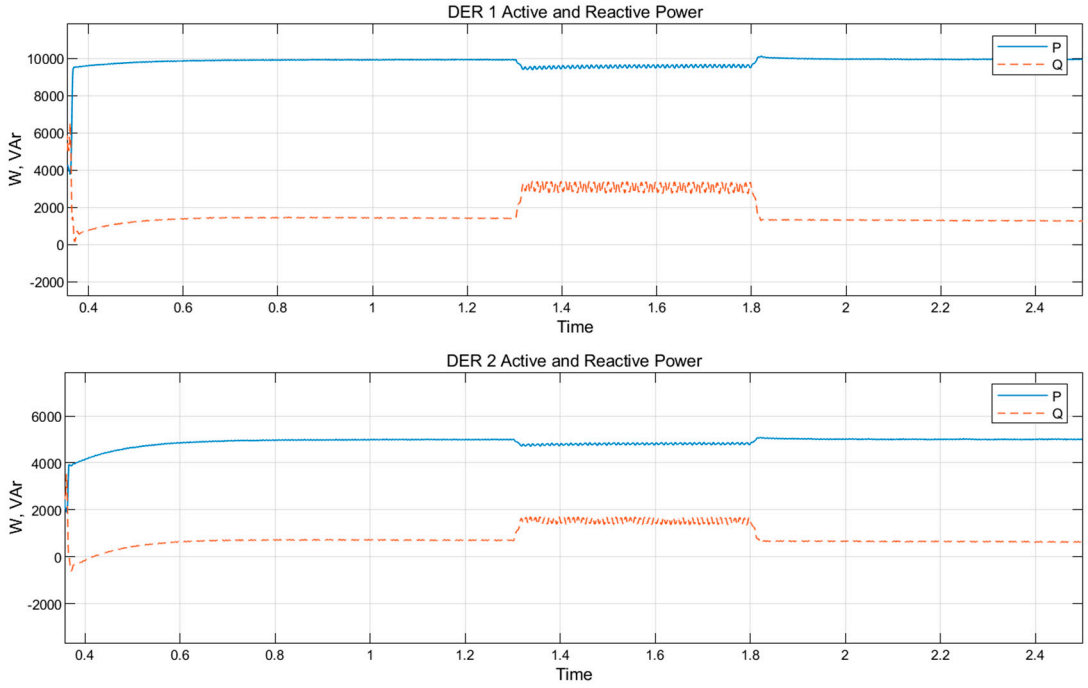

Figure 18. Power supplied by DER 1 and DER 2 under L-G fault.

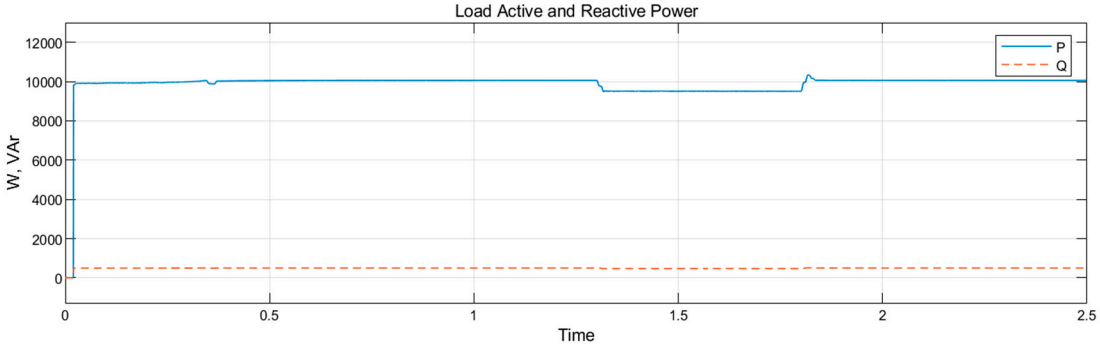

Figure 19. Power supplied to the local microgrid load under L-G fault.

6. Conclusions

A secondary controller which realizes an FRT control for voltage source inverter based DER using DSC fault detection algorithm is implemented in this work. This controller meets FRT requirements of Spanish grid codes by providing a secondary voltage control whose operation is effective and significant in the transient period of faults. This controller performance is further enhanced with an IGBT-diode switched AC reactor to improve the voltage and prevents the transient overcurrent in the microgrid during the grid fault. This ensures a continuous supply of the microgrid local sensitive load while meeting the grid code requirement of FRT. Similarly, the active power injection from the microgrid to the main grid is limited to maximize reactive power generation in supporting voltage sags (0.85–0.9 pu), moderate voltage sags (0.5–0.849 pu) and critical grid voltage sags (less than 0.5 pu). The sequence detection algorithm using the DSC is implemented to detect negative sequence and instance of fault in 0.0001515 s to activate the proposed FRT secondary control to comply with the grid code stipulations. The results of simulation confirm the performance and effectiveness of the proposed strategy.

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