Advanced electrical characterization of atomic layer deposited Al_2O_3 MIS-based structures

H. García, H. Castán, S. Dueñas
Dpto. Electricidad y Electrónica
E.T.S.I.Telecomunicación, University of Valladolid
Paseo de Belén 15, 47011 Valladolid, Spain
e-mail: hecgar@ele.uva.es

M. B. González, M. C. Acero, F. Campabadal
Institut de Microelectrònica de BarcelonaIMB-CNM, CSIC
08193 Bellaterra, Spain

***Abstract*—The electrical properties of Al_2O_3-based metal–insulator–semiconductor capacitors have been investigated. Three different metal gate electrodes were used: two mid-gap metals (TiN and tungsten) and aluminum, a metal with a work function close to the silicon electron affinity. Aluminum oxide films were grown on p-type silicon substrates by atomic layer deposition using trymethylaluminum and water as aluminum and oxygen precursors, respectively. The use of aluminum as the gate electrode prevents the formation of defects inside the oxide layers that could trap charge as has been found for W and TiN gate electrodes using C-V curves and flat band voltage transients. The use of TiN or W as gate electrodes increases the interfacial trap density. However, the leakage current, that follows a Fowler-Nordheim behavior, is low when using TiN electrodes due to a higher cathode barrier height.**

Keywords—high-k dielectrics; metal gates; atomic layer deposition; MIS capacitors; electrical characterization.

I. INTRODUCTION

Poly-silicon and silicon oxide (SiO_2) have served as the mainstay of the electrode and the insulator materials in complementary metal-oxide-semiconductor technology. The first challenge has been the replacement of the oxide by a high-k dielectric due to the unacceptably high leakage current in ultrathin SiO_2 layers. However, these high-k materials usually present lower breakdown electric fields, higher amount of defects and worse thermal stability. In addition, with the introduction of high-k gate dielectrics the poly-silicon gate has also been replaced by a metal gate to solve the problems related to poly-Si gate depletion and high gate resistance [1]. The gate depletion layer increases the equivalent oxide thickness. The introduction of metal gates not only removes the depletion layer but also decreases the gate sheet resistance and the boron penetration during source and drain implantations.

In this work, we have evaluated the electrical properties of metal-insulator-semiconductor (MIS) capacitors using aluminum oxide (Al_2O_3) as the gate insulator, and three different metal gate electrodes: tungsten (W), titanium nitride (TiN) and aluminum (Al). TiN has low electrical resistance and can suppress the outdiffusion of Si more efficiently than aluminum. The combination TiN/Al_2O_3has been found as a promising candidate due to its chemical compatibility, thermal stability and good adhesion properties [2]. Tungsten is a material that has been investigated since the metal gates were studied in order to replace poly-Si gates in the late 1970s due to its low resistivity value. However, there are some problems regarding this metal that have been attempted to be solved: W thin films cannot withstand an oxidizing ambient at high temperatures, and some dopants easily penetrate into the gate electrode [3]. Finally, aluminum has been the standard gate electrode for the evaluation of SiO_2 gate dielectrics.

We focused our attention mainly in the electrical properties and defects present at the oxide/semiconductor interface and in the bulk dielectric. The electrical characteristics of the samples were exhaustively studied by means of the following techniques: capacitance – voltage (C–V), deep level transient spectroscopy (DLTS) and flat-band voltage transients (V_{FB}-t). The conduction mechanisms were also studied by measuring current – voltage (I-V) characteristics at several temperatures from the liquid nitrogen temperature to room temperature.

The metal electrodes were deposited on atomic layer deposited (ALD) aluminum oxide (Al_2O_3). Although Al_2O_3 has a modest permittivity value (~ 9), it has a large band gap (~ 9 eV) and large band offsets with the Si substrates, enabling low leakage currents and high breakdown electric fields. This oxide also remains amorphous at temperatures up to 800 ºC [4].

II. EXPERIMENTAL

A. Sample preparation

The MIS capacitors were fabricated on p-type, boron doped, (100)-oriented Czochralski-grown silicon wafers with resistivity (0.1-1.4) Ω cm. The fabrication process started with standard wafer cleaning followed by a wet thermal oxidation process at 1100 °C leading to a 400 nm thick SiO_2 layer. Next, this field oxide was patterned by photolithography and wet etching. Immediately after cleaning in H_2O_2/H_2SO_4 and a dip in HF(5%), 5.9 or 11 nm thick-Al_2O_3 films were deposited by ALD. This process was done at 200ºC using trimethyaluminum (TMA) and water as aluminum and oxygen precursors, respectively. The thicknesses of the oxide layers were measured by ellipsometry. A post-deposition annealing was performed in N_2 atmosphere at 350 ºC for 30 minutes.

978-1-5090-5072-7/17/$31.00 ©2017 IEEE

TiN (150 nm), W (200 nm) or Al (500 nm) were then deposited by magnetron sputtering and patterned by means of standard photolithography and wet etching in the case of Al and by a lift-off process in the case of TiN and W.

The back side of the wafers was metalized with aluminum for electrically contacting the substrate. The fabricated MIS structures are square-shaped, and the electrical measurements were carried out on capacitors with area 1.44×10^4 μm^2.

B. Electrical characterization techniques

In order to record the electrical parameters at several temperatures varying between liquid nitrogen temperature (77 K) and room temperature, samples were first cooled in darkness from room temperature to 77 K at zero bias in an Oxford DM1710 cryostat. An Oxford ITC 502 controller was used to monitor and to keep the temperature constant during the measurements.

C-V curves were recorded using an Agilent 4294A impedance analyzer at a frequency of 100 kHz. In order to obtain the capacitance transients for DLTS technique, a 1 MHz Boonton 72B analog capacitance meter was used together with an HP54501A digital oscilloscope, which recorded the capacitance transients at several temperatures. The same oscilloscope and an EG&G 5206 lock-in analyzer were used to record the conductance transients in order to obtain the border trap distribution.

In previous works [5] we demonstrated that charging and discharging mechanisms of localized states inside the dielectric yield flat band voltage time transients. As the charge trapping or detrapping inside the insulator is usually tunneling assisted, states located deeper in the dielectric capture carriers after those located near the semiconductor/oxide interface, so the V_{FB} transients obtained are slower than the DLTS transients. These transients were obtained using a feedback system that varies the applied gate voltage accordingly so as to keep the capacitance at its flat-band voltage value.

Finally, a Keithley 4200-SCS semiconductor parameter analyzer was used to record the current – voltage (I-V) curves at several temperatures in order to obtain the conduction mechanisms.

III. RESULTS

The aluminum oxide permittivity value obtained from C-V measurements is about 10.5. As an illustration, Fig. 1 shows C-V curves measured at 100 kHz, at room temperature and at the temperature of liquid nitrogen (≈ 77 K) corresponding to 11 nm-thick oxide films.

The Al – Si work function difference is about -0.75 V for doping levels similar to the value we have used. We can observe (Fig. 1) that the flat band voltage value is very close to its theoretical value for the capacitor with the Al gate regardless the measuring temperature. This means that there is very little amount of charge trapped inside the insulator; in fact, no hysteresis is obtained in the C-V curves and the stretch-out is negligible in these curves. On the other hand, the theoretical TiN – Si and W –Si work function differences are very similar, about -0.45 V [1], although in the case of TiN, it depends on the composition [6]. But the flat-band voltage value is not close to this value for W electrode, so this means that there must be charge trapped inside the insulator: positive in this case. An estimation of the effective trapped charge density (N_{eff}) can be evaluated. The value obtained is 6×10^{12} cm^{-2}. Metal diffusion and oxygen diffusion has been specially observed in tungsten electrodes [3], and could be the cause for this charge. The flat-band voltage value is closer to the theoretical value for TiN electrodes, but in this case there exists negative trapped charge. In this case, the value obtained for N_{eff} is lower, 3×10^{12} cm^{-2}. D. Hoogeland *et. al.* [2] obtained a very similar V_{FB} value for TiN/Al_2O_3/p-Si system for 10 nm oxides. Hysteresis is observed in C-V curves in both samples, being the hysteresis amplitude larger in the case of W electrode. The defects that cause the hysteresis seem to be frozen at low temperatures, as the hysteresis phenomena disappear for low temperature.

The interfacial state density (D_{it}) was measured by means of DLTS. In the case of Al electrode, the DLTS transient amplitude is below our resolution limit. The stretch-out of the C-V curves is negligible in this case, corresponding to low D_{it} values. We can observe in Fig. 1 that the stretch out of C-V curves increases for TiN, and especially for W electrodes. The D_{it} values obtained by DLTS sustain these results: the interfacial state density value for W electrode is slightly higher than the value obtained for TiN electrode (≈ 1×10^{12} cm^{-2}eV^{-1} for TiN electrode and ≈ 2×10^{12} cm^{-2}eV^{-1} for W electrode).

The trap charging and discharging of defects inside the high-k layers that gives rise to hysteresis in the C-V curves also leads to variations in flat-band voltage.These flat-band voltage variations are shown in Fig.2. The samples were first biased in the inversion regime. Then the initial bias was removed and the gate voltage was recorded while keeping the capacitance constant at the flat-band condition. The decreasing transients obtained mean positive charge is being trapped as

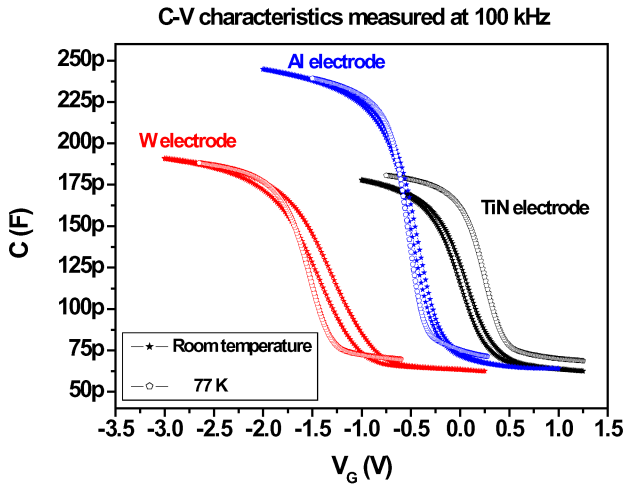

Fig. 1. Capacitance – voltage characteristics measured at room and at liquid nitrogen temperature, and at 100 kHz.

time passes. Capacitors using W showed the highest hysteresis amplitude. This capacitor shows the highest transient amplitude, as expected, because more defects inside the insulator can trap and detrap charge. The capacitor using Al as gate electrode showed almost no hysteresis in C-V curves, and the flat band voltage transient amplitude is the lowest. Samples with TiN electrode show a halfway behavior. Fig.3 (a) shows transients measured at several temperatures for TiN electrode. The transients amplitude was thermally enhanced, and the temperature dependence followed an Arrhenius plot (Fig.3 (b)). The activation energy has been found to be 235 and 103 meV for TiN and W electrodes respectively. The activation energy has sometimes been found to be similar to the soft optical phonon energies reported for high-k dielectrics [5].

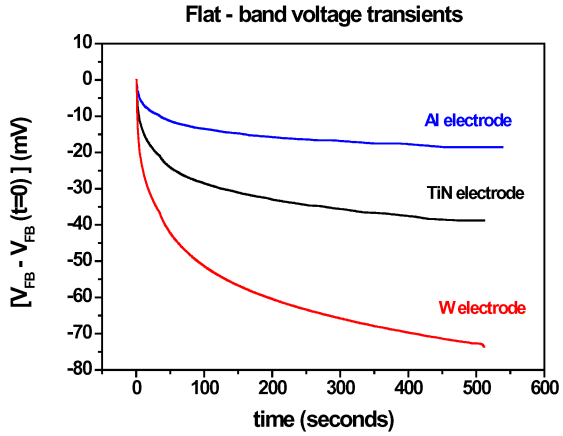

Fig. 2. Flat – band voltage transients measured at room temperature.

On the other hand, the border trap distribution was obtained in samples using Al as gate electrode. Fig. 4 shows the distribution. Defects are detected up to 15 Å inside the insulator, measured from the semiconductor interface. A maximum of $1.2x10^{11}$ $cm^{-2}eV^{-1}$is detected at an energy position of around 75 meV over the semiconductor valence band, and at a spatial position located very close to the interface. As said before, DLTS measurements in these samples provided interfacial state density values below the experimental resolution, therefore we can conclude than defects are preferentially located inside the dielectric.

Leakage current densities were measured at the accumulation regime and at several temperatures ranging from 100 K to room temperature. The current density remains nearly independent of the measurement temperature. This is a characteristic of tunneling conduction, following the Fowler-Nordheim current behavior:

$$J = A\,F^2 exp\left(-\frac{B}{F}\right) \qquad (1)$$

where $A = \frac{mq^3}{8\pi m^* \emptyset}$ [A V^{-2}] ,$B = \frac{8\pi\sqrt{2m^*}\emptyset^{3/2}}{3hq}$ [V m^{-1}], and F is the electric field.

Fig.5 shows the representation of $ln(J/F^2)$ vs $1/F$ measured at 200 K. Different effective electron mass values in aluminum oxide can be found: Groner *et. al.* [7] obtained a value of 0.23 m_0, Kim *et. al.* [8] obtained a value of 0.5 m_0 and Specht *et. al.* [9] a value of 0.45 m_0 for Al_2O_3 grown by atomic layer deposition. This scatter in the electron effective mass value can lead to differences in the barrier height value obtained. Using the TiN electrode, we obtained a barrier height value of 3.17 eV using an electron effective mass value of 0.23 m_0.The theoretical value of the conduction band offset of Al_2O_3 to TiN is 3.8 eV [10]. Other authors obtained lowervalues (3.3 eV [11]), similar to the value we have obtained. In the case of Al gate electrode, we obtained a barrier height value of 2.64 eV, a similar value to the obtained by Afanas'ev *et al* (2.9 eV) [12]. Finally, a value of 2.3 eV for the barrier height was obtained in the case of W gate electrode. This low barrier height is the responsible for the higher leakage current in samples using W electrodes.

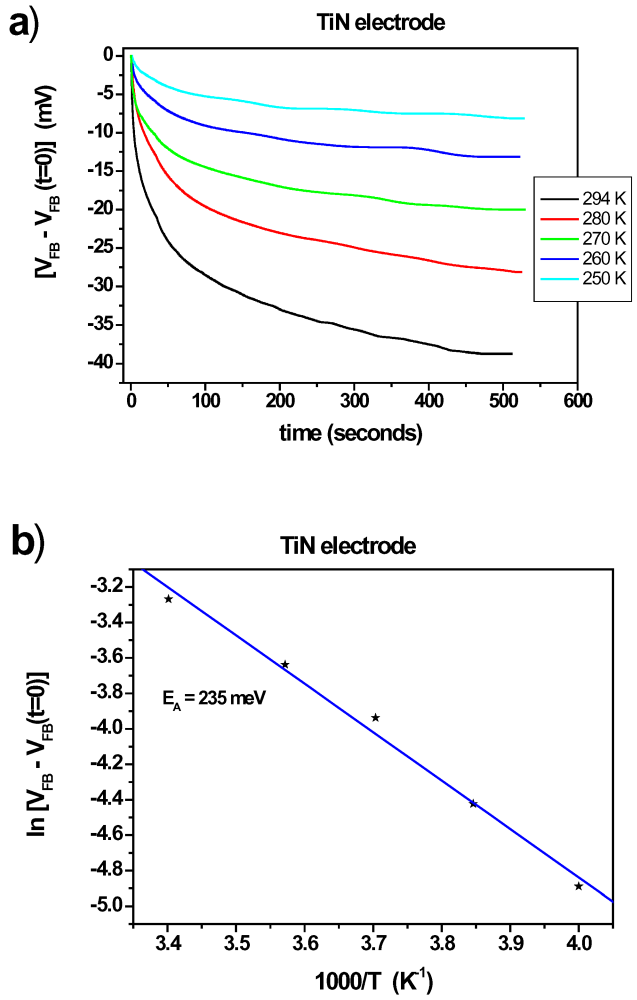

Fig. 3. Flat - band voltage transients measured at several temperatures for TiN electrode (a) and Arrhenius plot (b).

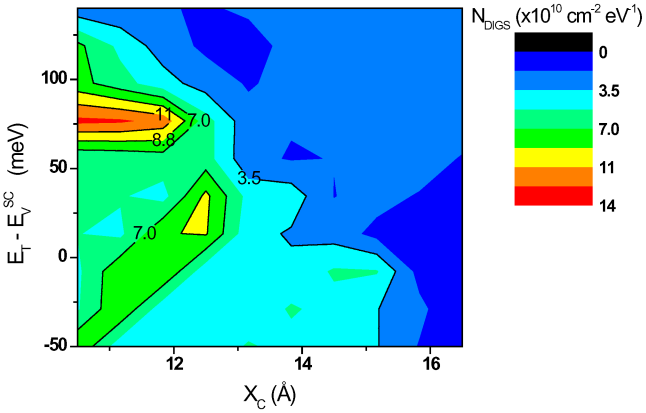

Fig. 4. Border traps of Al/Al_2O_3/Si MIS structures as a function of the energetic position from the semiconductor valence band and spatial distance from the interface (measured in angstroms).

IV. CONCLUSIONS

An electrical characterization study of Al_2O_3-based MIS capacitors using different metal gate electrodes has been carried out. Our experimental results revealed that the charge trapped inside the oxide layer is negligible when using Al as gate electrode. The use of W or TiN as the gate electrode originates charge trapped, detected by the hysteresis in C-V curves and by the flat-band voltage transients. This trapped charge is negative for TiN electrode. On the other hand, the trapped charge is positive in the case of tungsten electrode and could be due to oxygen diffusion through the metal gate, as usually attributed to W films.

The interfacial state density is below our detection limit in the case of aluminum electrodes, even for the thinnest films. When using W and TiN electrodes, the interfacial state densityis in the order of 10^{12} cm^{-2} eV^{-1}. Although the deposition of these metal gates worsens the interface quality,

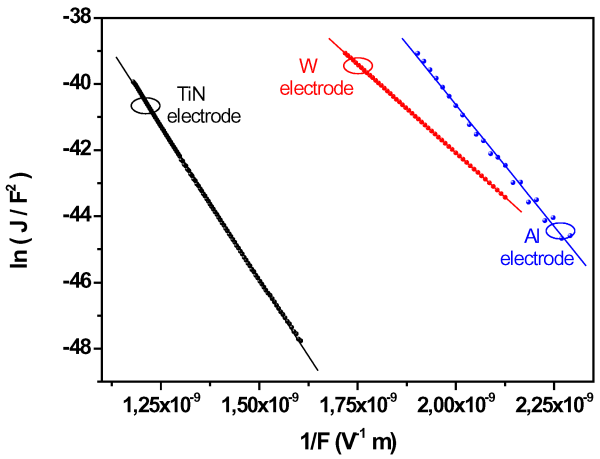

Fig. 5 Current – electric field dependence obtained for the different top electrodes at 200 K fitting following the Fowler-Nordheim model.

the amount of interfacial defects remains into acceptable values.

The gate leakage currents have also been measured. The currents are almost independent of the temperature, what means a Fowler-Nordheim behavior at high electric fields. This model fits well the leakage current data, and provides a barrier height of 3.17, 2.64 and 2.3 eV for TiN, Al and W, respectively. This result explains the better behavior of samples with TiN layer as top electrode in terms of leakage currents, and demonstrates the suitability of using this material in this kind of structures.

ACKNOWLEDGMENT

This study has been supported by the Spanish TEC2014 under Grant Nos. 52152-C3-3-R, 52152-C3-1-R and 54906-JIN.

REFERENCES

[1] Y-C. Yeo, "Metal gate technology for nanoscale transistors-material selection and process integration issues," Thin Solid Films, vol. 462-463, pp. 34-41, September 2004.

[2] D. Hoogeland, K. B. Jinesh, F. Roozeboom, W. F. A. Besling, M. C. M. van de Saden, and W. M. M. Kessels, "Plasma-assisted atomic layer deposition of TiN/Al_2O_3 stacks for metal-oxide-semiconductor capacitor applicarions," J. Appl. Phys., vol. 106, pp. 114107 (1-7), December 2009.

[3] J. H. Sone, S-O. Kim, K-J. Kim, H. S. Kim, and H. J. Kim, "Formation of low pressure chemically vapour deposited W thin film on silicon dioxide for gate electrode application," Thin Solid Films, vol. 253, pp. 377-381, December 1994.

[4] S. Jakschik, U. Schroeder, T. Hecht, M. Gutsche, H. Seidl, and J. W. Bartha, "Crystalliztion behavior of thin ALD-Al_2O_3 films," Thin Solid Films, vol. 425, pp. 216-220, February 2003.

[5] S. Dueñas, H. Castán, H. García, L. Bailón, K. Kukli, T. Hatanpää, M. Ritala and M. Leskelä, "Experimental observations of temperature dependent flat-band voltage transients on high-k dielectrics," Microelectron. Reliab., vol. 47, pp. 653-656, April-May 2007.

[6] S-H. Lee,R. Choi, and C. Choi, "Effects of composition and thickness of TiN metal gate on the equivalent oxide thickness and flat-band voltage in metal oxide semiconductor devices," Microelectron. Eng., vol. 109, pp. 160-162, September 2013.

[7] M. D. Groner, J. W. Elam, F. H. Fabreguette, and S. M. George, "Electrical characterization of thin Al_2O_3 films grown by atomic layer depoition on silicon and various metal substrates," Thin Solid Films, vol. 413, pp. 186-197, June 2002.

[8] J. Kim, J. Song, O. Kwon, S. Kim, C. S. Hwang, S. Park, S. J. Yun, J. Jeong, and K. S. Hyun, "Improvement in electrical insulating properties of 10-nm-thick Al2O3 film grown on Al/TiN/Si substate by remote plasma annealing at low temperatures," Appl. Phys. Lett,. vol. 80, pp. 2734-2736, April 2002.

[9] M. Specht, M. Städele, S. Jakschik, and U. Schröder, "Transport mechanisms in atomic layer deposited Al_2O_3 dielectrics," Appl. Phys. Lett. vol. 84, pp. 3076-3078, April 2004.

[10] F. Mondon, and S. Blonkowsky, "Electrical characterisation and reliability of HfO_2 and Al_2O_3-HfO_2 MIM capacitors," Microelectron. Reliab., vol. 43, pp. 1259-1266, August 2003.

[11] L. P. B. Lima, H. F. W. Dekkers, J. Lisoni, J. A. Diniz, S. Van Elshocht, and S. De Gendt, "Metal gate work function tuning by Al incorporation in TiN," J. Appl. Phys., vol. 115, pp.074504 (1-5), February 2014.

[12] V. V. Afanas'ev, M. Houssa, A. Stesmans, G. J. Adriaenssens, and M. M. Heyns, "Band alignment at the interfaces of Al2O3 and ZrO2-based insulators with metals and Si," J. Non-Cryst. Solids, vol. 303, pp. 69-77, May 2002.