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Research paper

Study of the admittance hysteresis cycles in TiN/Ti/HfO_2/W-based RRAM devices

S. Dueñas [a,*], H. Castán [a], H. García [a], E. Miranda [b], M.B. Gonzalez [c], F. Campabadal [c]

[a] Department of Electronics, University of Valladolid, Paseo de Belén 15, 47011 Valladolid, Spain
[b] Departament d'Enginyería Electrònica, Universitat Autónoma de Barcelona, 08193 Bellaterra, Spain
[c] Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC), Campus UAB, 08193 Bellaterra, Spain

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ABSTRACT

Similarly to the current, the admittance of TiN/Ti/HfO_2/W-based resistive memories shows well-defined minor switching loops associated with partial transitions between the ON and OFF states. Excellent control of the intermediate states is achieved in these samples by means of a proper sequence of input signals and current compliances. It is shown that, as the resistance state of the conductive filament changes, the associated susceptance also exhibits multilevel response. Susceptance values are negative in the ON state, indicating an inductive behavior of the conductive filaments.

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1. Introduction

A great deal of works related to reproducible switching effect of several oxides for memory applications have been published in the last years. Many of them report the electrical tuning of resistance between two clearly differentiated states (high and low resistance) [1,2]. In order to broaden their potential applications, the study of the admittance behavior is of great interest. For instance, in this work we prove that the small signal parameters measured at zero bias can be varied in a continuum depending on the stimulus previously applied. That can be used on neuromorphic applications. Moreover, the fact of these parameters can be measured at zero bias reduces the power consumption and minimizes the effect on the device state itself when it is sensed. However, few papers about experimentally observed changes on capacitance during the switching process can be found [3–5]. A MEM-Z device showing a memory effect and in which both the resistance and the capacitance can be tuned simultaneously has been recently reported [6]. This paper deals with a detailed study of admittance cycles in HfO_2-based RRAM devices that show bipolar current-voltage loops.

2. Experimental

The devices under investigation are TiN/Ti/20 nm-HfO_2/W RRAMs. HfO_2 films were deposited by atomic layer deposition (ALD) at 225 °C using TDMAH and H_2O as oxidant precursors, and N_2 as carrier and purge gas. The resulting structures are square cells of $5 \times 5\ \mu m^2$.

Electrical measurements were carried out putting the sample in a light-tight, electrically shielded box. DC-current and admittance were measured using a Keithley 4200SCS semiconductor analyzer. A parallel admittance model was selected to perform the characterization because it directly provides the device conductance (G) and susceptance (B) values in which this work is focused. The voltage was applied to the TiN/Ti top electrode with the W bottom electrode grounded.

3. Results and discussion

The investigated RRAM devices require an initial electroforming step in order to activate the switching property ($V_F = 4$ V). This is accomplished using a voltage ramp with current limitation (CC = 0.1 mA). After this, RS cycles with good repetitiveness are performed. Subsequently, CC was progressively increased in order to control the size and/or the number of CFs [7] (Fig. 1). It is remarkable that the maximum CC value (50 mA) was never reached. In this experiment, the CC value is varied in a discrete way. This fact does not allow to conclude whether the increase in current is due to the increase in the thickness or in the number of filaments.

Similarly to the *I-V* characteristic, the real (conductance, G) and imaginary (susceptance, B) parts of the admittance signal exhibit hysteretic behavior. Small-signal measurements were carried out at room temperature and different frequencies in the range 20–500 kHz and with a CC of 50 mA. Bias voltages applied in the set region consist of double linear ramps: 0 V → V_{peak} → 0 V, where V_{peak} is a positive voltage

* Corresponding author.
E-mail address: sduenas@ele.uva.es (S. Dueñas).

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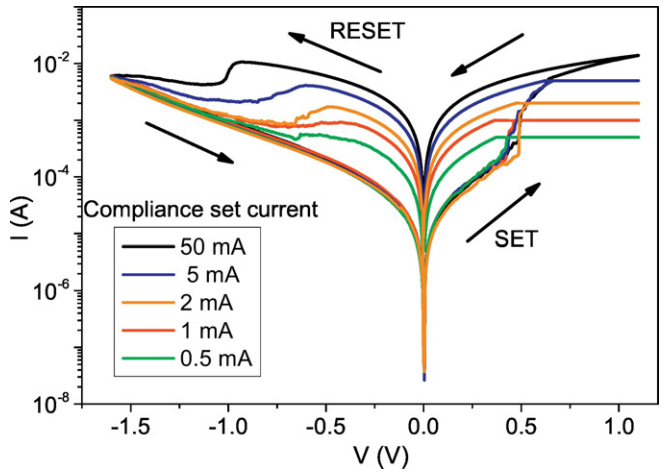

Fig. 1. Resistive switching loops showing set and reset processes, and the influence of compliance current.

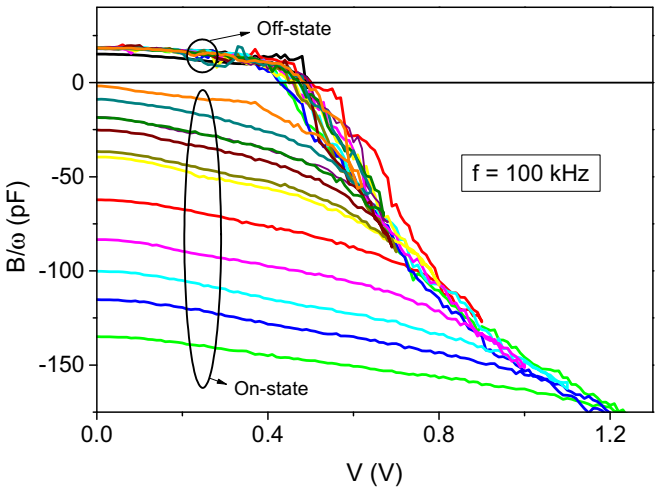

Fig. 3. B/ω vs voltage curves in the set region, obtained by using the DC sweep voltage mode.

ranging from 0 to + 1.3 V, a value that leads to complete set. Figs. 2 and 3 show the G and B/ω curves at 100 kHz obtained in this way. In these figures it is observed that the experimental values vary continuously due to the increase in the thickness of the conductive filament. The appearance of new filaments would give rise to discrete steps in these magnitudes which are not observed experimentally.

Similarly, in the reset region (Figs. 4 and 5), V_{peak} is a negative voltage ranging from 0 to − 1.6 V, a bias voltage leading to complete reset. Remarkably, negative values of B/ω are recorded for devices in the ON state both for positive and negative voltages (see Figs. 3 and 5). This means that the imaginary part of the admittance not only consists of the metal-insulator-metal (MIM) capacitance, but there appears an inductive term related to the CFs as well [6]. This effect is more important as the device size decreases. While the geometric capacity decreases with area, the inductive term due to the conductive filament is area independent, and its influence even more evident with scaling. In this connection, measurements performed at different frequencies are plotted in Figs. 6 and 7. The B/ω signal at the ON state depends on the frequency, and it is negative (Fig. 6). On the contrary, the G signal does not depend on the frequency (see Fig. 7). Therefore, at the ON state the CFs can be modeled as an inductance (L) in series with a resistive term (R_{ON}). In turn, both elements are in parallel with the capacitance of the MIM structure (C). Therefore, the total admittance of the structure can be expressed as:

$$Y = \frac{1}{R_{ON} + j\omega L} + j\omega C \tag{1}$$

And the real and imaginary parts of Y read:

$$Real\,(Y) = G = \left(\frac{1}{R_{ON}}\right)\frac{1}{1 + \dfrac{\omega^2 L^2}{R_{ON}^2}} \tag{2}$$

$$Im\,(Y) = B = \omega\left(C - \frac{\dfrac{L}{R_{ON}^2}}{1 + \omega^2 L^2 / R_{ON}^2}\right) \tag{3}$$

From the above expressions, when L dominates, $Im(Y)$ becomes negative and frequency dependent.

Measurements shown so far were carried out by sweeping the DC bias voltage. Since in the final high-end application of RRAMs, devices are usually operated in a pulsed voltage mode [8], pulsed measurements at room temperature were also carried out. For the set region study, a first 0 V → − 1.3 V (2.5 s) → 0 V pulse was applied to establish the

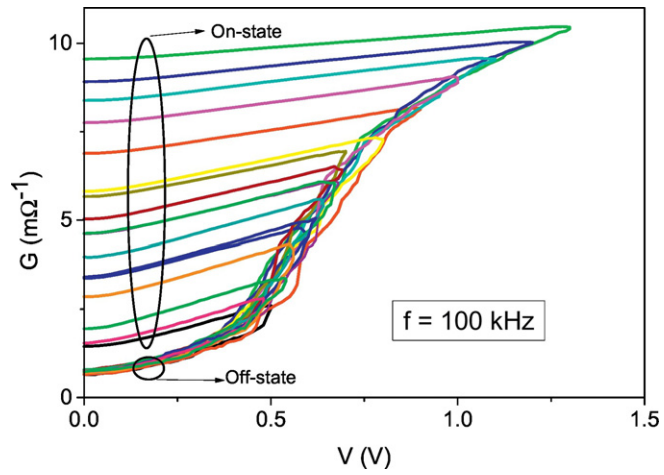

Fig. 2. Conductance-voltage curves in the set region, obtained by using the DC sweep voltage mode.

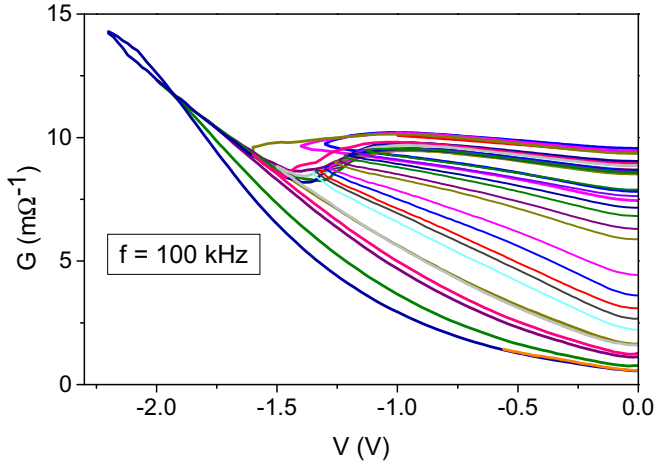

Fig. 4. Conductance-voltage curves in the reset region, obtained by using the DC sweep voltage mode.

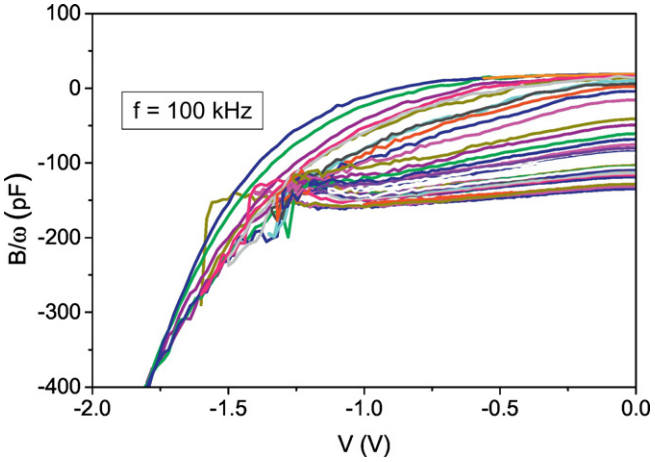

Fig. 5. *B*/*ω* vs voltage curves in the reset region, obtained by using the DC sweep voltage mode.

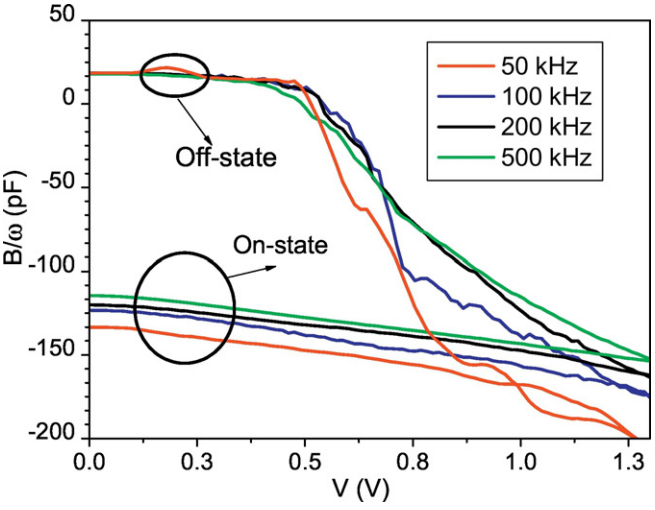

Fig. 6. *B*/*ω* vs voltage curves at different frequencies for positive voltages.

reset initial condition. The waveform used consisted in square pulses varying between 0 V (2.5 s) and V_{set} (2.5 s), with the following values of V_{set}: 0.1, 0.2, 0.3, … 1.1 V. After each set pulse, the admittance was

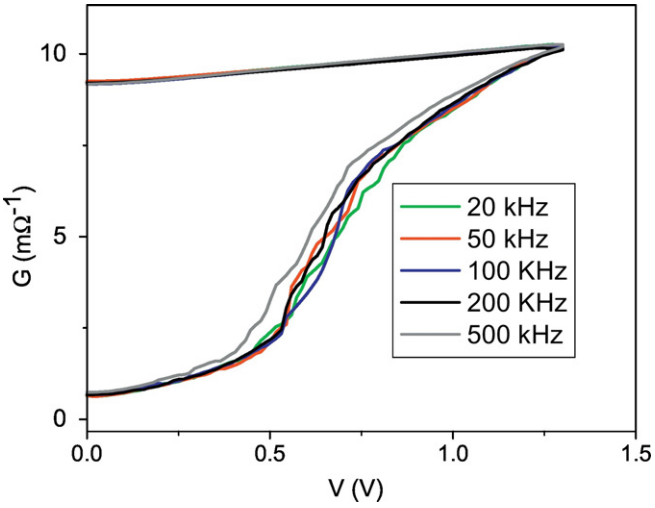

Fig. 7. *G* vs voltage curves at different frequencies for positive voltages.

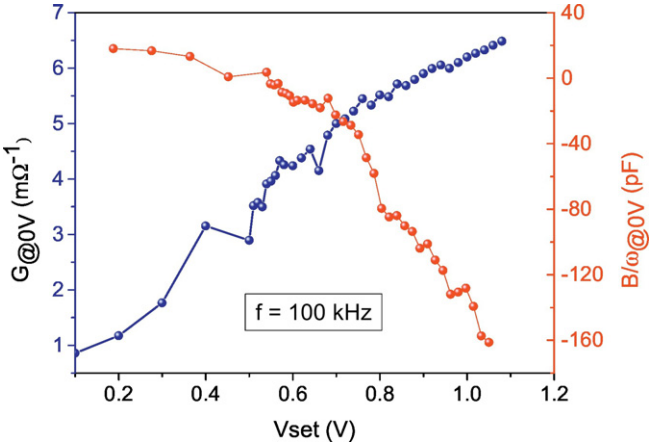

Fig. 8. Dependency of the conductance and *B*/*ω* at 0 V in the ON-state as a function of V_{set}, obtained by using the pulsed voltage mode.

recorded at 0 V. A similar study was carried out for the reset region. The initial condition was established by applying a 0 V → 1.1 V (2.5 s) → 0 V pulse sequence, and the waveform used varied between 0 V (2.5 s) and V_{reset} (2.5 s), with the following values of V_{reset}: −0.1, −0.2, −0.3, … −1.3 V. Figs. 8 and 9 show the results obtained in the set and reset regions at the frequency of 100 kHz. These results prove that is possible to control the intermediate states by voltage pulses. However, an accurate control on the initial conditions is mandatory. For instance, the first value of the susceptance on Fig. 9 (−50 pF after a pulse of 0.1 V) markedly differs from the last value of Fig. 8 (−160 pF after the last pulse of 1.1 V). We attribute this discrepancy to the fact that the initial set pulse in Fig. 9 was too short to establish a complete set. On the contrary, the last value of Fig. 8 is the cumulative result of the effect of a high number of positive pulses.

4. Conclusion

A good control of the RRAM device state, both in set and reset regions, was accomplished by gradually sweeping the bias voltage. Conductance and susceptance loops can be achieved with great repetitiveness. This allows us to determine a specific value of conductance and susceptance for each value of bias voltage applied. Importantly, the memory state of the device can be read by sensing the conductance and/or the susceptance at 0 V.

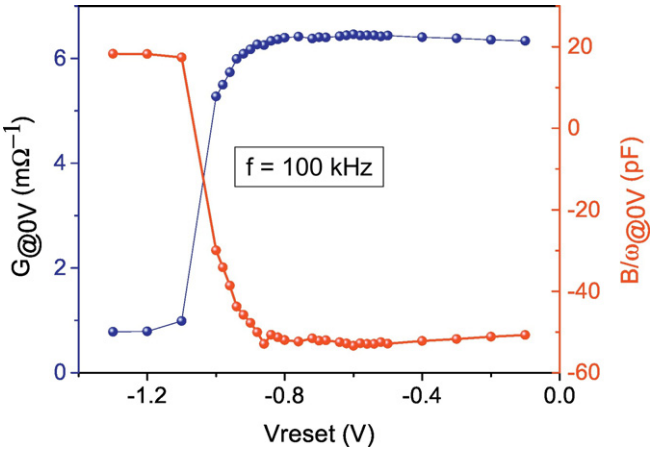

Fig. 9. Dependency of the conductance and *B*/*ω* at 0 V in the OFF-state as a function of V_{reset}, obtained by using the pulsed voltage mode.

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