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Verilog-A Based Implementation of a MOSFET Model for Analog Integrated Circuit Design

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Resumen:

La tesis expone en el desarrollo e implementación de un modelo compacto de un MOSFET, basado en el modelo teórico EKV, e implementado utilizando el lenguaje Verilog-A. La utilización de entornos de simulación y de compilación, como el servidor abierto OpenVAF y Ngspice, es fundamental para facilitar la ejecución efectiva del trabajo. La construcción de un modelo que pueda realizar la función de un nMOS o un pMOS nanométrico operando en un estado saturado se ve facilitada por éstos. En este modelo se incorporan dependencias físicas y se asegura la obtención de expresiones continuas para todas las regiones de inversión. El comportamiento del modelo se valida frente a datos experimentales mediante de simulación. El resultado de es un modelo preciso y versátil, apto para soportar diseños de circuitos analógicos integrados con un amplio rango de valores para el coeficiente de inversión.

Abstract:

The present thesis sets out the development and implementation of a compact model of a MOSFET, based on the theoretical EKV model, and implemented using the Verilog-A language. The utilization of simulation and compilation environments, such as the open server OpenVAF and Ngspice, is instrumental in facilitating the effective execution of the work. The construction of a model that can perform the function of an nMOS or a pMOS nanometric operating in a saturated state is facilitated by these. In this model, physical dependencies and second-order effects are incorporated, ensuring the attainment of continuous expressions for all inversion regions. The model's behaviour is validated against experimental data by means of simulation. This results in an accurate, compact and versatile model, which is suitable for supporting integrated analog circuits designs with a wide range of values for the inversion coefficient.

Palabras Clave:

MOSFET, Verilog-A, Open-source, Modelo EKV, Región Saturación

Keywords:

MOSFET, Verilog-A, Open-source, EKV model, Saturation Region

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ABSTRACT

Recent advances in the field of analogue electronics have led to an increased demand for the creation of programmable models of analogue circuits. The present thesis sets out the development and implementation of a compact model of a MOSFET, based on the theoretical EKV model, and implemented using the Verilog-A language. The utilization of simulation and compilation environments, such as the open server OpenVAF and Ngspice, is instrumental in facilitating the effective execution of the work. The construction of a model that can perform the function of an nMOS or a pMOS nanometric operating in a saturated state is facilitated by these. In this model, physical dependencies such as temperature, channel length, and second-order effects are incorporated, ensuring the attainment of continuous expressions for all inversion regions. The model's behaviour is validated against experimental data by means of simulation, thus enabling the evaluation of parameters such as drain current, inversion coefficient, capacitances, transconductances, and response to thermal and flicker noise. This results in an accurate, compact and versatile model, which is suitable for supporting integrated analog circuits designs with a wide range of values for the inversion coefficient.

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ACRONYMS

MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
EKV	Enz-Krummenacher-Vittoz
DC	Direct Current
AC	Alternating Current
NMOS	Negative-channel Metal-Oxide-Semiconductor
PMOS	Positive-channel Metal-Oxide-Semiconductor
QS	Quasi-Static
NQS	Non-Quasi-Static
IC	Inversion Coefficient
ID	Drain Current

Chapter 1

INTRODUCTION

1.1 Background

In the contemporary era, analogue integrated circuits are being utilized with greater frequency in a variety of industrial applications and environments. Consequently, the design of these circuits is subject to constant evolution and progression, with the objective of addressing the demand for reduced power consumption and enhanced energy efficiency. In this context, MOSFET transistors assume a particularly salient role, given their status as the primary active device in the majority of analogue circuits.

It is imperative to exercise a high degree of control over these transistors, given their pivotal role in determining the performance, gain, and linearity of the circuit. This is particularly true when considering the mode of operation of the transistors in different inversion regions, categorized as weak, moderate, or strong.

In order to obtain an accurate and flexible representation of the behaviour of a MOSFET, it is necessary to use compact models that allow continuous simulation in the different operating regions. This will be of vital importance in processes that require advanced technology and lower power consumption. The solution to this growing market need was the development of the EKV model. This model provides a precise description of the second-order effects to which MOSFET transistors are subjected, such as channel length modulation or vertical field mobility reduction, among others.

Concurrently, significant advancements have been made in the analytical modeling of these analogue circuits. Concurrently, languages that implement the description of these circuits, such as Verilog-A, have also advanced. It is possible to implement customized models of different analogue devices for subsequent simulation in environments such as Ngspice or Spectre by utilizing this language. Consequently, Verilog-A has become a versatile and widely utilized language among engineers seeking to develop compact portable models, incorporate tangible effects into existing models, or validate such models against experimental data.

In this context, the present paper focuses on the study, construction and implementation of a compact model of an EKV transistor using the Verilog-A language. The implementation of this process will be facilitated by the utilization of the OpenVAF and Ngspice environments. The objective of this study is to ascertain the behaviour of the MOSFET under various

polarization and temperature conditions. The analysis will extract parameters such as the drain current, capacitances, and transconductances, along with other fundamental operating values, to ensure the effective functioning of an analogue circuit.

In addition to the acquisition of a theoretical and mathematical functional model and the advancement of associated theoretical research, the objective of this work is to utilize this model in professional simulation environments.

1.2 Objectives of Work

The aim of this thesis is to fulfill a series of objectives in order to construct a model correctly and ensure its behaviour. It will also make a suitable contribution to future works.

- Learn to handle the different development environments, OpenVAF and Ngspice. Master the programming languages needed to use them: Verilog-A and SPICE.
- Create a functional Verilog-A model of an nMOS and pMOS transistor operating under saturation conditions and in any inversion region.
- Obtain the operating point of the device, as well as the drain current, main voltages, capacitances and transconductances at different temperatures.
- Prepare the model for use in more complex analogue circuits.
- Verify that the model is functioning correctly through its parameters and variables. Verify that it responds as expected in different environmental situations.

1.3 Outline

The document is divided into chapters where:

Chapter 1 - Introduction: The objectives of the thesis, the concept of the work, and the methodology are introduced.

Chapter 2 - Theoretical Background: An explanation of the technology addressed in this work. This includes the characteristics of the MOSFETs, regions of operation, prominent architectures, and the effects to be considered when modeling the analogue device.

Chapter 3 - Setup Work Applications: Description of how the working applications were prepared. This includes the open server, OpenVAF, and the compatible simulator, Ngspice.

Chapter 4 - Build the Model: Construction of the model. The steps followed to create the Verilog-A model, including the considerations, expressions and parameters used.

Chapter 5 - Simulation and Results: Analysis of the results obtained from the model. Verification of the correct functioning of the code.

Chapter 6 - Conclusions and future work: Presentation of the final conclusions of the work carried out and some proposals for future work.

1.4 Related Work

The following documents have been selected as the primary reference material for this study. In order to achieve a more profound comprehension of the operational mechanics of the EKV model, it is imperative to ascertain the parameters of its essential values. This undertaking is undertaken with the objective of elucidating the effects that exert influence on the model.

1.4.1 Nanoscale MOSFET Modeling: The simplified EKV model for the design of low-power analog circuits

This article introduces the EKV (Enz-Krummenacher-Vittoz) model, a compact and accurate alternative to traditional models for designing the characteristics of MOSFETs in processes requiring the most advanced CMOS technology. It also explains how the inversion coefficient (IC) can be used as an alternative to the over-excitation voltage, the difference in voltage between the gate and the source, and the threshold voltage. The introduction of the inversion coefficient enables the model to be used in weak, moderate, and strong inversion operations. The EKV model is oriented towards nanometer technologies in the saturated state and enables MOSFETs to be characterized with a small number of parameters while maintaining high accuracy in current and transconductance values.

1.4.2 Nanoscale MOSFET Modeling: Using the inversion coefficient as the primary design parameter

This document is a continuation of 'Nanoscale MOSFET Modelling Part 1'. Here, the inversion coefficient is the primary variable used to model analogue circuits with advanced CMOS technology. The simplified EKV design is used for the analysis of the essential variables of analogue circuits, taking into account only the main parameters. These variables are analysed in the three inversion modes: weak, moderate and strong. An attempt is then

made to extract the operating point. In this article, we derive simple expressions for MOSFETs as a function of IC to enable quicker analysis of behaviour, eliminating the need for external simulations. To validate the results, the model is compared with real measurements of devices of various sizes, as well as with the BSIM6 model.

1.4.3 Optimizing Drain Current, Inversion Level, and Channel Length in Analog CMOS Design

This article proposes a methodology for designing analogue circuits in which several parameters can be optimized simultaneously. The inversion coefficient, the drain current and the channel length are optimized here, forming the basis of the rest of the model. This approach provides greater control over the MOSFET inversion regime and enables the simultaneous optimization of power, gain, bandwidth and noise efficiency. The paper also examines channel saturation voltage, voltage and current mismatches, as well as thermal and flicker noise.

1.4.4 Tradeoffs and Optimization in Analog CMOS Design

It presents a methodology for optimizing the design of integrated circuits using CMOS technology. The inversion coefficient is used as the main variable to characterize the devices, with the aim of controlling their performance and power consumption. The study employs the EKV model and empirical data to verify the correct operation of the methodology. The paper also discusses the MOSFET operating plane, which is a visual tool used to determine the optimal operating regions of the MOSFET according to the applicable requirements. Additionally, it analyses how parameters such as transconductance efficiency, velocity saturation, thermal noise density, and flicker density react to different operating points.

1.4.5 The EPFL-EKV MOSFET Model Equations for Simulation

This article presents a compact EKV model of a MOSFET transistor. It has been designed to be compatible with the simulation of more complex analogue circuits. The model focuses on characterizing low-power nanometer MOSFETs so that their behaviour in all inversion regions can be simulated continuously. This is made possible by the mathematical formulation used in the model. Another notable feature is that the model has unique and continuous expressions for the device's various operating modes. The model is structured into two sections: the intrinsic parameters, which describe the behaviour of the transistor; and the

extrinsic parameters, which model the contact resistance, capacitance, and diodes located between the terminals of the MOSFET.

1.4.6 EKV3. MOSFET Compact Model. Model's Documentation

This paper presents an enhanced version of the compact EKV 2.6 model. While it follows the same dynamics as the previous model, it attempts to unify the expressions so that the model can operate across all regions and inversion levels. However, this article improves upon the previous one by implementing a more detailed model that incorporates geometric variation, device mismatch, and other adverse effects that can affect the device. The model also takes into account the presence of intrinsic and parasitic capacitances, as well as leakage currents and temperature influence.

Chapter 2

THEORETICAL BACKGROUND

To realize the design and characterization of a circuit based on MOSFET technology first requires a proper understanding of this technology. The definition of a MOSFET is a field transistor that is used in electronics to amplify the commutation of a signal [1]. The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a devise with a majority of carriers, which can be electrons or voltaic voids depending on whether we talk about a nMOS or a pMOS.

2.1 Construction of a MOSFET

To manufacture a MOSFET device, a series of specific processes must be carried out, but before this it is vital to subject the substrate that will be the basis of the nMOS or pMOS to a series of prior preparation processes.

First of all, the state of the substrate must be checked. In the case of microelectronics applications, it is vital that the substrate has a very high degree of purity. In its natural state, silicon oxide has a purity of 98, 99%, but even this is not enough for the use of the MOSFET, so the level of unwanted impurities must be much lower than the level of impurities that will be intentionally introduced later. Apart from the purity, it must also be taken into account that the manufacturing process can be influenced by the crystalline orientation, in real crystals the surfaces present discontinuities which then affect different factors of the device, and it must also be taken into account that the crystal will present defects, both native and interstitial, which will cause the periodicity of the network to be lost.

One of the processes that must be carried out prior to the manufacture of the device is to obtain purified silicon. To achieve this, a series of chemical and physical processes must be carried out on the silicon. With the chemical processes, polycrystalline silicon can be obtained with a degree of purity of up to 99.999999%. But for the manufacture of MOSFETs, a purity of 99.99999999% is required, so from that point it is necessary to resort to physical processes, such as purification by zones, the nacelle method or the floating zone method.

After obtaining the desired level of purity, it is necessary to transform the semiconductor into a rod-shaped single crystal, with a certain crystalline orientation and type of doping. To achieve this, two different methods are usually used, the Czochralski method and the floating

zone method. The former consists of growing a solid phase on a liquid phase contained in a crucible. The floating zone method is more similar to recrystallization than to growth from a liquid phase, and is therefore more complex than the former, but the profiles obtained are more homogeneous.

The last step before manufacturing the MOSFET would be the preparation of the substrate, first the single crystal must be marked so that its crystalline orientation and the type of doping can be known. Then the single crystal would have to be cut to form the wafers, this is done with special saws whose edge contains diamond powder. Finally, the substrate would have to be polished to remove any remaining damage and defects on the surface, which would be achieved by both mechanical and chemical polishing.

After all the previous processes we can start building a MOSFET, for which we will need to follow a series of steps; diffusion, ionic implantation, epitaxial growth, ... as it's explained in [2] The process is similar for nMOS and pMOS, for a nMOS a subtract type p is needed. Then the subtract is treated through different procedures, first a termical oxidation to form three layers SiO_2, Si_2N_3 and SiO_2. After that a photo-resin is applied and through a lithography process the areas of the drain and the source will be isolating. With a ionic implantation the braking channels are build.

One's you have the braking channels another oxidation is made, leaving inside that layer Si_3N_4 to make sure the oxide don't enter where the transistors should be place. Then the superficial isolating is removed.

The next step is the emplacement of the polysilicon, for that a layer is place and then using again the process of lithography the rest of it is removed leaving only the polysilicon of the gate.

The last step will be a ionic implantation of phosphorous, arsenic and antimony, thanks to which the drain and the source are created. And with that the nMOS will be build, as is shown in figure 2.1.

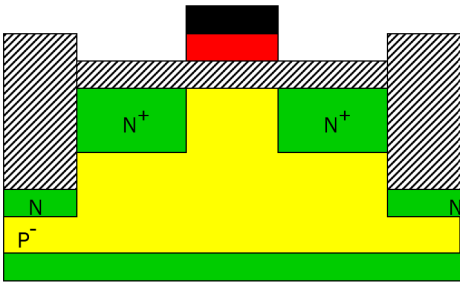

Figure 2.1: Graphical scheme of the layout of a nMOS.

(Maria Cristina Perez Barreiro (2024). "Tema 2: Procesos de Fabricación". *Microelectronics. University of Valladolid.*)

In the other hand, for a pMOS the process is almost the same, the difference is that the pMOS is build from a subtract type n and the ionic implantation is made with boron instead of antimony, arsenic and phosphorous.

2.2 Operation of a MOSFET

Within the MOSFET devices a distinction can be made between nMOS and pMOS, both are majority carrier devices but in the nMOS the carriers are electrons and in the pMOS they are electrons and in the pMOS they are holes. The nMOS devices work in such a way that if the gate voltage is less than the threshold voltage the channel remains cut off, so that the current flowing between the drain and the source is practically zero. However, when the gate voltage is positive with respect to the substrate voltage, electrons appear in the channel and the conductivity increases. In pMOS, on the other hand, the behaviour is analogous: the gate voltage must be negative to cause holes to appear in the channel and thus help with conductivity.

The structure of an nMOS consists of a lightly doped P-type silicon substrate containing two heavily doped n+ regions. Between these two regions, there is a P-type region called the channel, which is covered by a layer of silicon dioxide SiO_2 and a layer of polycrystalline silicon forming the gate. As the oxide layer is insulating, the current from the gate to the channel is practically zero. Due to the symmetry of the structure, there is no physical difference between the drain and the source. The three terminals are located on the surface, and sometimes a fourth terminal is used for the bulk.

Analogous to the nMOS, the pMOS has an N-type substrate, which contains the heavily

doped p-type regions that will be the source and the drain.

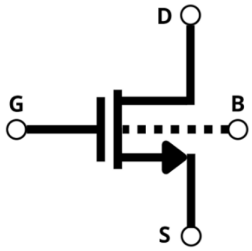

Figure 2.2: Symbol of a nMOS.

(Jorge Iván Cuevas Chávez (2024) "Caracterización eléctrica del circuito sujetador parásito en circuitos CMOS de compuerta cuasi-flotante" *Technological Institute of Cd. Guzmán.*)

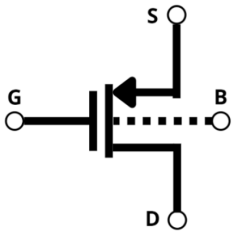

Figure 2.3: Symbol of a pMOS.

(Jorge Iván Cuevas Chávez (2024) "Caracterización eléctrica del circuito sujetador parásito en circuitos CMOS de compuerta cuasi-flotante" *Technological Institute of Cd. Guzmán.*)

Focusing on the general operation of these devices, we will talk in a generic way about the different regions of operation, both about the effects seen in the device in each of these regions and about the conditions in which a MOSFET is found in each of these regions.

If we focus for the moment on the behaviour of an nMOS, we know that the two most basic concepts for it to work correctly are that it is necessary to apply a positive voltage between the drain and the source and that if the voltage between the gate and the source is zero, no current flows through the channel because the drain and the source are isolated. However, when a voltage starts to be applied to the positive gate with respect to the source, we know that an electric field starts to appear which repels the holes and attracts the electrons towards the gate, thus increasing the conductivity of the channel. Thus, when this voltage continues to increase, there comes a point where the bulk area under the gate is no longer P-type and becomes N-type due to the dense accumulation of electrons. At this point the channel is created between the drain and the source and the current is allowed to flow. Once the channel is created, with a suitable voltage V_{ds}, current will exist between the drain and the source, until the voltage becomes so great that the channel recedes from the vicinity of the drain. This is known as the saturation region and will be the conditions under which we work here.

2.2.1 Sub-threshold Region

Looking at the different situations mentioned above, we will start with the sub-threshold region. the transistor is in this area as long as there is no channel formed between the drain and the source, which is always the case when the voltage between the gate and the source is less than the threshold voltage. However, within this region we can also find different situations, we find the accumulation region, the depletion region and the inversion region, which differ from each other according to the value of the voltage between the gate and the source.

2.2.1.1 Accumulation Zone

Looking at the different situations mentioned above, we will start with the accumulation zone. This is when the voltage V_{gs} is well below the threshold voltage and negative, in this region the bulk structure remains in its initial distribution, like its show in the figure 2.4. In this situation the MOS structure can be seen as a capacitance associated with the gate due to the oxide separating the gate and the semiconductor. This capacitance is called the specific oxide capacitance per area unit C_{ox}, and we will see that this capacitance affects the rest of the behaviour of the MOSFET. The specific oxide capacitance per area unit is given by Equation 2.1 [3], where ε_{ox} is the permittivity of the oxide and X_{ox} is the width of the oxide.

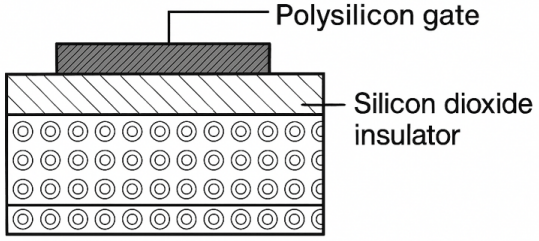

Figure 2.4: Graphical scheme of the MOSFET Accumulation zone.

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.1}$$

In this region, as already mentioned, we work with negative gate voltages, so due to the field created in the oxide by this voltage, the majority carriers are attracted and concentrate at the

junction between the oxide and the semiconductor. Due to this polarization, the MOSFET behaves like a capacitor.

Another concept associated with this is the total oxide capacitance of a given transistor C_{ox} which results from the product of the specific oxide capacitance per unit area and the actual area of the transistor under consideration, Equation 2.2 [3].

$$C_{ox} = C'_{ox} \cdot L \cdot W \tag{2.2}$$

2.2.1.2 Depletion Zone

If the voltage between the gate and the source continues to increase, the accumulation zone is left behind and the depletion zone is entered. This is so called because the voids that were previously next to the oxide are now repelled towards the bottom of the bulk, thus creating a charge-free region or depletion zone, as you can see in the figure 2.5. In this area of operation, the voltage between the gate and the source is positive, but still below the threshold voltage.

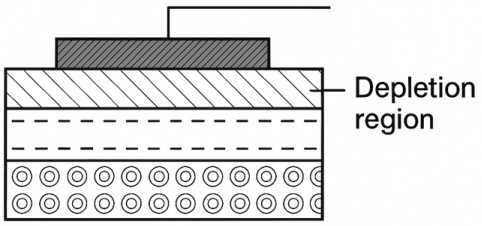

Figure 2.5: Graphical scheme of the MOSFET Depletion zone.

The increased voltage creates an electric field in the oxide, called ε_{ox}, which points to the bulk and also creates a field that penetrates the semiconductor ε(x). The electric field generates a voltage in the crystal that will be maximum at the surface, and decreases to zero ($V_b = 0$) at the bottom of the crystal.

The electric field in the crystal acts on the carrier concentration, especially at the surface. Due to the effect of the electric field, the emptiness zone extends to a depth X_d. This region, without free carriers, has only uncovered charges and is called the space charge. The width of the vacancy zone can be calculated using the one-dimensional Poisson solution for an abrupt junction, giving the Equation 2.3 [4], where ε_{si} is the permittivity of silicon, ϕ_s is the

potential at the crystal surface, q the electron charge and Na is the initial concentration of the P-type crystal.

$$X_d = \sqrt{\frac{2\,\varepsilon_{\mathrm{si}}\,\phi_s}{q\,N_a}} \tag{2.3}$$

On the other hand, the space charge can then be calculated as shows Equation 2.4 [5]. This space charge, in series with oxide capacitance C_{ox}, determines the gate-substrate capacitance curve in small-signal analysis, modeled as two capacitors in series.

$$Q_{B0} = -q\,N_a\,X_d = -\sqrt{2\,\varepsilon_{\mathrm{si}}\,q\,N_a\,\phi_s} \tag{2.4}$$

The MOSFET drain zone is therefore a direct analogy to the depletion region of a reverse biased PN junction, and plays a key role in determining the threshold voltage, input capacitance and body effect when there is source-substrate biasing. Once we know this, we could define the tension in the oxide with Equation 2.5 [4].

$$V_{ox} = -\frac{Q_{BO}}{C'_{ox}} \tag{2.5}$$

2.2.1.3 Inversion Zone

By further increasing the voltage between the gate and the source until it is higher than the threshold voltage V_t, we enter the inversion zone. Here the electrons are attracted to the region of the substrate under the gate, creating an N-type zone which will become the channel of the device and link the drain to the source, as shown in the figure. Therefore, we know that the absolute voltage to be applied to create the channel is the difference between V_{gs} and the threshold voltage. In this situation, if we were to apply voltage between the drain and the source, current could flow through the channel.

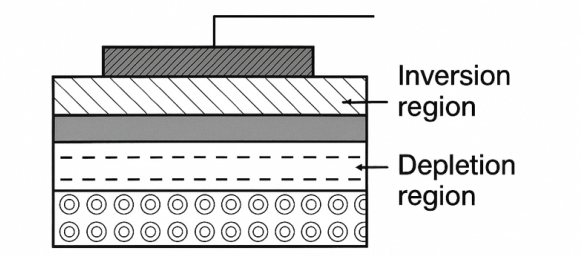

Figure 2.6: Graphical scheme of the MOSFET Inversion zone.

Under these conditions, if no voltage V_{ds} is applied the channel would be symmetrical along its entire length.

Once we enter the inversion zone and as the voltage value between the gate and the source increases, the width of the depletion zone X_d also increases. However, this zone does not grow indefinitely, but there comes a point where the field at the junction between the oxide and the substrate is so large that it causes free electrons to be directed towards the junction. When the inversion occurs, the potential at the crystal surface reaches a value called ϕ_{si}, which depends on the doping level of the crystal.

To quantify this process, the Fermi potential of the bulk is used, which satisfies the following Equation 2.6, where *ni* is the intrinsic density. Strong inversion is reached when the ϕ_{Si} potential doubles the value of the Fermi potential. When this condition is fulfilled, the formation of the channel under the gate of the MOSFET device starts, and it is at this moment that the depletion region reaches the maximum width X_d.

$$|\phi_F| = \left|\frac{K \cdot T}{q}\right| \cdot ln(\frac{Na}{ni}) \tag{2.6}$$

Analogously to this, we know that the maximum space charge will be given when the maximum width of the depletion region is reached, Equation 2.7, so its value will be that of the following Equation 2.8 [4].

$$X_{dm} = \sqrt{\frac{2\,\varepsilon_{\mathrm{si}}}{q\,N_a}\,2\,\phi_F} \tag{2.7}$$

$$Q_{B0,\mathrm{max}} = -\sqrt{2\,\varepsilon_{\mathrm{si}}\,q\,N_a\,2\,\phi_F} \tag{2.8}$$

It is also known that as the voltage from the gate to the source value increases above the threshold voltage value, more inversion electrons will accumulate, whose charge is represented by QI, so that the total charge density will also increase and will follow the Equation 2.9 [6].

$$QS = Q_{BO,\max} + QI \tag{2.9}$$

Once we know this we can determine the value of the gate voltage that generates the inversion process, this value will be called V_{t0} and will follow the Equation 2.10 [6].

$$V_{t0} = V_{ox} + \phi_{Si} \tag{2.10}$$

At the start of the inversion there are almost no free electrons so the charge due to these QI will be very small compared to the space charge, $QI << Q_{BO}$. Knowing this we can conclude that at this point the surface charge density is equivalent to the space charge, so the oxide tension in the depletion zone at this point will be as follows in Equation 2.11 [6].

$$V_{OX} = -\frac{Q_S}{C'_{ox}} = -\frac{Q_{B0,\max}}{C'_{ox}} = \frac{\sqrt{2\,q\,\varepsilon_{\text{si}}\,N_a\,2\,|\phi_F|}}{C'_{ox}} \tag{2.11}$$

If we also want to take into account the charges that will appear on the oxide, we have to add the concept of the flatband voltage VFB. This takes into account the charges on the oxide and the MOS interface, and also the difference between the work functions of the metal and the semiconductor. Therefore, if we put all these concepts together, we can obtain the gate voltage generated by the inversion process, Equation 2.12 [6].

$$V_{T0} = V_{FB} + \frac{\sqrt{2\,q\,\varepsilon_{\text{si}}\,N_a\,2\,|\phi_F|}}{C'_{ox}} + 2\,|\phi_F| \tag{2.12}$$

Therefore, as can be understood from the above, the sub-threshold region is characterized by a lack of current between the drain and the source, and by a voltage from the gate of

the MOSFET device to the source terminal that is less than or at best equal to the threshold voltage, hence the name of this particular operating region.

2.2.2 Linear Region

Having already discussed the sub-threshold or cutoff region, we can move on to the next operating region. This is where the most optimal conditions for the normal operation of the device are found, it is also the region of operation where it is easiest to predict the behaviour of the MOSFET device you are dealing with. This phenomenon can be attributed, in large part, to the observation that, within the linear region, the current traversing the I_{ds} channel exhibits a linear relationship with the voltage differential between the drain and the source, as the nomenclature would suggest.

Once the voltage between the gate and the source is high enough to be in inverting mode, if a voltage is applied between the drain and the source we obtain a current that goes from one terminal to the other. It is at this point that the device enters the linear region of operation.

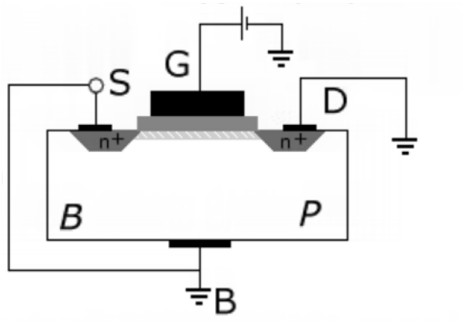

Figure 2.7: Graphical scheme of the MOSFET Cut-off region.

(Vicente García. (2012) "El Transistor MOSFET. Electrónica Práctica Aplicada". *https://www.diarioelectronicohoy.com/blog/el-transistor-mosfet*)

Within this linear region, it is known that as the voltage V_{ds} increases, the shape of the channel changes. As previously mentioned, the channel is formed in the inversion mode, in which, as there is no voltage between the drain and the source, the channel is symmetrical throughout its length, having the same width both in the area close to the drain and the area close to the source, as you can see in the figure 2.7. However, in the linear region, as there is already a voltage V_{ds}, the part of the channel in the vicinity of the drain becomes narrower, but the original channel length remains as the figure 2.8 show.

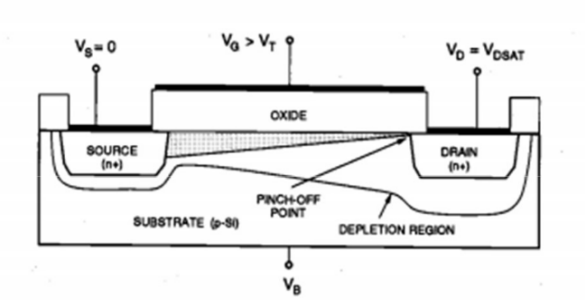

Figure 2.8: Graphical scheme of the MOSFET lineal region.

(Diego Mallada Morales. "Modelado y caracterización del transistor MOSFET: Extracción de parámetros". *University of Valladolid. Science Department.*)

This phenomenon occurs because, on the side of the channel in closest proximity to the source terminal, the field used to create the channel is always worth the difference between the voltage V_{gs} and the threshold voltage. As previously mentioned, this value is the one used to create the channel in inversion mode, meaning that the width of the channel does not vary on the source side. Conversely, in the vicinity of the drain, the voltage that maintains the channel is no greater than the difference between the gate and the drain. Consequently, as the V_{ds} voltage increases, the channel becomes narrower.

It can be deduced from the available evidence that, while provided Equation 2.13 is satisfied the channel will maintain its original length [6].

$$V_{gs} - V_t > V_{ds} \tag{2.13}$$

In the event of the expression becoming unfulfilled due to an excessive increase in the voltage V_{ds}, it can be deduced that the voltage V_{gd} will be less than the threshold voltage. Consequently, the channel will move away from the drain, thereby initiating a decrease in the effective length of the channel. It is at this particular point that the device enters the saturation region.

As previously established, the linear region is characterized by the maintenance of constant channel length. This results in the formation of a continuous channel, which is predominantly influenced by the majority carriers. This is applicable to both nMOS electrons and pMOS holes. In this region of operation, the surface potential never cuts the channel, so that, as previously mentioned, the current between the drain and the source will be proportional to the voltage V_{ds} for a given voltage V_{gs}.

Consequently, it can be deduced that the equation for the drain current in this region is given by Equation 2.14 [3].

$$I_D = \mu\, C'_{ox}\, \frac{W}{L} \left[(V_{GS} - V_{th})\, V_{DS} - \tfrac{1}{2}\, V_{DS}^2 \right] \tag{2.14}$$

In this regime, the channel of the MOSFET device is to be considered as a block of silicon, the conductivity of which is governed by the Equation 2.15 [4], where $n(x)$ is the density of the majority carriers, which is dependent on the gate voltage. In the event of the application of a negligible voltage, V_{ds}, the voltage drop is distributed uniformly along the entire length of the channel, resulting in the attainment of a channel resistance, R_{on}, as per the Equation 2.16 [4].

$$\sigma = q\, \mu_n\, n(x) \tag{2.15}$$

$$R_{\text{on}} \approx \frac{1}{\mu_n\, C'_{ox}}\, \frac{L}{W\, \left(V_{GS} - V_{th}\right)} \tag{2.16}$$

In a more practical setting, MOSFETs in linear mode can be used as variable resistors controlled by the gate terminal. However, to ensure the stability of the device, it is imperative to maintain a constant voltage between the drain and the small source, thereby preventing the occurrence of saturation.

2.2.3 Saturation Region

The final region of operation is the saturation region. The MOSFET device enters this region when the Equation 2.13 is no longer fulfilled. It can thus be concluded that, in the event of the MOSFET being in saturation, the channel will have moved away from the vicinity of the drain, as demonstrated in the accompanying figure 2.9. These conditions will be the ones with which we will engage in the following sections of this paper, dealing with nMOS and pMOS devices under saturation conditions.

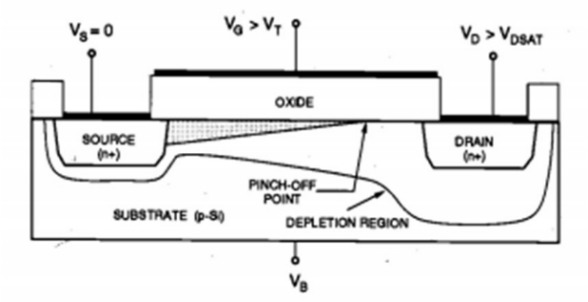

Figure 2.9: Graphical scheme of the MOSFET Saturation region.

(Diego Mallada Morales. "Modelado y caracterización del transistor MOSFET: Extracción de parámetros". *University of Valladolid. Science Department.*)

Despite the reduction in channel length, it is understood that the current between the drain and the source does not vanish due to the free electrons departing the channel being attracted by the high voltage of the drain, thus traversing the depletion zone. This effect ensures that the voltage between the drain and the source remains practically constant. The reason for this is that if the voltage V_{ds} increases, the length of the channel decreases. This, in turn, results in an increase in the resistance and the force with which the electrons are attracted to the drain.

Therefore, in circumstances where the device is operating in saturation, the current flowing between the drain and the source is subject to control by the gate voltage. It is evident that, in the event of a fixed V_{ds} voltage and a fixed gate voltage, the current would be governed by a number of factors. These include the distance between the drain and the source, the width of the channel, the threshold voltage, the width of the oxide itself, the dielectric coefficient of the gate, and the mobility of the carriers in the device.

In a manner analogous to the linear operating region, within the saturation region the drain current is governed by the Equation 2.17 [3]. However, if the dependence of V_{ds} on the reduction of the effective channel length is to be incorporated into this relationship, the so-called channel-length modulation parameter, λ, can be included to form the Equation 2.18.

$$I_{D,\text{sat}} = \frac{1}{2}\,\mu_n\,C'_{\text{ox}}\,\frac{W}{L}\,(V_{GS} - V_{th})^2 \tag{2.17}$$

$$I_D \approx I_{D,\text{sat}}\left[1 + \lambda\,V_{DS}\right] \tag{2.18}$$

In this paper, the focus is on the saturation conditions of short-channel devices, and it is argued that this focus enables the discovery of a number of additional effects on the behaviour of the devices.

2.2.3.1 Drain-Induced Barrier Lowering

In the context of short-channel MOSFET devices operating in the saturation region, a range of effects must be taken into consideration, including, but not limited to, Drain-Induced Barrier Lowering (DIBL). This effect can be expressed as follows: an increase in the voltage between the drain and the source results in a decrease in the effective threshold voltage [7].

The phenomenon can be attributed to the fact that, in nanometric technologies, the distance between the drain and the source is excessively small. This results in the electric field generated in the vicinity of the drain affecting the source by reducing the potential barrier at the end of this, and consequently increasing the leakage current. This indicates that the electric field, when specified, exerts an influence on the source, thereby facilitating the flow of free electrons from the source to the drain, obviating the necessity for an increase in gate voltage.

Therefore, in compact models, the DIBL can be quantified by this slope, Equation 2.19.

$$\text{DIBL} \;=\; -\frac{\Delta V_{th}}{\Delta V_{DS}} \tag{2.19}$$

In a similar manner, the threshold voltage of short-channel devices is affected, necessitating the reformulation of its expression to yield the Equation 2.20.

$$V_{th}(V_{DS}) \;\approx\; V_{th0} \;-\; \text{DIBL} \;\cdot V_{DS} \tag{2.20}$$

In summary, short-channel MOSFETs operating in the saturation region are subject to the following adverse effects, which are a consequence of the DIBL effect. It can thus be concluded that the control previously exerted by the gate on the behaviour of the drain current is now being assumed by the voltage at the drain terminal itself. This has the effect of causing the sub-threshold swing to degrade and the leakage current to rise exponentially.

Consequently, there is a shift in the $I_d - V_{gs}$ characteristic curve, moving it towards lower gate values.

A further deleterious effect is the reduction of the analogue gain, because the DIBL increases the value of the output conductance gds, which in turn reduces the intrinsic gain of the MOSFET device, in other words the transconductance of the device between the output conductance g_m/g_{ds}. This has been demonstrated to result in a deterioration in the performance of small-signal amplifiers.

Finally, it is important to note that there exist techniques capable of mitigating the impact of Drain-Induced Barrier Lowering in short-channel devices. The most straightforward solution to this problem would be to use devices with a longer channel length. However, if the utilization of short-channel devices is deemed advantageous due to the characteristics they offer, advanced architectures such as FinFET, FDSIO or SOI can be employed.

The capacity of architectures such as FinFETs to mitigate the effects of DIBL is attributable to their geometric design. FinFETs incorporate an 'envelope gate' that enhances the electrostatic control of the channel, thereby minimizing the impact of the electric field of the drain on the source, in comparison to alternative architectures. In a planar MOSFET, the gate only exerts influence in the upper region of the channel. This enables the drain field to pass underneath and affect the source potential barrier, as previously outlined.

However, in the case of a FinFET, the channel is formed by a very thin layer of silicon that the gate surrounds on up to three sides. This configuration is known as a multi-gate configuration. This novel approach entails the utilization of the gate field to regulate the potential across the entirety of the channel area. Consequently, the depletion zones in the vicinity of the drain are confined to that specific area, thereby precluding the possibility of extension towards the source [8].

Furthermore, in these devices, there is a reduction in both the channel thickness and the effective channel length. However, the latter is maintained at a relatively short, controlled distance, thereby ensuring that the drain and source remain electrostatically isolated from each other.

This effect therefore has important implications when it comes to short-channel devices, but effective solutions have also been found.

2.2.3.2 Saturation Velocity

In the context of short-channel MOSFET devices operating in the saturation region, an additional effect that warrants consideration is the effect of saturation velocity.

The phenomenon under discussion can be traced back to the electric field that is generated in the channel when there is a significant voltage difference between the drain and the source. The electric field thus engenders a cessation of linear acceleration in the carriers within the channel, i.e. electrons in the case of nMOS and holes in the case of pMOS, resulting in the attainment of a limiting velocity. This limiting velocity is a material property of the channel and is denoted as the saturation velocity v_{sat}.

The critical electric field, denoted E_c, is the value of the electric field at which the velocity of the carriers is expressed by the following Equation 2.21 [4]. This relationship is linear, with a slope that corresponds to the mobility of the carriers in the channel.

$$V_d = \mu_o \cdot E \tag{2.21}$$

However, at values of the electric field that exceed a critical threshold, the collisions of the free carriers become exceedingly frequent. Consequently, they are unable to gain additional energy from the field, resulting in the cessation of their acceleration and the subsequent stagnation at the saturation velocity. As previously outlined, the saturation velocity may be expressed as by Equation 2.22, where E_c is defined as the critical electric field. This limitation in velocity signifies that the value of the drain current ceases to increase as the voltage between the gate and the source rises.

$$V_{sat} = \mu_o \cdot E_c \tag{2.22}$$

Therefore, in circumstances where the carriers are moving at saturation velocity, the drain current will be governed by the Equation 2.18.

$$I_{D,sat} \approx W\, C'_{ox}\, v_{sat}\, (V_{GS} - V_{th}) \tag{2.23}$$

In the case of the ekv models, the creation of a parameter L_{sat}, has been observed. This is defined as the length of the channel at the saturation rate. This is given by the Equation 2.24 [9]. It is imperative to emphasize that the primary rationale for the necessity of this parameter is predicated on the scaling of λ_c, which is to be followed in accordance with the Equation 2.25 [9].

$$L_{sat} = \frac{2\,\mu_n\,U_t}{v_{sat}} \tag{2.24}$$

$$\lambda_c = \frac{L}{L_{sat}} \tag{2.25}$$

In order to adapt the value of the inversion coefficient to this situation, it is necessary to set λ_c as a function of the channel length at the saturation rate.

It is evident that the saturation speed regime exerts a significant influence on the transconductance of the MOSFET, as evidenced by the proximity of its value to attaining a certain degree of independence from the channel length. This assertion is substantiated by the Equation 2.26 [9].

$$g_{m,sat} \approx W\,C'_{ox}\,v_{sat} \tag{2.26}$$

Consequently, it can be posited that the saturation rate functions as a physical limit on both current and gain for these devices, compelling integrated circuits designers to meticulously evaluate the trade-off between channel length, carrier mobility and saturation rate, with a view to optimizing the device to the greatest extent possible and thereby maximizing performance.

2.2.3.3 Hot Electrons Degradation

The final phenomenon for the saturation region that will be discussed is the degradation of hot carriers. In MOSFET devices, this phenomenon occurs when some electrons or holes, depending on the device type, acquire sufficient kinetic energy to overcome the potential barriers when exposed to strong electric fields.

The ability of these carriers to penetrate the dielectric of the gate oxide is dependent on their capacity to overcome the potential barriers that are in place. The effect of this phenomenon is detrimental to the standard operation of the MOSFET device, since the presence of hot carriers instigates substantial leakage currents and engenders a permanent alteration in the characteristics of the transistor.

The most significant effects of hot carrier degradation are threefold. Firstly, the gate threshold voltage is displaced. Secondly, the device's own transconductance is lost. Thirdly, and as mentioned above, the leakage current increases markedly.

As previously mentioned, it should be noted that the effect is exacerbated by decreasing the length of the gate. Technologies with a length of less than 100 nanometers are particularly impacted by this effect. In such conditions, it can be observed that the presence of elevator fields in the pinch-off region serves to enhance the generation of hot carriers. This, in turn, results in the voltage between the drain and the source becoming non-linear, thereby reducing the operational lifespan of the MOSFET.

This effect has prompted integrated circuit designers to explore methods for reducing the drain voltage, thereby preventing the formation of such substantial electric fields. In the field of semiconductor engineering, certain solutions have been proposed, including the design of slightly doped drainers and the utilization of architectures such as FinFET.

In order to measure the damage caused by this effect, certain tests can be performed to check the accelerated aging of the devices. The experimental setup involves the application of high voltage pulses, both V_{gs} and V_{ds}, and the subsequent measurement of the evolution of threshold voltage, transconductance and leakage current over time. The process of extraction enables the subsequent extraction of a series of parameters, which in turn facilitate the prediction of the device's lifetime. A comparison of these parameters with empirical model values is then possible.

In practice today, these devices are utilized in saturation mode when a stable drain current is required in analogue applications, such as current sources or linear regulators.

2.2.4 Breakdown Region

It is imperative to note that the breakdown operating region is an undesirable state to avoid entering. The primary characteristic of this phenomenon is that the voltage between the drain and the source V_{ds} exceeds a critical value. This results in the saturation region being left behind, and the MOSFET ceases to behave as a gate-controlled switch. Instead, it enters a state of punch-through.

Avalanche breakdown is characterized by the presence of a high density of free electrons, which, when interacting with silicon atoms, results in the generation of additional electron-hole pairs. This phenomenon can be likened to that of hot electrons, exhibiting a similar effect. It is evident that this process is characterized by an increase, resulting in a substantial rise in drain current, even in the absence of gate voltage. The voltage V_{ds} at which this occurs is contingent on the technology employed and is typically specified by the manufacturer, as this scenario can result in irreversible damage to the device. An illustration of this phenomenon is the generation of irreversible defects in the transistor material when the avalanche current overheats the oxide and silicon.

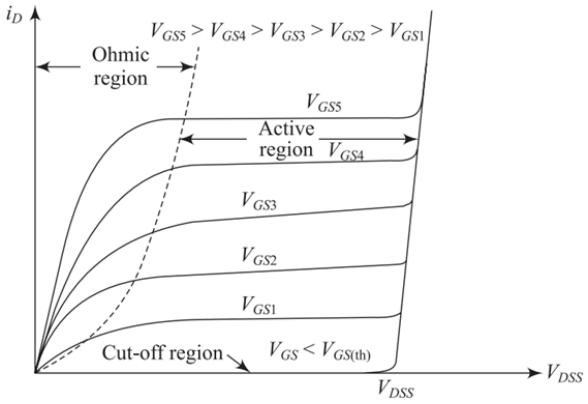

Figure 2.10: MOSFET Characteristic curve.

(S Rvivarman. "I-V Characteristics of Power MOSFET".
https://sravivarman.com/technical-articles/i-v-characteristics-of-power-mosfet/)

Conversely, an examination of the characteristic curve, figure 2.10, of the MOSFET reveals the breakdown region with clarity, situated after the active or saturation region where the current remains constant. However, it is when the current reaches this operating zone that the drain current is suddenly triggered.

2.3 Second Order Effects of a MOSFET

As previously mentioned, MOSFETs have a number of operating regions, each with its own characteristics. The device's behaviour, the equations used to describe its characteristics, and its functionality can all vary from one region to another. However, in addition to understanding the operating regions, it is important to consider some effects that can alter the expected behaviour of MOSFETs.

We will now take a closer look at some of these effects, such as the subthreshold current effect, mobility variation and the body effect.

2.3.1 Subthreshold Current Effect

To more accurately model a MOSFET device, it is important to consider the sub-threshold current. This unwanted diffusion current occurs when the device is in the cutoff region, where theoretically no current should be flowing through the device. This behaviour is particularly significant in nanometric MOSFETs because their small size exacerbates non-ideal effects such as sub-threshold currents.

This current originates when the voltage between the gate and the source is lower than the threshold voltage, or what is the same, when the device is in the cutoff region, as explained above. Under these conditions, no current should flow through the device because the channel has not yet formed. However, due to the high electron concentration gradient at the source and low gradient in the channel, a diffusion current appears, which is favored by the applied voltage V_{ds}.

This sub-threshold current exhibits exponential behaviour with respect to the voltage between the gate and the source. In the sub-threshold region, carrier transport occurs by diffusion between the source and drain terminals through the charge concentration. This concentration is insufficient to form the channel, but sufficient to create this undesired effect. Therefore, the sub-threshold current can be expressed by the Equation 2.27 [10], where n is the ideality factor, which depends on the oxide and channel capacities. This expression clearly demonstrates the exponential nature of the sub-threshold current as a function of the voltage between the gate and the source.

$$I_{DS} \approx I_0 \cdot e^{\frac{(V_{GS}-V_{th})}{n \cdot U_t}} \tag{2.27}$$

A notable parameter associated with this behaviour is the subthreshold slope. This parameter establishes the point at which the voltage between the gate and the source must be increased for the subthreshold current to increase by one decade. This behaviour follows the Equation 2.28 [10]. Ideally, the theoretical minimum value should be 60 mV per decade at room temperature; however, due to imperfections and the side effects of real devices, this value increases to 100 mV per decade. This parameter can also be used to determine a device's actual ability to shut down effectively.

$$S = \frac{dV_{GS}}{d(\log_{10} I_{DS})} = n \cdot \ln(10) \cdot U_t \tag{2.28}$$

The emergence of subthreshold current not only causes an effect outside the ideal characteristics of the transistor, but also static power consumption. This occurs during the device's inactive states, when it should theoretically not consume resources. This has forced designers to create tools, such as power gating, to reduce the effects.

However, this effect has also been exploited in circuits where power requirements are very low and speed is not critical, forcing devices to operate in the subthreshold region.

2.3.2 Variation of Carrier Mobility

Another important factor to consider when characterizing a MOSFET device is the variation in carrier mobility across the substrate. This will be electrons in the case of nMOS and holes in the case of pMOS. Mobility is represented as μ and appears explicitly when calculating the current through the channel, making it important in terms of device operation. The higher the mobility, the greater the current that will flow through the channel to maintain a fixed voltage value between the drain and the source.

However, although mobility is a material-related characteristic, it also varies depending on a number of physical and technological factors.

Logically, one of the main factors affecting carrier mobility is the type of carrier involved. Electrons in silicon are much more mobile than holes, almost twice as mobile, which is why nMOS and pMOS devices are often preferred, since the latter are slower.

Another important factor affecting carrier mobility is temperature. As temperature increases, the vibration of the crystal lattice also increases, leading to more collisions between the carriers and reducing their mobility. Therefore, the mobility of the carriers is related to

temperature by the Equation 2.29 [10]. The exponent varies depending on the material and the type of carrier, for electrons in silicon, for example, it would be 2.4, whereas for holes it would be 2.2. This explains why MOSFETs are slower and consume more power when they heat up, so care should be taken with operating conditions.

$$\mu(T) \propto T^{-m} \tag{2.29}$$

In the figure 2.11 you can see graphically how the mobility of the carriers decrease when the temperature increase.

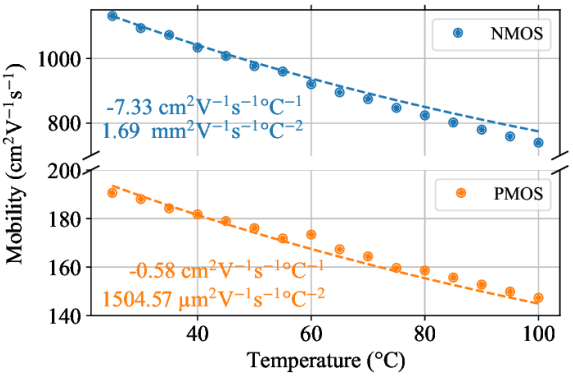

Figure 2.11: Mobility versus temperature MOSFET characteristic.

(Nicolas Roisin, Thibault Delhaye, Nicolas André and Denis Flandre. (2022) "Low-Power Silicon Strain Sensor Based on CMOS Current Reference Topology." *Institute of Information and Communication Technologies, Electronics and Applied Mathematics. Belgium.*)

Similarly, the concentration of impurities in the device substrate also influences electron mobility. In areas with a higher concentration of dopers, there are more scattering centers for electrons or holes. This increases the number of shocks and deflections, reducing the velocity of the current and, consequently, the mobility. This problem arises during the fabrication process and is exacerbated in the source and drain areas due to the high level of doping; therefore, special care must be taken in these areas.

Another factor to consider is the thickness and quality of the oxide layer and the interface. Thinner oxide makes it easier to control the channel; however, the electric field generated in the channel is also more intense, increasing collisions and reducing mobility. The presence of structural defects in the crystal also reduces the mobility of the crystal's carriers.

We can see that modeling mobility realistically can be a complex task as it is a nonlinear function dependent on many parameters such as voltages V_{gs} and V_{ds}, temperature and

manufacturing characteristics. One model that can handle this is the Berkeley Short-channel IGFET Model ,BSIM , which considers dependence on the electric field and temperature, as well as surface roughness and other short-channel effects.

2.3.3 Body Effect

The body effect occurs when there is a non-zero voltage between the source and substrate of a MOSFET device. In calculations, this voltage is usually set to zero, but for some applications, it is necessary to apply a voltage between these two terminals. This results in the so-called body effect.

Having a non-zero voltage between the source and the substrate V_{bs} is similar to reverse biasing the N+P junction. This increases the depletion zone, which was previously only due to the gate voltage. Consequently, the damping zone under the gate is also modified, as is the space charge. The new expression for the space charge is therefore given by Equation 2.30 [6].

$$Q_B = -\sqrt{2 \cdot \varepsilon_{\text{si}} \cdot q \cdot N_a \cdot (2 \cdot |\phi_F| + V_{SB})} \tag{2.30}$$

Varying the value of the space charge modifies the device's threshold voltage, which now follows the Equation 2.31 [6]. This considerably modifies the device's characteristics because the minimum gate voltage required for a channel to form between the drain and source increases.

$$V_T = V_{FB} + \frac{\sqrt{2 \cdot \varepsilon_{\text{si}} \cdot q \cdot N_a \cdot (2 \cdot |\phi_F| + V_{SB})}}{C'_{\text{ox}}} + 2 \cdot |\phi_F| + \frac{q \cdot D_i}{C'_{\text{ox}}} \tag{2.31}$$

The above expression can also be written as Equation 2.32 [6] if part of it is replaced by the parameter representing the polarization coefficient of the substrate, γ, Equation 2.33 [6].

$$V_T = V_{T0} + \gamma \left[\sqrt{2 \cdot |\phi_F| + V_{SB}} - \sqrt{2 \cdot |\phi_F|} \right] \tag{2.32}$$

$$\gamma = \frac{\sqrt{2 \cdot \varepsilon_{\text{si}} \cdot q \cdot N_a}}{C'_{\text{ox}}} \tag{2.33}$$

From a practical point of view, this effect can have positive and negative consequences. Increasing the threshold voltage increases the gate voltage at which the current can flow through the channel, thus decreasing the efficiency of the MOSFET. Additionally, the body effect complicates the design of integrated circuits, as different bulk biases can alter the threshold voltage values within the same circuit.

However, this effect can also be exploited. Back-biasing is an integrated circuit design method that involves changing the bulk voltage to dynamically adjust the threshold voltage. This reduces power consumption, for example, when the circuit does not require high speed.

Furthermore, as will be seen below, there are already architectures that electrically isolate the substrate, greatly mitigating the body effect. One example is the Silicon-On-Insulator (SOI) architecture.

2.3.4 Impact Ionization

Impact ionization represents a significant second-order effect that manifests in MOSFET devices. The process under discussion involves the accumulation of a significant quantity of energy by hot electrons, which subsequently collide with substrate atoms and the drain. This results in the creation of unwanted currents.

The effective channel length is reduced when a pMOS or nMOS reaches the saturation region, as the voltage between the drain and the source increases. Under these conditions, impact ionization occurs.

Impact ionization is defined as the process in which the presence of a high voltage, the voltage between the drain and the source, at saturation results in the generation of a substantial electric field by the drain, thereby inducing a significant number of free electrons to accumulate energy. This stored energy originates from the impacts, with a greater number of collisions resulting in a greater energy output. When the accumulated energy between collisions exceeds the ionization threshold, E_{ion}, the creation of hot electrons occurs. In silicon, the ionization threshold is typically in the order of 3.6 electron volts (eV).

The electrons in question have been observed to accelerate and subsequently collide with substrate and drain atoms. The result of this interaction is that the electrons are so energetically excited that they are capable of extracting an electron from the valence band, thereby creating an electron-hole pair.

The most undesirable effect of these new electron-hole pairs is that the hole is attracted by the negative substrate polarization, creating an unwanted substrate current. Conversely, the

electrons are attracted by the positive gate voltage, thereby creating an additional undesirable current.

This effect assumes particular significance in nanometric devices, given the impact of the diminutive channel length on the extent to which the drain electric field exerts influence on the remaining device elements.

One of the parameters that is utilized in order to measure the aforementioned effect is the impact ionization coefficient, denoted by the letters α for electrons and β for holes. This coefficient is indicative of the number of ionization that occur per unit distance traversed in the device material. The value of the parameter in question is found to be dependent upon the electric field, and is governed by the Equation 2.34 [10], where A and B are empirically obtained constants that are found to depend on the material being treated.

$$\alpha(E) = A \cdot e^{-B/E} \tag{2.34}$$

In order to estimate the importance of the effect of hot electrons on the device under consideration, measurements of the current through the substrate are taken. Conversely, holes are typically less problematic due to their comparatively low mobility, as previously outlined in relation to electrons.

Nevertheless, impact ionization is problematic as it ultimately results in the degradation of MOS device parameters, affecting the threshold voltage, the sub-threshold current, the transconductances, and leading to permanent damage to the device. Consequently, this phenomenon has prompted device engineers to explore methodologies aimed at reducing the drain voltage.

2.3.5 Modulation of the Channel Length

Finally, an effect that is also of great significance and more in the field to be discussed in this paper is the modulation of the channel length in nanometric MOSFETs in the saturated state.

From an ideal point of view, the channel length is constant. As previously outlined in the saturation region, the voltage between the gate and the drain is lower than the threshold

voltage. That is to say, the gate voltage exceeds the threshold voltage, thus allowing the channel to form. However, the voltage between the drain and the source is so high that the depletion zone of the drain extends until it reaches the gate. This results in the channel being cut and its effective length being reduced. As the voltage on the drain increases, the channel will become smaller and smaller. This decrease in channel length has been shown to cause an increase in drain current. The resistance of the channel is reduced as it becomes shorter, and the voltage between the drain and the source is applied over a shorter distance.

This effect is more pronounced in a short channel device, as the effect of the electric field of the drain on the source is greater.

Consequently, it can be deduced that the modulation of the channel length exerts an influence on the current, a factor that must be considered when modeling the device. The Equation 2.35 [10] for the current flowing through the MOSFET channel is derived from the necessity to account for this phenomenon. The modulation coefficient of the channel length, denoted by λ_c, is a function that is influenced by various factors, including the saturation length of the channel.

$$I_D = \frac{1}{2}\mu C'_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda_c V_{DS}) \tag{2.35}$$

Consequently, the MOSFET can no longer be regarded as a constant current source with an infinite output impedance; rather, it possesses a finite output impedance. This phenomenon is illustrated by the positive slope in the I_d/V_{ds} curves for MOSFETs in saturation, as demonstrated in figure 2.12.

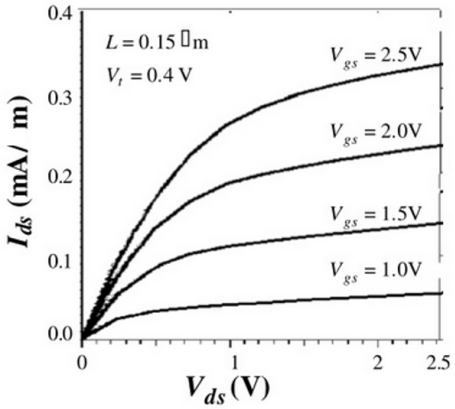

Figure 2.12: Output characteristic of a short device.

(Karen B. Melancon (2025) "Advancements in MOSFET Technology: Velocity Saturation and Short Channel Effect." *https://www.sciencedirect.com/topics/engineering/channel-length-modulation*)

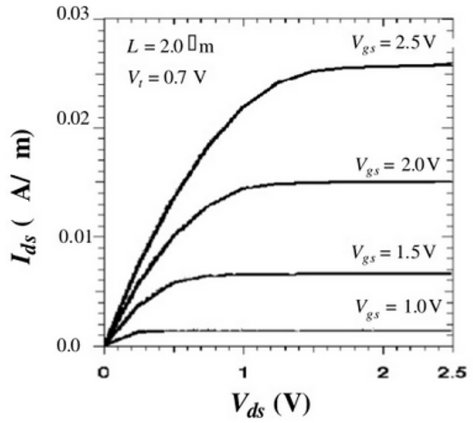

Figure 2.13: Output characteristic of a long device.

(Karen B. Melancon (2025) "Advancements in MOSFET Technology: Velocity Saturation and Short Channel Effect." *https://www.sciencedirect.com/topics/engineering/channel- length-modulation*)

As illustrated in figure 2.13, the behaviour of a long-channel device differs significantly from that of a nanometric device, as long-channel devices demonstrate minimal sensitivity to modulation of the channel length. This phenomenon is exemplified in figure 2.13, where the device's behaviour approaches an ideal state.

This modulation of the channel length also has other consequences. It is evident that one of the factors contributing to this phenomenon is the reduction in the output resistance of the MOSFET, r_o, which is now subject to the Equation 2.36 [10]. This has been demonstrated to have a detrimental effect on the gain of the device in specific configurations.

$$r_o = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} = \frac{1}{\lambda I_D} \tag{2.36}$$

It can thus be concluded that channel length modulation is an effect that must be considered when modeling a device in saturation, particularly in the case of a nanometric MOSFET.

2.4 EKV Model

The EKV model (Enz-Krummenacher-Vittoz) is a compact model representing a MOSFET transistor. The model was developed during the 1990s at the Electronics Laboratory of the École Polytechnique Fédérale de Lausanne by Christian Enz, François Krummenacher and Eric A. Vittoz. The development of this model was driven by the objective of producing a compact, physical model of a MOSFET transistor that would be compatible with other analogue integrated circuits [11]. The necessity to devise this model arose from the recognition that conventional models were insufficient to simulate reduced voltage and current conditions. The primary factor contributing to the success of the EKV model was its capacity to represent the MOSFET in a continuous manner across the various inversion regions, namely weak, moderate, and strong, thereby facilitating the derivation of expressions that rendered the design and simulation of integrated circuits more straightforward.

Since the inception of this model, the EKV has undergone significant evolution over time, through its numerous iterations. EKV 2.6, developed by the EPFL (École Polytechnique Fédérale de Lausanne) team in 1997, is widely regarded as one of the most significant versions. This version represented a breakthrough in the design of high-precision analogue circuits, introducing a single equation to the model that maintained the continuity of the first and second derivatives with respect to the terminal voltage.

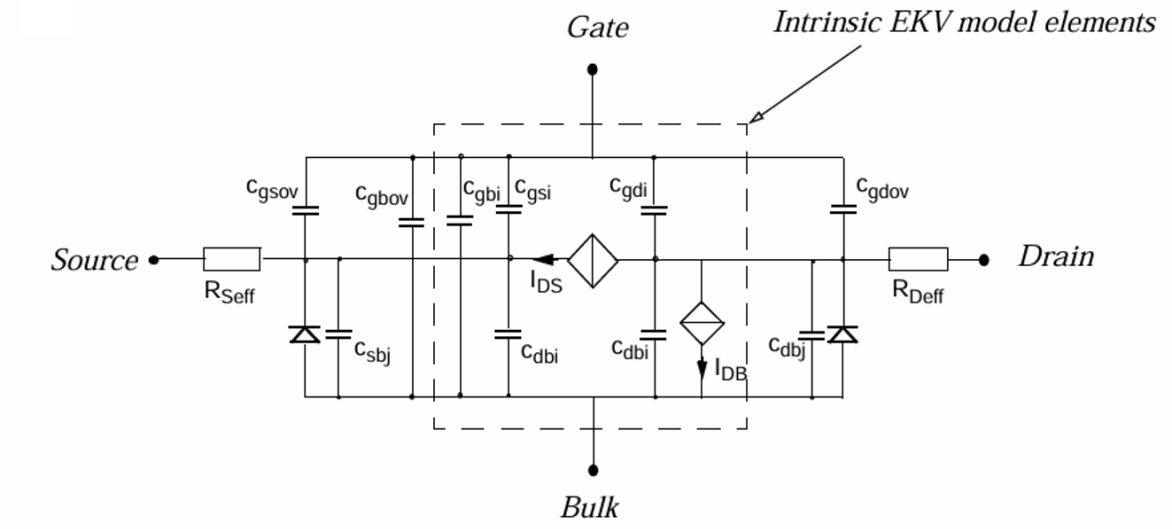

Figure 2.14: Intrinsic and extrinsic elements of the MOS transistor for the EKV Model.

(Matthias Bucher, Christophe Lallement, Christian Enz, Fabien Théodoloz, François Krummenacher. (1997) "The EPFL-EKV MOSFET Model Equations for Simulation." *Electronics Laboratories, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland.*)

Furthermore, this version incorporates second-order effects into the model, including channel length modulation, load-sharing effect, saturation velocity, impact ionization effect, thermal noise and flicker noise. This version is modeled on the circuit shown in the figure 2.14. It is evident that the model takes into account the intrinsic and extrinsic capabilities of the transistor. Furthermore, he pioneered the development of a non-quasi-static (NQS) model for alternating current simulation.

Subsequent to this, the EKV 3 model was developed by the Technical University of Crete (TUC). This new version incorporates numerous parameters that accurately represent the physical phenomena to which the transistor is typically subjected, thereby providing a more precise description of advanced CMOS technologies, including quantum effects, the effects of shallow trench isolation (STI) stress, and the effects of internal and external capacitances. This model offers a variety of simulation modes, rendering it suitable for a broad spectrum of applications.

As previously outlined, this model employs a compact physical representation of the MOSFET channel, utilizing the normalized forward and reverse currents to unify the drain current. The fundamental expression employed is the ratio of the transconductance to the current. This enables the expressions for the device loads, capacitances and noise to be obtained coherently by means of derivation. By following this approach, these expressions can subsequently be incorporated into simulators such as Ngspice.

This model is notable for its capacity for geometric scaling, a quality that renders it an excellent instrument for the purpose of representing nanometric transistors. Furthermore, it exhibits an excellent response to extreme temperature variations.

Chapter 3

SETUP WORK APPLICATIONS

3.1 OpenVAF

In the context of this project, the utilization of diverse tools was contemplated for the purpose of compiling the code to be generated in Verilog-A. Ultimately, the decision was made to employ an open-source tool. This decision was made on the premise that the work completed would be able to continue in the future and would be of public use, thereby allowing any individual to utilize the model or propose enhancements without restrictions through the open-source framework. Following extensive consultation, it was determined that the model should be straightforward to utilize. Consequently, the primary focus of the subsequent model development should be on the code itself rather than on the management of the open-source components.

Consequently, it was determined that the tool to be utilized in this thesis is the open-source OpenVAF. This is a simulation tool that facilitates the compilation of disparate programming languages. In this particular instance, the software will be employed to compile the model in Verilog-A, thereby facilitating the generation of files that are compatible with a range of simulators. For the purposes of this work, the file to be obtained has been assigned the OSDI extension, a file type that is frequently utilized for the representation of electronic circuits through simulations.

The open-source software known as OpenVAF was initially developed for use on the Linux operating system. However, in this particular instance, it is to be used directly on a Windows computer. In order to achieve this objective, it is necessary to utilize the Windows Subsystem for Linux (WSL), which facilitates the execution of open-source software on a Linux distribution that operates directly on the Windows operating system.

Once the WSL environment has been established, the subsequent step is to proceed with the installation of OpenVAF. This process is meticulously delineated in the official website's instructions, which are characterized by their clarity and comprehensiveness.

In this project, OpenVAF will be configured as an auxiliary tool that will act as a local compiler. This will allow the file conversion process to be automated, thus facilitating the work. This is due to the fact that, during the modeling of the device, the code will be

continuously evolving, meaning that it will be necessary to make the compilation process as efficient as possible.

3.2 Ngspice

Conversely, upon the successful implementation of the model in OSDI extension, the subsequent phase involves conducting simulations, for which Ngspice will be utilized. Ngspice is a general-purpose circuit simulator that has been employed in both research and teaching contexts.

In the context of this thesis, the tool will be used as the primary simulator to run the netlist that is necessary to obtain the values and behaviour of the model defined in Verilog-A. Consequently, sophisticated simulations can be conducted on the modeled apparatus.

In order to successfully install Ngspice, it is essential to adhere to the instructions provided on the official website, where a selection of different versions is available. In this instance, the most recent version, Ngspice-44.2, was selected, in addition to a version with a console environment that facilitates the execution of simulations of files with SP extension.

In the context of utilizing this tool, two distinct options are available for execution: the first option involves the execution of simulations from the Ngspice console environment, while the second option entails the execution of said simulations from within the Windows Subsystem for Linux. In this instance, the second option will be utilized, thereby enabling the execution of the Verilog-A code and the conducting of simulations within a unified environment.

It is evident that Ngspice will process the netlist, apply the initial conditions and obtain the corresponding results or warnings. A further benefit of utilizing this instrument is its capacity to save the values obtained during the simulation in a text file. This functionality enables the subsequent processing of the data in other tools, such as MATLAB, thereby facilitating comprehensive analysis and interpretation.

Indeed, the generation of graphs in this thesis will be accomplished through the utilization of MATLAB, a programming language that facilitates the management of data in a straightforward manner and boasts a more extensive array of graphical capabilities when compared with the Ngspice alternative.

```
C:\Users\albag>cd C:\OpenVAF\corriente\ekv_model5

C:\OpenVAF\corriente\ekv_model5>openvaf ekv_model5.va
Finished building ekv_model5.va in 0.10s

C:\OpenVAF\corriente\ekv_model5>ngspice netlist_model5.sp
```

Figure 3.1: Example of compilation and simulation of the model, in the terminal WSL.

Having already prepared the two tools to be used, OpenVAF and Ngspice, figure 3.1 provides an example of how to work in the WSL environment. Firstly, the appropriate terminal must be entered, using the "cd" command. Subsequently, the code should be compiled with the VA extension, with particular attention paid to ensuring that it is error-free and generates the OSDI extension file. In conclusion, the simulation is conducted using Ngspice through a netlist with SP extension. This netlist will utilize the OSDI file to employ our custom device in the simulation.

Chapter 4

BUILD THE MODEL

After the previous documentation about the technology that is treat in this thesis, the Verilog-A programming language, the ngSpice net list and the setup of the open source that is use in this work, is the moment of create a model of an analog device. In this case, the first device will be a simple version of a nMOS.

4.1 nMOS Model with Verilog-A

As mentioned above, we will start with a very simple and reduced version of an nMOS. This way we can be more sure that everything is going as expected and check more precisely how the parameters we introduce affect the simulation of the analogue device.

Therefore, the first OpenVAF implementation of this nMOS will be done without taking into account the effect of external capacitances, noise, temperature perturbations and some adverse effects that the channel may suffer during the operation of this device. In addition, as previously mentioned, a very simple ekv model will be used, where a constant saturation state is assumed for the device. This will further simplify the code because it will only need to reflect the operation of the device in a saturation state, bypassing the channel inversion state and the linear operating region of the CMOS device.

In this first approximation, the input function will be performed by the nMOS voltages (Vgb, Vdb, Vsb). These voltages will be those of the device terminals referred to the bulk, therefore, we are talking about the voltage between the drain and the bulk, the source and the bulk and finally, the nMOS gate and the bulk. On the other hand, the output we are trying to obtain is the current of the drain, that is to say, the current that goes from the drain terminal to the source terminal, and therefore the code will be made to obtain the value of this current. In this code we will also have a series of parameters that will help us to reach the ideal result, although later on some of these will be treated as variables dependent on external elements such as temperature. In the image below you can see the code obtained by following the above mentioned requirements.

A number of parameters and equations used for the characterization of analogue devices have been used for this program.

Parameter name	Value	Description	Units
TNOM	25.0	Nominal Temperature	C
SCALE	1.0	Scale	-
L	$0.5 \cdot 10^{-6}$	Channel length	m
W	$0.5 \cdot 10^{-6}$	Channel width	m
VTO	0.5	Long-channel threshold voltage	V
N	1.0	Slope factor	-
N0	1.0	Long Channel Slope Factor Fine Tuning	-
k	$1.3807 \cdot 10^{-23}$	Boltzmann constant	J/q
q	$1.602 \cdot 10^{-19}$	Electron charge	C
LAMBDA_C0	0.05	Minimal length modulation coefficient	-
LSAT	$20.0 \cdot 10^{-9}$	Channel saturation length	m
UO	$4.1667 \cdot 10^{-2}$	Low field mobility in the channel region	$\frac{m^2}{v \cdot s}$
COX	$10.0 \cdot 10^{-3}$	Gate oxide capacitance per unit area	F
EOX	$3.45 \cdot 10^{-11}$	Oxide permeability	$\frac{F}{m}$
DL	0.0	Difference between effective and drawn gate length	m
XL	0.0	Optical offset for Gate Length	m
XW	0.0	Optical offset for Gate Width	m

Table 4.1: Parameters of the first nMOS model

As mentioned above, the parameters in the 4.1 and the following equations are used in this program, these have been obtained from various sources [11] [12] [9] [13], including studies working with the EKV model used here .

4.1.1 Pinch-off Voltage for a nMOS

For the model under consideration we have started with the most basic equations for CMOS devices. First of all, the pinch-off voltage is obtained Equation 4.1 [9].

$$V_p = \frac{V_{gb} - V_{to}}{n} \tag{4.1}$$

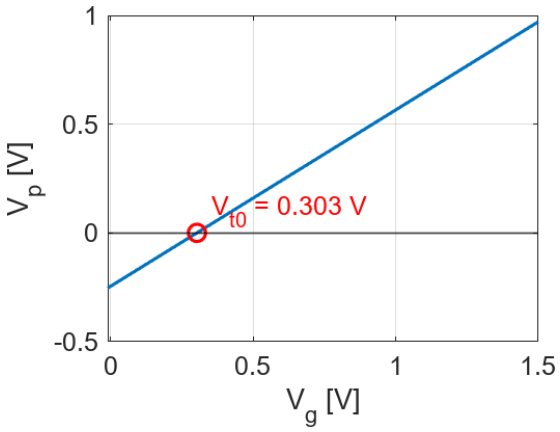

Figure 4.1: Pinch-off Voltage versus Gate Voltage of a nMOS.

Utilizing this expression within our model yields a pinch-off voltage that functions as illustrated in the figure 4.1 with respect to the voltage between the gate and the bulk. The graph illustrates that for a pinch-off voltage of zero, the gate voltage and the threshold voltage are congruent.

4.1.2 Thermodynamic Voltage for a nMOS

Once the pinch-off voltage is know the normalized source inversion charge can be obtained [9]. But first is also needed the thermodynamic voltage which is obtained from Equation 4.2 [9].

$$U_t \triangleq \frac{k \cdot T}{q} \tag{4.2}$$

4.1.3 Normalized Source Inversion Charge for a nMOS

To be able to obtain the normalized source inversion charge from Equation 4.3 a function is needed, that is why the LambertW function, Equation 4.4 [3], is used.

$$\frac{V_p - V_{sb}}{U_t} = 2q_s + \ln(q_s) \tag{4.3}$$

$$q_s = \frac{1}{2} \cdot \text{LambertW}\left(2e^{V_p - V_{sb}}\right) \tag{4.4}$$

The mentioned function can get the normalized source inversion charge using the voltage of the source refereed to the bulk and the pinch-off voltage. But one thing with the values to be passed to the function and how it is implemented in reality, a number of parameters and the following equations are needed.

$$\text{NUV} = N0 + 3 \cdot NCS \cdot t_{ox} \cdot CHSH_L \tag{4.5}$$

$$q(v) = \begin{cases} z_1 = \frac{1}{4} \cdot \left(\frac{v}{NUV} - 1.4 + \sqrt{\frac{v}{NUV} \cdot \left(\frac{v}{NUV} - 0.384936 \right) + 9.662671} \right) \\ z_2 = \frac{\frac{v}{NUV} - (2 \cdot z_1 + \ln z_1)}{2 \cdot z_1 + 1} \\ z_1 \left(1 + z_2 \cdot (1 + 0.07 \cdot z_2)\right) \cdot NUV & \text{if } \frac{v}{NUV} < -0.6 \\ z_{1,ln} = 0.5 \cdot \left(\frac{v}{NUV} - 0.201491 - \sqrt{\frac{v}{NUV} \cdot \left(\frac{v}{NUV} - 0.402982 \right) + 2.446562} \right) \\ z_1 = \frac{1}{4} \cdot \left(\frac{v}{NUV} - 1.4 + \sqrt{\frac{v}{NUV} \cdot \left(\frac{v}{NUV} - 0.384936 \right) + 9.662671} \right) \\ z_2 = \frac{\frac{v}{NUV} - \left(2 \cdot \exp(z_{1,ln}) + z_{1,ln}\right)}{2 \cdot z_1 + 1} \\ z_1 \left(1 + z_2 \cdot (1 + 0.483 \cdot z_2)\right) \cdot NUV & \text{if } \frac{v}{NUV} \geq -0.6 \end{cases} \tag{4.6}$$

The mentioned LambertW function has two cases that depend on the parameter *NUV* Equation 4.5 [12], but this parameter is going to be more simple than that because in the case that has been working here the disturbances of the noise are not taking into account. So in this initial model *NUV* is going to depend only on the long channel slope factor fine tuning.

$$\text{NUV} = N0 \tag{4.7}$$

The cases of the LambertW function also depend on the variable v that in this case will be Equation 4.8.

$$v = \frac{V_p - V_{sb}}{U_t} \tag{4.8}$$

After calculating v and *NUV* the normalized source inversion charge can be obtained by Equation 4.6 [12].

4.1.4 Inversion Coefficient for a nMOS

Consequently, now that we have the normalized source inversion charge, the pinch-off voltage and the thermodynamic voltage we can go on to calculate other variables that are necessary before applying the Equation 4.9 [9] that allows us to obtain the inversion coefficient. From which we can later derive the drain current.

$$IC = \frac{4\left(q_s^2 + q_s\right)}{2 + \lambda_c + \sqrt{4\left(1 + \lambda_c\right) + \lambda_c^2\left(1 + 2q_s\right)^2}} \tag{4.9}$$

4.1.5 Drain Current for a nMOS

To arrive at the Equation 4.12 for the drain current, it is also necessary to obtain the specific square current, Equation 4.10 [9], and the specific current, Equation 4.11 [9], which is obtained once the previous one is known.

$$I_{\text{spec}\square} \triangleq 2 \cdot n \cdot \mu_0 \cdot COX \cdot U_t^2 \tag{4.10}$$

$$I_{\text{spec}} \triangleq I_{\text{spec}\square} \cdot \frac{W}{L} \tag{4.11}$$

Having obtained all the above expressions, a simple multiplication is all that is needed to know the value of the drain current of the device we are dealing with Equation 4.12 [9].

$$IC \triangleq \left|\frac{I_D}{I_{\text{spec}}}\right| \text{ saturation} \tag{4.12}$$

With Equation 4.12 [9] is only needed to clear the I_D, because as it said before in this paper a permanent saturation situation is assumed for the CMOS devices.

4.2 Temperature Variation of nMOS Analog Device Parameters

After building the most basic model of an nMOS in Verilog-A and performing various tests to check that it works correctly, that the variables behave as expected and that the parameters are correctly adjusted for the objective required in this case, we move on to the next step in the construction of the model.

The model will progressively become more complex in order to be able to simulate all the cases that we want to take into consideration and create different analogue circuits. After this first nMOS model, the next addition will be to convert some of its parameters into temperature-dependent variables.

This will be done with certain precautions; we will try to keep the model as simplified as possible, so we will look for equations that do not depend on many different parameters or that have linear relationships with temperature. In this way, the type of model we are looking for is kept as small and practical as possible, but taking into account all the necessary scenarios.

For this new model of an nMOS, four different variables will be added to the previous temperature dependence. These will be the slope factor, the threshold voltage, the N0, and low field mobility in the channel region.

Parameter name	Value	Description	Units
TEMP		Device Temperature	K
KP	$500.0 \cdot 10^{-6}$	Mobility multiplied with COX	$\frac{A}{V^2}$
VT0	0.5	Threshold voltage with Nominal Temperature	V
TCV	$1.0 \cdot 10^{-3}$	Threshold voltage temperature coefficient	$\frac{V}{K}$
BEX	-1.5	Exponential temperature dependence of KP	-
NEX	0.12	Exponential temperature dependence of the slope factor	-

Table 4.2: Parameters for temperature dependence of the nMOS model

To achieve this, it is necessary to add a number of parameters to the initial model, so that the behavior of the variables with temperature variation is faithfully reflected.

4.2.1 Threshold Voltage Temperature Dependence

Once all the necessary parameters are available at Table 4.2, the temperature-dependent variables can be defined. We start with the threshold voltage Equation 4.13 [11], for which we need the threshold voltage temperature coefficient and the threshold voltage at nominal temperature.

$$VTO(T) = VTO - TCV \cdot (T - T_{\text{nom}}) \tag{4.13}$$

4.2.2 Slope Factor Temperature Dependence

Another variable with which a temperature dependence can be established is the slope factor, that is defined in Equation 4.14. This dependence would be proportional to the NEX parameter whose value is obtained in the article [14] , in a graph that shows the variation of the slope factor with the effect of temperature following Equation 4.15.

$$N(T) = N(T_{\text{nom}}) \cdot \left(\frac{T}{T_{\text{nom}}}\right)^{NEX} \tag{4.14}$$

$$\left(\frac{400}{300}\right)^{NEX} = \frac{1.18}{1.14} \tag{4.15}$$

The parameter N0 is also going to be modified to be temperature dependent following the Equation 4.17 by using the parameter NEX0. The function of this parameter will be to help establish this dependence. In the case we are dealing with, NEX0 will be set to the same value as NEX, Equation 4.16, for this simplified model, since it is not necessary for the moment to add more components that affect the behavior of the nMOS.

$$NEX0 = NEX \tag{4.16}$$

$$N0(T) = N0(T_{\text{nom}}) \cdot \left(\frac{T}{T_{\text{nom}}}\right)^{NEX0} \tag{4.17}$$

The decision to modify the parameter N0 and make it temperature-dependent is taken so that the model can adapt to more situations when testing its performance. In particular, making N0 a variable will help the model to work in cryogenic temperature conditions.

4.2.3 Mobility of the Channel Region Temperature Dependence

The last parameter to be set also with a temperature dependence will be the Low field mobility in the channel region. For this we also have to modify the KP (Mobility multiplied with COX) to be temperature dependent as in Equation 4.18 [11], which will follow a similar relationship with temperature as the slope factor but with its own parameter, BEX. This parameter is obtained from the [11].

$$KP(T) = KP(T_{\text{nom}}) \cdot \left(\frac{T}{T_{\text{nom}}}\right)^{BEX} \tag{4.18}$$

$$\mu_0 = \frac{KP(T)}{COX} \tag{4.19}$$

With these modifications, the initial model would have been adapted to add the desired temperature variation and therefore the next step can be taken, which would be to add certain capacitance between the nodes of the CMOS device to achieve a more realistic behavior of the CMOS device.

4.3 Length Variation of nMOS Analog Device Parameters

In order to more accurately and correctly characterize the analogue device being described in the Verilog-A language, it is necessary to scale the channel length. By doing this, it is possible to establish a dependence between this length and certain variables, such as the slope factor or the threshold voltage of the NMOS channel.

Apart from the scaling itself, a relationship between the λ_c variable and the channel length will also be established [15]. Therefore, a list of parameters is necessary to perform both of them. The parameters that are not related with the value of λ_c are taken from [11] and [12].

Parameter name	Value	Description	Units
LAMBDA_C0	0.08	Minimal velocity saturation parameter at long channel	-
LSAT	$19.9 \cdot 10^{-9}$	Channel saturation length	m
DL	0.0	Difference between effective and drawn gate length	m
DW	0.0	Difference between effective and drawn gate width	m
XL	0.0	Optical offset for Gate Length	m
XW	0.0	Optical offset for Gate Width	m

Table 4.3: Parameters for length dependence of the nMOS model

For the scaling of the parameters depending of the length of the channel various parameters are needed, Table 4.4, this parameters have been obtained through the experimentation for the conditions that appeared with a temperature of $300K$, as shown in the article [16].

Parameter name	Value	Description
VT0_A	0.117	Parameter for threshold voltage scaling
VT0_B	-0.19	Parameter for threshold voltage scaling
VT0_C	0.069	Parameter for threshold voltage scaling
N_A	0.38	Parameter for slope factor scaling
N_B	-2.81	Parameter for slope factor scaling
N_C	1.225	Parameter for slope factor scaling
I0_A	$-0.51 \cdot 10^{-7}$	Parameter for specific current per square scaling
I0_B	-1.03	Parameter for specific current per square scaling
I0_C	$-12.7 \cdot 10^{-7}$	Parameter for specific current per square scaling
L_VT0	$25.0 \cdot 10^{-6}$	Length for threshold voltage with nominal temperature
L_N0	$7.0 \cdot 10^{-8}$	Length for slope factor with nominal temperature
L_I0	$1.3 \cdot 10^{-6}$	Length for specific current per square with nominal temperature

Table 4.4: Parameters for length scaling of the nMOS model

Therefore, with the parameters already established in Table 4.3, the dependence of λ_c on channel length can be characterized by Equation 4.20 [15].

$$\lambda_C = \frac{\text{LSAT}}{L} + \lambda_{\text{C0}} \tag{4.20}$$

To give more structure to the model we will also establish the following relationships, Equation 4.22 and Equation 4.21 [12], so that it is more moldable depending on the situation in which the nMOS finds itself.

$$L_{\text{scaled}} = L \cdot \text{SCALE} + XL \tag{4.21}$$

$$W_{\text{scaled}} = W \cdot \text{SCALE} + XW \tag{4.22}$$

In addition to the aforementioned considerations, the effective length and width of the channel will be incorporated. The following measurements are the authentic metrics of the channel that facilitate the conduction of current subsequent to the manufacturing process. This

variation in theoretical length and width is typically attributable to the masking process, which engenders a slight modification in these measurements. The expressions employed to ascertain the effective length and width of the channel are Equation 4.23 and Equation 4.24, respectively.

$$L_{eff} = L + DL \tag{4.23}$$

$$W_{eff} = W + DW \tag{4.24}$$

On the other hand, as mentioned above, some variables will be scaled depending on the temperature, using the parameters of the Table 4.4 obtained in a situation where the ambient temperature was $300K$ as it's mentioned in [16]. This process will scale the channel threshold voltage, the slope factor and the specific current per square, following the Equation 4.25, Equation 4.26 and Equation 4.27 respectively.

$$V_{TO_L} = V_{TO_a} \left(\frac{L}{L_{VTO_0}} \right)^{V_{TO_b}} + V_{TO_c} \tag{4.25}$$

$$n_L = n_a \left(\frac{L}{L_{n_0}} \right)^{n_b} + n_c \tag{4.26}$$

$$I_{0_L} = I_{0_a} \left(\frac{L}{L_{I_0}} \right)^{I_{0_b}} + I_{0_c} \tag{4.27}$$

Once we have these variables correctly scaled with respect to the length of the channel, we will have all the variables dependent on it that will be necessary.

After doing all this, it could be said that the construction of the most basic model of the nMOS device is concluded. With the code obtained, certain checks have been carried out to verify its correct operation.

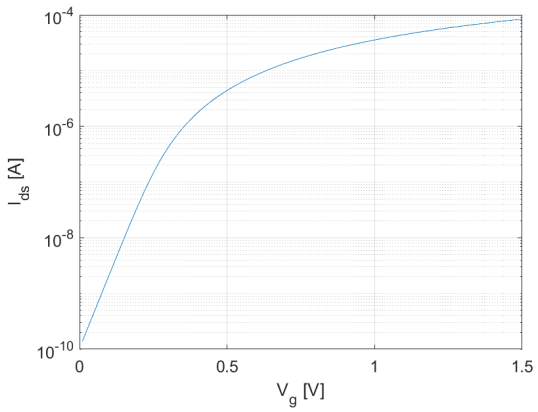

Figure 4.2: The drain to source current versus the gate voltage. $L = 1.0\mu m$ and $W = 0.5\mu m$

An example is shown in the figure 4.2, where you can see the characteristic behaviour of the drain current versus gate voltage of a nMOS. In addition, a comparison was also made with the numerical values that could be expected when using the selected equations and it was seen that they did indeed coincide with those obtained through the simulation.

4.4 Capacitance of the nMOS Device

As already mentioned, capacitances are also a relevant part that must be taken into account in the model if we want its behavior to be more similar to reality, as it said in [17] "Additionally, extrinsic gate-source, gate-bulk, and gate-drain overlap capacitances and the drain diffusion capacitance reduce operating bandwidth from the intrinsic value, especially for short-channel devices where intrinsic gate capacitances are small". Therefore, in this nMOS model we are going to introduce two capacitances, one between the gate and the source (C_{gs}) and the other between the gate and the drain (C_{gd}). Once the expressions of the aforementioned capacitances have been obtained, their effects will be included in the model by modifying the current that flows through the branches where these capacitances are located [18].

In order to proceed to include these capacitances in the analogue device, certain parameters must first be included in the model, table 4.5 [12], which will be necessary for their characterization.

Parameter name	Value	Description	Units
LOV	$10.0 \cdot 10^{-9}$	Length of the overlap area	m

Table 4.5: Parameter for capacitance of the nMOS model

The parameter indicated in the table 4.5 is the overlap length of the MOSFET, LOV, defined as the portion of the gate that is situated above the area of both the drain and the source. In other words, the area of the gate that lies beyond the extension of the channel itself, as illustrated in the accompanying image 4.3. The presence of this overlapping area gives rise to the manifestation of parasitic capacitors, both between the gate and the source and between the gate and the drain. It has been demonstrated that, at the inception of channel modulation, there exists an area of overlap between the gate and the carriers. This overlap is a contributing factor to the process.

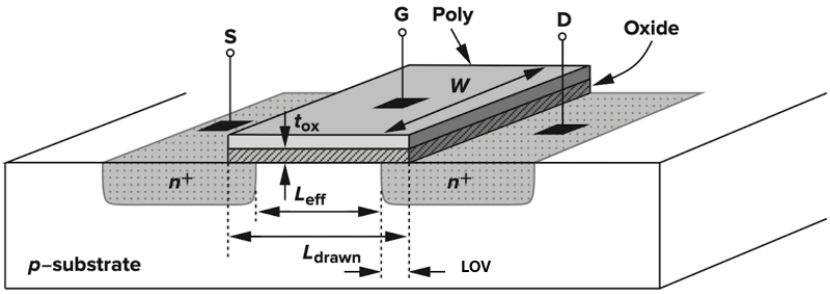

Figure 4.3: Graphical scheme of the MOSFET with the overlap length appreciation.
(Browny. (2/14/2022) "[MOSFET 01] Basic MOS device". *https://browny.tistory.com/20*)

Once we have the parameters we need, the expression for the capacitance between the gate and the drain is very simple, Equation 4.28 [3], and only depends on the width of the channel, gate oxide capacitance per unit area and length of the overlap area.

$$C_{gd} = COX \cdot W \cdot LOV \tag{4.28}$$

On the other hand, the expression for the capacitance between the gate and the source is Equation 4.29 [3]. Witch is somewhat more complex and depends on the channel length and the normalized source inversion charge Equation 4.4, in addition to the above parameters.

$$C_{gs} = COX \cdot W \cdot [\, L \cdot \frac{q_s}{3} \cdot \frac{2q_s + 3}{(q_s + 1)^2} + LOV] \tag{4.29}$$

Once the respective values of the capacitances have been found, this value is applied to the current flowing through the branches where they are located, so that the model suffers the effects of these [18]. Therefore, the value of the capacitance is multiplied by the voltage difference at both ends of the capacitance , Equation 4.30 and Equation 4.31. With this we obtain the charge of each branch.

$$Q_{gd} = C_{gd} \cdot V_{gd} \tag{4.30}$$

$$Q_{gs} = C_{gs} \cdot V_{gs} \tag{4.31}$$

Then all that would be needed would be to derive this electric charge with respect to time as in Equation 4.32 Equation 4.33, and we would obtain the current through the capacitances.

$$I_{gd} = \frac{dQ_{gd}}{dt} \tag{4.32}$$

$$I_{gs} = \frac{dQ_{gs}}{dt} \tag{4.33}$$

This would model the effect of capacitances on the basic analogue device being built, so that it can be implemented in circuits considering this behavior.

4.5 Extension of the nMOS Model

Once you have the most basic model of an nMOS represented in the Verilog-A language and you have done the necessary checks on how it works, you can make the model somewhat more complex. But all this is done keeping in mind that we want to obtain a representation of the nMOS that is easy to manipulate.

To this end, the effect of the transconductances, the velocity saturation voltage and the noise effects between others will be added to the device at this point. As well as, the necessary modifications of the code in order to obtain the operating point of the nMOS.

4.5.1 Node Charges

The term inversion charges is used to denote the electrical inversion charge that accumulates at the extremities of the channel. The inversion charge is located at a point close to the source, and is denoted as q_s. The inversion charge located near the drain is denoted as q_d.

It is evident that these charges are directly related to the carrier density generated by the voltage between the gate and the source in the channel region. Within the linear operating region of the MOSFET, both q_s and q_d exhibit comparable values due to the effective channel length extending across the entirety of the space between the source and the drain. Consequently, the channel carriers exert a uniform effect on both. However, when this analogue device enters saturation, the channel is cut off in the vicinity of the drain, which causes the inverting load of the drain to decrease drastically compared to the inverting load near the source, because the carrier concentration near the drain decreases. Consequently, the drain load is reduced, while the source inversion load is increased due to the strong inversion it has to bear.

It is evident that, in the limit of saturation $q_d << q_s$. Given the assumption of a continuous saturation state within the model, it can be concluded that q_d can be disregarded in relation to q_s in the subsequent expressions.

4.5.1.1 Normalized Intrinsic Node Charges

The subsequent step in the model will involve the modeling of the normalized charges at the internal MOSFET nodes q_S and q_D. It is posited that these variables represent the moving charge density at the source and drain ends, respectively.

It is evident that a multitude of applications can be realized through the utilization of these components. The drain current can be delineated as a function of them, as well as the capacitance between terminals. This can be ascertained by deriving these charges with respect to the voltages applied at the extremities of the capacitances. Alternatively, they can be employed to endeavor to maintain continuity between the disparate regions of operation.

The expressions that must be obtained in order to calculate the intrinsic normalized charge of the source and of the drain are, respectively, Equation 4.34 [12] and Equation 4.35 [12].

$$\mathrm{qS} = \frac{n}{3} \cdot \left(2 \cdot q_s + q_d + \frac{\left(1 + \frac{4}{5} \cdot q_s + \frac{6}{5} \cdot q_d\right) \cdot (q_s - q_d)^2}{2 \cdot (q_s + q_d + 1)^2} \right) \tag{4.34}$$

$$\mathrm{qD} = \frac{n}{3} \cdot \left(q_s + 2 \cdot q_d + \frac{\left(1 + \frac{6}{5} \cdot q_s + \frac{4}{5} \cdot q_d\right) \cdot (q_s - q_d)^2}{2 \cdot (q_s + q_d + 1)^2} \right) \tag{4.35}$$

As previously stated, the model is developed under the assumption that the device is in saturation. Consequently, the inverting load of the drain can be disregarded in comparison to that of the source. This results in the derivation of a new expression for the normalized intrinsic load of the source, Equation 4.36, and another for the normalized intrinsic load of the drain, Equation 4.37.

$$\mathrm{qS} = \frac{n}{3} \cdot \left(2 \cdot q_s + \frac{\left(1 + \frac{4}{5} \cdot q_s\right) \cdot (q_s)^2}{2 \cdot (q_s + 1)^2} \right) \tag{4.36}$$

$$\mathrm{qD} = \frac{n}{3} \cdot \left(q_s + \frac{\left(1 + \frac{6}{5} \cdot q_s\right) \cdot (q_s)^2}{2 \cdot (q_s + 1)^2} \right) \tag{4.37}$$

4.5.1.2 Total Charges

In addition to the intrinsic charges of the nodes in the model, the total source and drain charges will be defined. These are no longer one-dimensional; they are Coulomb charges that describe the total amount of charge stored or displaced at each terminal of the MOSFET. This value is contingent on the physical parameters of the device and the region of operation in which the device is situated.

It is evident, therefore, that the generic equation required to calculate the total charge of one of the terminals is Equation 4.39 [11]. The value in question is contingent upon the total oxide capacitance and the thermodynamic voltage of the device, Equation 4.38 [11].

$$C_{ox} = COX \cdot W_{\mathrm{eff}} \cdot L_{\mathrm{eff}} \tag{4.38}$$

$$Q_{(I,B,D,S,G)} = C_{ox} \cdot U_t \cdot q_{(I,B,D,S,G)} \tag{4.39}$$

The expressions for the total charge of the source and the total charge of the drain will be Equation 4.40 and Equation 4.41, respectively.

$$Q_S = C_{ox} \cdot U_t \cdot q_S \tag{4.40}$$

$$Q_D = C_{ox} \cdot U_t \cdot q_D \tag{4.41}$$

4.5.2 Transconductances of a nMOS Device

To continue with the construction of the model, we are going to express the partial derivatives of the drain current with respect to the slight variations that occur in the voltage at the device terminals, known as the transconductances.

4.5.2.1 Source Transconductance

One of the transconductances we are going to model is the normalized source transconductance. To do this, we will follow the following equation obtained from the [9], which uses the parameter λ_c and the inversion coefficient, both of which have already been used previously.

One of the transconductances we are going to model is the normalized source transconductance. For this, in the [9] we find we find the Equation 4.42 that depends on the parameter λ_c and the inversion coefficient, both already used before, so we use this one to modulate the desired effect in our model.

$$g_{\text{ms}} \triangleq \frac{\sqrt{(\lambda_c IC + 1)^2 + 4IC - 1}}{\lambda_c(\lambda_c IC + 1) + 2} \tag{4.42}$$

With this transconductance, it is possible to measure the effect that the voltage between the source and the substrate has on the drain current. This effect is known as the *body effect*, and is based on the modification of the properties of the channel by having a non-zero voltage between these two terminals of the nMOS. The increase in the emptying area of the channel is due to the fact that the channel is now under the effects of the V_{sb} voltage in addition to the gate voltage.

$$G_{\text{ms}} = \frac{g_{ms} \cdot I_{spec}}{U_t} \tag{4.43}$$

Apart from this, we can also obtain the source transconductance following Equation 4.43. And ones we have it be can modulate the source transconductance efficiency $\frac{G_{ms}}{I_D}$. This is obtained by simply dividing the source transconductance by the current from the drain to the source.

Finally, we will find the value of the normalized source transconductance efficiency as a function of the voltage between the source and the substrate V_{sb}, normalize in terms of the thermal voltage. This is also known as the body-bias efficiency, because it is directly related to the body-effect explained above. This efficiency is defined as $\frac{G_{ms} \cdot U_t}{I_D}$.

4.5.2.2 Output Conductance

The normalized output conductance will also be added to the model, this is defined in a similar way to the normalized source transconductance, Equation 4.45, this one will use both known and unknown parameters. The σ_d parameter and the λ_d parameter, which for the time being will take the same value as λ_c, must also be used, Equation 4.44.

Parameter name	Value	Description	Units
LAMBDA_D	λ_C		-
SIGMA_D	0.6	Body effect DIBL Coefficient	-

Table 4.6: Parameters for output conductance of the nMOS model

$$\lambda_d = \lambda_c \tag{4.44}$$

$$g_{\text{ds}} \triangleq \frac{\sigma_d}{n} \cdot \frac{\sqrt{(\lambda_d IC + 1)^2 + 4IC - 1}}{\lambda_d(\lambda_d IC + 1) + 2} \tag{4.45}$$

This conductance reflects channel-length modulation, which occurs when the voltage between the drain and the source increases beyond the saturation point and therefore, the active length of the channel starts to decrease. Therefore, the normalized output conductance reflects the effect on the drain current of variations in the voltage V_{ds}.

$$G_{\mathrm{ds}} = \frac{g_{ds} \cdot I_{spec}}{U_t} \tag{4.46}$$

In addition to this, we will also get the output transconductance by following the Equation 4.46. And again the output transconductance efficiency is obtained by dividing the transconductance by the drain current, $\frac{G_{ds}}{I_D}$.

We will also characterize $\frac{G_{ds} \cdot U_t}{I_D}$, which analogously to the one explained above is the logarithmic slope of the drain current but this time as a function of the output voltage, the voltage between the drain terminals and the source.

4.5.2.3 Gate Transconductance

Finally, we will also model the transconductance of the gate, which is defined in the Equation 4.47. But it can also be obtained through the following Equation 4.48 [9], where it depends on the conductance between the source and the gate and the slope factor.

Therefore, from the Equation 4.48 , if the terms are substituted, the Equation 4.49 will be arrived at. This expression is the one we will use in this model.

$$g_m \triangleq \frac{\partial I_{DS}}{\partial V_{GS}} \tag{4.47}$$

$$\frac{G_{ms}}{G_{spec}} = \frac{n \cdot G_m}{G_{spec}} \tag{4.48}$$

$$G_m = n \cdot G_{ms} \tag{4.49}$$

Knowing that, we can conclude that the normalized gate transconductance can be also defined by the normalized source transconductance and the slope factor, following the Equation 4.50 that is deducted from Equation 4.49.

$$g_m = n \cdot g_{ms} \tag{4.50}$$

By modeling, this transconductance we are able to define how the drain current is affected by variations in the voltage between the gate and the source.

We will also model the gate transconductance efficiency $\frac{G_m}{I_D}$. In addition, we will also calculate the normalized gate transconductance efficiency, which can be known as $\frac{G_m \cdot U_t}{I_D}$. Both of them are extracted dividing the source transconductance efficiency and the normalized source transconductance efficiency, receptively, by the slope factor.

4.5.3 Velocity Saturation Voltage of a nMOS Device

In the program we will also model the velocity saturation voltage, this will be done in order to obtain the value of the voltage between the drain and the source from which the velocity of the carriers in the channel is limited. This limitation in the velocity of the carriers arises when the V_{ds} exceeds the critical level known as E_c, which is characterized by the following Equation 4.51 where its value depends on the saturation velocity and the mobility of the carriers, in the case of the nMOS electrons.

$$E_c = \frac{v_{sat}}{\mu_o} \tag{4.51}$$

$$V_{DSsat} = 2 \cdot U_t \cdot [(\sqrt{IC + \frac{1}{4}} + \frac{1}{2}) + 1] \tag{4.52}$$

Therefore, following the Equation 4.52 obtained from the paper [11], when the voltage between the drain and the source reaches the velocity saturation voltage the carriers stop accelerating, staying at their saturated velocity and therefore the current grows more slowly limiting the gain and degrading the gate transconductance.

4.5.4 Noise Effects

It is imperative that this model incorporates noise as a fundamental element. Noise is defined as a device that manifests the inherent random fluctuations that affect charge carriers, i.e. electrons in the case of nMOS, and also acts on some internal physical phenomena of the device. It can thus be concluded that noise has the capacity to impact the performance of analogue circuits, particularly in the context of low-signal applications. Furthermore, noise has been shown to generate a problem of precision in the device, thereby causing variability

between circuits. This, in turn, gives rise to a significant design problem if one seeks to create a larger circuit by employing different MOSFETs.

The primary noises that impact these devices are thermal noise, shot noise, flicker noise, and finally, short channel-induced noise.

The initial topic of discussion is thermal noise, which is attributable to the random movement of free electrons within the channel region of the MOSFET, even in de-energized states.

Conversely, shot noise manifests in devices wherein carrier emission occurs through a barrier. However, in a MOSFET, this noise is not predominant, and its effects are mitigated. This phenomenon can be attributed to the fact that carrier emission does not traverse the terminal potential barrier; rather, it is known to flow through the device channel. However, it has been observed that this phenomenon may manifest in leakage currents.

Another characteristic noise is flicker noise, which is dominant at low frequencies and is attributed to the charge exchanges that occur between the oxide-semiconductor interface and the MOSFET channel itself.

In conclusion, the noise induced by the short channel, as indicated by its name, is present in sub-micrometric technologies. This noise has been observed to cause effects ranging from channel heating to modulation of the channel length. However, this phenomenon is represented by the saturation velocity, which has been demonstrated to be capable of modifying thermal and flicker noise levels.

Parameter name	**Value**	**Description**	**Units**
KF	$1.0 \cdot 10^{-25}$	Flicker noise coefficient	-
AF	1.0	Flicker noise exponent	-

Table 4.7: Parameters for flicker noise effects of the nMOS model

In this model, however, the focus will be on the effects of two noises: thermal noise and flicker noise. In order to ascertain their values, it is first necessary to establish the parameters that are listed in Table 4.7.

4.5.4.1 Thermal Noise

In this program, thermal noise will be modeled as a case study. Thermal noise, otherwise referred to as Johnson-Nyquist noise, constitutes one of the primary noises that must be considered when the characterization of a MOSFET is to be undertaken with precision.

This noise, as previously explained, originates from the random movement of the carriers in the channel, electrons in the case of nMOS or holes in the case of pMOS, during conduction in the channel. This undesirable movement is attributable to thermal agitation, that is to say, the thermal energy possessed by the particles as a consequence of the temperatures attained by the device.

It is acknowledged that thermal noise is of the white noise variety, a category defined by the constancy of its spectral density with respect to frequency. Moreover, this phenomenon of noise is not contingent upon the physical characteristics of the device, such as its length. Rather, it is determined by conduction. The equation that describes the behaviour of power spectral density of the thermal noise in the drain current, Equation 4.53 [3].

$$S_{\Delta I_D^{(\text{thermal})}}(f) = 4 \cdot k \cdot T \cdot \gamma_{noise} \cdot G_{ms} \tag{4.53}$$

$$\gamma_{noise} = \frac{2}{3} \cdot \frac{q_s + \frac{3}{4}}{q_s + 1} \tag{4.54}$$

In the Equation 4.53, the γ is a bias-dependent parameter, that follows Equation 4.54 [5]. The remaining terms are already established and their definitions have been previously elucidated.

$$S_{\Delta V_G^{(\text{thermal})}}(f) = \frac{S_{\Delta I_D^{(\text{thermal})}}(f)}{G_m^2} \tag{4.55}$$

In addition to the power spectral density of the thermal noise in the drain current, the power spectral density of the thermal noise in the gate voltage can also be obtained by employing the Equation 4.55 [3].

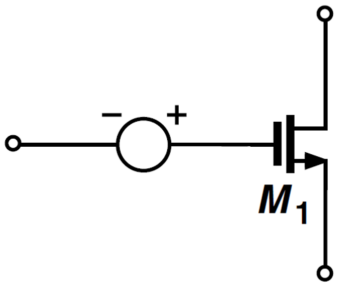

Figure 4.4: Noise disturbing as a voltage source.

(Bruno Talanto (2020) "Noise-Figure of Common-Source (CS) and Common-Gate (CG) Field-Effect Transistors (FETs)." *University of California, San Diego.*)

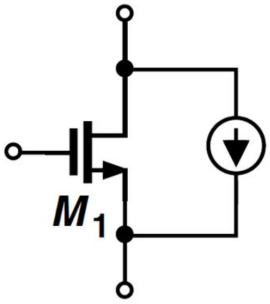

Figure 4.5: Noise disturbing as a current source.

(Bruno Talanto (2020) "Noise-Figure of Common-Source (CS) and Common-Gate (CG) Field-Effect Transistors (FETs)." *University of California, San Diego.*)

The distinction between the two expressions is determined by the manner in which the noise influence the device. This phenomenon is clearly evident in the images 4.4 and 4.5. As illustrated in figure 4.4, the MOSFET is shown to be disturbed by a voltage source, which serves to illustrate the effect of the noise. Figure 4.5 similarly illustrates the noise by means of a current source, in an analogous manner.

4.5.4.2 Flicker Noise

It is imperative that another of the noises that must be modeled for the correct representation of an nMOS or pMOS through the code is flicker noise. This phenomenon is also referred to as low-frequency noise or flicker noise, and as the name suggests, it is a noise that is very characteristic of electronic devices that operate at low frequencies.

Flicker noise is characterized by a spectral density that decreases with frequency, resulting in increased intensity at low frequencies. The disturbance originates from charge traps situated between the gate oxide and the conduction channel. These traps randomly trap and release channel carriers, thereby altering the channel current.

$$S_{\Delta I_D^{(\text{flicker})}}(f) = \frac{G_m^2 \cdot K_F}{COX \cdot W \cdot L} \cdot \frac{1}{f^{AF}} \tag{4.56}$$

Equation 4.56 is employed to express the behaviour of the power spectral density of the flicker noise in the drain current. In this expression, K_F represents the flicker noise coefficient and AF the flicker noise exponent. As demonstrated in Equation 4.56, it is evident that the magnitude of the noise effect is directly proportional to the increase in the channel width and length of the device.

$$S_{\Delta V_G^{(\text{flicker})}}(f) = \frac{K_F}{COX \cdot W \cdot L} \cdot \frac{1}{f^{AF}} \tag{4.57}$$

$$S_{\Delta V_G^{(\text{flicker})}}(f) = \frac{S_{\Delta I_D^{(\text{flicker})}}(f)}{G_m^2} \tag{4.58}$$

The following Equation 4.57 is analogous to the previous one, but it describes the flicker noise as a voltage at the gate of the MOSFET. In addition to its own expression, the power spectral density of the flicker noise in the gate voltage can also be obtained through the power spectral density of the flicker noise in the drain current. This can be achieved by the given Equation 4.58.

4.5.5 Operating Point of a nMOS Device

Finally, in this phase of the model we will modify the code in order to obtain the operating point with all the necessary variables. This operating point will be used to fix the terminal voltages and the currents between them under static conditions.

With this analysis done, the different operating regions can be determined, which in our case will always be saturation since the model is designed for a CMOS device in those conditions. It also allows us to know some parameters such as the capacitances of the device, its nominal transconductances or the efficiency of the transconductances, things that will be useful later on when we want to do an AC analysis or an analysis of noise and other disturbances. The operating point will also be very useful when doing an analysis in time, since this point can be used to start the analysis, thus avoiding jumps at the beginning of the simulation.

To prepare the code for the calculation of the operating point, it is enough to create a function called OPP, whose structure is predefined in the program for this task [18]. In order to calculate the subsequent operating point, it is necessary to consider the model to be acting as an nMOS. In accordance with this assumption, it is possible to use all of the default parameters for this purpose, Table 4.1, Table 4.2, Table 4.3, Table 4.4, Table 4.5, Table 4.6

and Table 4.7. Furthermore, the operating temperature is set at $37C$, which is simulated using a device with $L = 0.5 \cdot 10^{-6}m$ and $W = 0.5 \cdot 10^{-6}m$. The gate voltage is set at $0.7V$ for the DC component and $1.0V$ for the AC component. The voltage between the drain and the source is maintained at $12.0V$ for the DC component and $1.0V$ for the AC component.

Once this is done, all the parameters that we want to calculate the operating point, voltages, currents, capacitances, etc., are included in this function. In the following table 4.8 you can see the variables obtained from the operation point with its corresponding value.

Variable name	**Value for IC = 0.01**	**Value for IC = 1.01**	**Value for IC = 30.0**	**Units**
id_op	$8.29929 \cdot 10^{-9}$	$8.38228 \cdot 10^{-7}$	$2.48979 \cdot 10^{-5}$	A
qs_op	5.20094	5.20094	5.20094	-
Cgs_op	$1.56061 \cdot 10^{-15}$	$1.56061 \cdot 10^{-15}$	$1.56061 \cdot 10^{-15}$	F
Cgd_op	$5.0 \cdot 10^{-17}$	$5.0 \cdot 10^{-17}$	$5.0 \cdot 10^{-17}$	F
cgs_op	0.624242	0.624242	0.624242	-
cgd_op	0.02	0.02	0.02	-
Gm_op	$2.4932 \cdot 10^{-7}$	$1.53629 \cdot 10^{-5}$	$1.07468 \cdot 10^{-4}$	A/V
Gms_op	$3.07246 \cdot 10^{-7}$	$1.89323 \cdot 10^{-5}$	$1.32437 \cdot 10^{-4}$	A/V
Gds_op	$1.49592 \cdot 10^{-7}$	$9.21775 \cdot 10^{-6}$	$6.4481 \cdot 10^{-5}$	A/V
gm_op	$8.03016 \cdot 10^{-3}$	0.494813	3.46137	-
gms_op	$9.89586 \cdot 10^{-3}$	0.609776	4.26557	-
gds_op	$4.8181 \cdot 10^{-3}$	0.296888	2.07682	-
Gm_Id_op	30.0411	18.3278	4.31637	1/V
Gms_Id_op	37.0207	22.5861	5.31922	1/V
Gds_Id_op	18.0247	10.9967	2.58982	1/V
GmUt_Id_op	0.803016	0.489914	0.115379	-
GmsUt_Id_op	0.989586	0.603739	0.142186	-
GdsUt_Id_op	0.48181	0.293948	0.0692274	-
I_flicker_noise_op	$6.26223 \cdot 10^{-19}$	$3.78222 \cdot 10^{-17}$	$2.30424 \cdot 10^{-16}$	A^2/Hz
V_flicker_noise_op	$1.00743 \cdot 10^{-5}$	$1.6025 \cdot 10^{-7}$	$1.99511 \cdot 10^{-8}$	V^2/Hz
I_thermal_noise_op	$3.36708 \cdot 10^{-27}$	$2.07478 \cdot 10^{-25}$	$1.451367 \cdot 10^{-24}$	A^2/Hz
V_thermal_noise_op	$5.416763 \cdot 10^{-14}$	$8.79073 \cdot 10^{-16}$	$1.25666 \cdot 10^{-16}$	V^2/Hz

Table 4.8: Values of the operating point

Once the operating points have been obtained for different values of the inversion coefficient, values that represent the three inversion regions of the MOSFET device, it is evident that the values taken by the most characteristic variables, such as the capacitances or the transconductances, agree with the expected outcomes. In any event, a series of simulations will be conducted in order to verify that the device's behaviour is in accordance with the expected parameters.

We simulate the inversion coefficient versus the overdrive voltage, and as shown in the figure 4.6 the behaviour is as expected. With this we can check that the drain current is correct since

the override voltage had already been verified previously. This graph also coincides with the results obtained in the paper [9], so we can see that the ekv model behaves as desired.

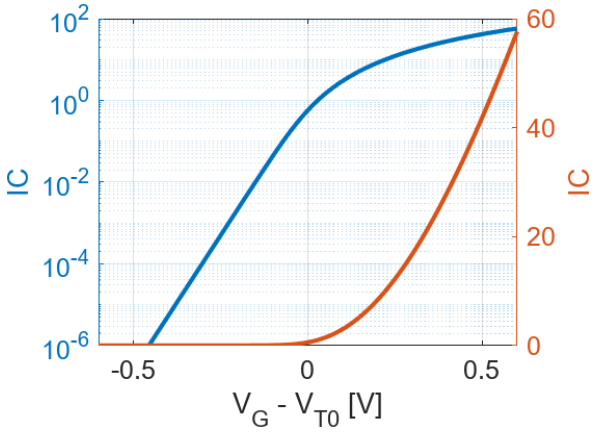

Figure 4.6: The inversion coefficient versus the overdrive voltage. $L = 0.5\mu m$ and $W = 0.5\mu m$.

Apart from verifying the inversion coefficient, we are also interested in checking the transconductance, because for the operating point we obtain somewhat high values, as shown in the table 4.8. To do this, we will look for the values of the normalized source transconductance and the normalized output transconductance as the inversion coefficient changes.

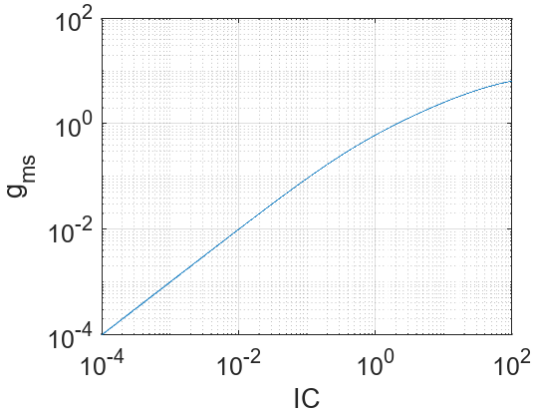

Figure 4.7: Normalized source transconductance versus the inversion coefficient.

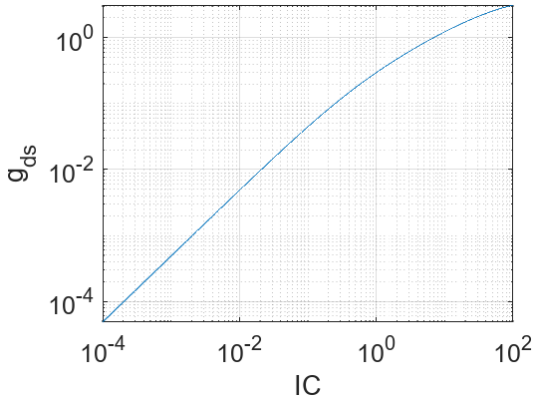

Figure 4.8: Normalized output conductance versus the inversion coefficient.

In the following figures 4.7 and 4.8, we verify the behaviour of these transconductances, in these apart from seeing that the values grow with IC as expected we verify that they behave in a similar way to the EKV model in the paper [9].

4.6 pMOS Model with Verilog-A

Once the Verilog-A model for an nMOS has been constructed, taking into account all manufacturing and performance considerations, such as scaling with respect to temperature or channel length, the model can be adapted to function for both an nMOS and a pMOS.

This objective is realized through the configuration of the model. The most significant aspect of this adaptation will be the sign inversion of the MOSFET voltages. It is imperative to note that this inversion will be executed at the commencement of the code, thereby exerting its influence on the expressions that have been established within the code. In order to achieve this objective, it is necessary to create a variable which is to be designated 'TYPE'. The value of this variable will be one if the MOS is n-type and minus one if the MOS is p-type. This will ensure that the potential found at the terminals of the MOSFET is matched in both cases. This variable will be utilized at the outset and in order to accurately display the output currents and capacitances, given that these are inverted in the pMOS with respect to the nMOS.

In addition to the aforementioned procedure, it is also necessary to take into account the adjustment of the parameters, depending on whether the device under consideration is an nMOS or a pMOS. It is evident that novel parameters will need to be established in order to facilitate both the scaling with respect to temperature and the scaling with respect to channel length. The values for these parameters can be found in the table 4.9 provided.

Parameter name	**N-type Value**	**P-type Value**
LAMBDA_C0	0.08	0.15
LSAT	$19.9 \cdot 10^{-9}$	$19.2 \cdot 10^{-9}$
VT0_A	0.117	0.06
VT0_B	-0.19	-0.405
VT0_C	0.069	0.339
N_A	0.38	1.985
N_B	-2.81	-2.9
N_C	1.225	1.2382
I0_A	$-0.51 \cdot 10^{-7}$	$-0.31 \cdot 10^{-7}$
I0_B	-1.03	-1.8525
I0_C	$-12.7 \cdot 10^{-7}$	$2.24 \cdot 10^{-7}$
L_VT0	$25.0 \cdot 10^{-6}$	$10.0 \cdot 10^{-6}$
L_N0	$7.0 \cdot 10^{-8}$	$4.15 \cdot 10^{-8}$
L_I0	$1.3 \cdot 10^{-6}$	$0.187 \cdot 10^{-6}$

Table 4.9: Parameters for length scaling of the model

The scaling with respect to channel length will be carried out using the same expressions for both types of MOSFET, with the difference being that different values will be used for this scaling. These parameters have been obtained experimentally at an operating temperature of 27°C [16]. As previously stated, the expressions are identical in the case of the pMOS, as outlined in section "Length Variation of nMOS Analog Device Parameters".

The expression employed for the modulation of the length modulation coefficient, λ_c, is analogous to that utilized in the context of N-type MOSFETs. It is noteworthy that the values that characterize the equations, λ_{c0} and $LSAT$, are subject to variation. These data have been obtained from the graph describing the behaviour of the length modulation coefficient with respect to the variation of the channel length for a pMOS [15]. It is evident that λ_{c0} will be the minimum value adopted by the length modulation coefficient. The appearance of this coefficient is contingent on an increase in channel length.

Should all these changes be implemented, it is anticipated that the pMOS will be modeled with perfect fidelity on the Verilog-A code that was in existence prior to the implementation of the aforementioned changes. In this manner, the model is merely adapted, without altering the fundamentals that have been adhered to throughout the entirety of the programming process. This process maintains a straightforward and lucid structure, yet it is concurrently prepared to accommodate an augmented computational load and incorporate additional specifications into the respective MOSFET.

Chapter 5

SIMULATION AND RESULTS

Following the successful creation of the model of the MOSFET device in Verilog-A, the subsequent stage is to verify its correct operation. In order to accomplish this objective, the following approach will be adopted: a simulation will be conducted to reproduce the most significant characteristics of any analogue device. These characteristics include voltages, currents and behaviour with respect to temperature. In addition to verifying the functionality of the model, the generation of graphs will be undertaken, the purpose of which is to illustrate the response of the MOSFET to varying voltages, currents, or inversion levels. It is imperative to acknowledge the nature of the MOSFET, whether it is an nMOS or a pMOS, and to recognize its nanometric measurements, its adherence to the ekv model, and its state of saturation.

5.1 Length Scaling

Initially, the model's responses to variations in channel length are obtained through simulations. The objective of this study is to simulate the response of the threshold voltage, the slope factor, the specific square drain and the length modulation coefficient. The graphs obtained were then subjected to rigorous scrutiny to ensure their compatibility with the anticipated outcomes, a process that entailed a comparative analysis with prior studies [16], in which experimental measurements were derived from simulated devices.

The initial step in this process will be to ascertain the results of the model's operation as an nMOS. Subsequently, the same graphs are obtained for the case of the P-type MOSFET device.

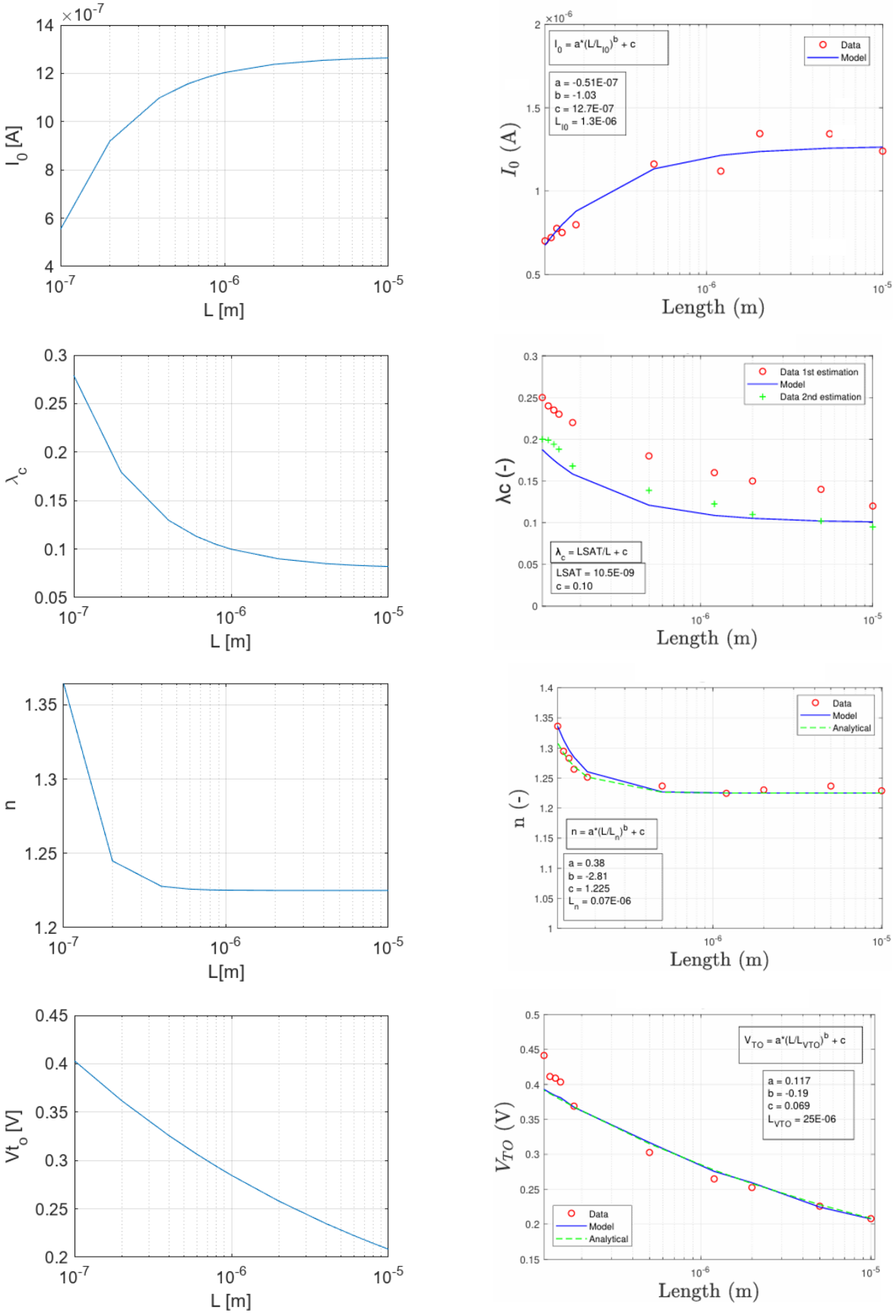

Figure 5.1: The parameters I_0, λ_c, n and V_{to} versus the length of the channel of the nMOS. The left column shows the result of the model operating at 37ºC and the right column shows experimental values of the nMOS [16].

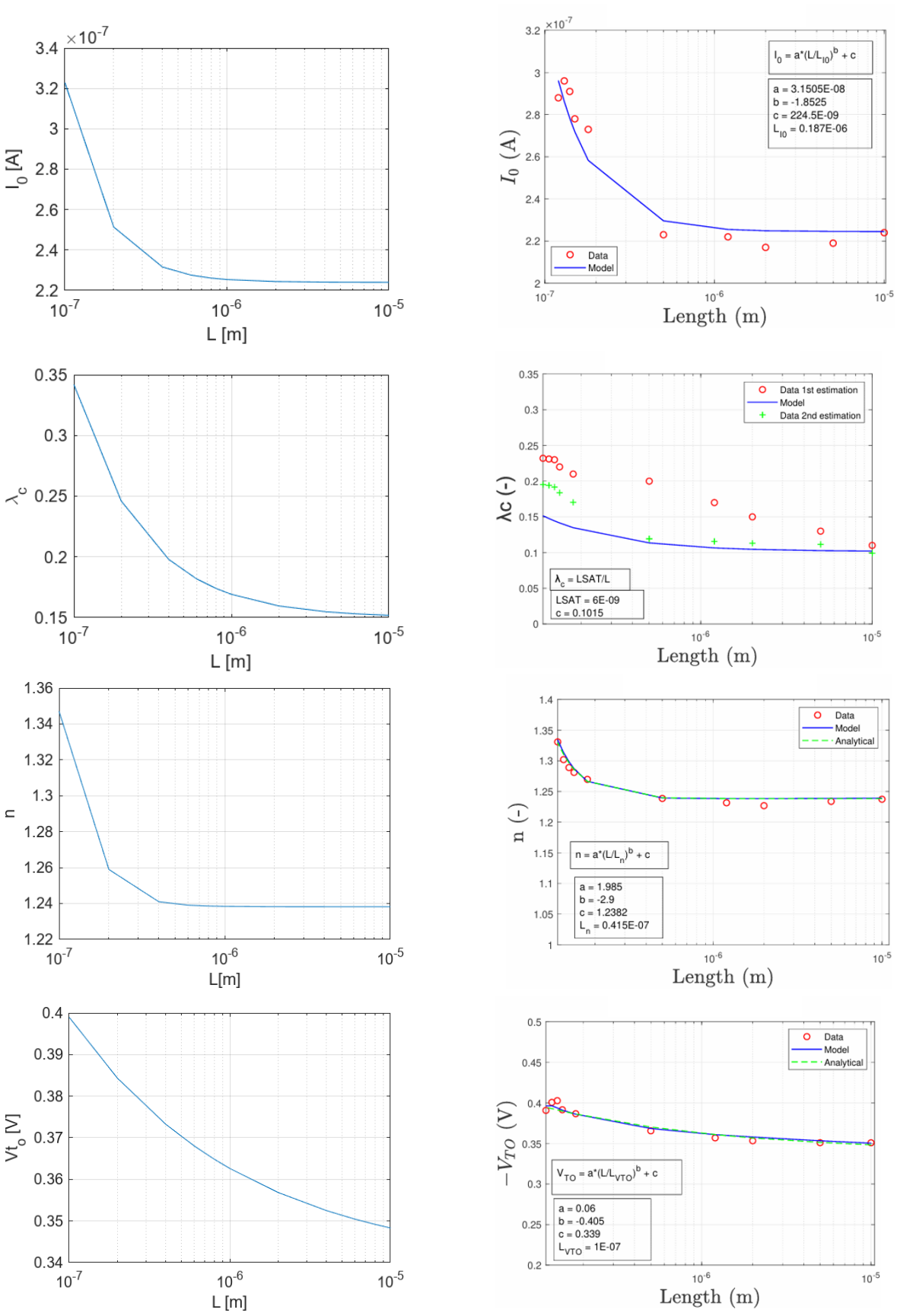

Figure 5.2: The parameters I_0, λ_c, n and V_{to} versus the length of the channel of the pMOS. The left column shows the result of the model operating at 37ºC and the right column shows experimental values of the pMOS [16].

As previously indicated, figure 5.1 illustrates the threshold voltage, slope factor, specific square drain and length modulation coefficient versus channel length for an N-type MOSFET. The initial column displays the data obtained using the model created, while the subsequent column presents the experimental data referenced in [16]. Conversely, figure 5.2 presents the same cases, but for a pMOS device.

As is evident, the values of our model are in excellent agreement with those obtained through experimentation. The sole value that exhibits a slight deviation is that of the λ_c. This discrepancy can be attributed to the utilization of different values for the scaling with respect to the length in these two cases. Specifically, the values employed in this particular instance, denoted by [15], differ from those used in the article, which are derived from the graphs located on the right.

Notwithstanding this fact, it is evident that the values are acting in accordance with the expected parameters. It is evident that the threshold voltage undergoes a decline in value as the channel length is increased. In nanometric devices, as in the present case, the DIBL effect is generally observed. This arises from the increased attraction of the electrostatic potential between the drain and the source when their proximity increases. Consequently, this effect decreases the potential barrier that prevents current from flowing through the channel when it is in the cut-off state. Consequently, analogous to this principle, increasing the distance between the drainer and the source serves to reduce the influence of the drainer on the area proximate to the source, thereby facilitating optimal behaviour and thus maintaining the threshold voltage value.

Conversely, the slope factor exhibits a decline in value as the channel lengthens. This phenomenon can be attributed to an augmentation in the deplexing capacity of the area beneath the channel, thereby affording the DIBL effect a heightened degree of control over the gate. It has been demonstrated that both pMOS and nMOS exhibit a comparable response to variations in channel length. However, it has been established that pMOS typically possess a higher slope factor due to their reduced doping levels, which consequently leads to diminished doping capacitance.

The specific current per square exhibits a distinct behaviour in relation to the channel length, contingent on whether the MOSFET is of the N-type or P-type. Ideally, this magnitude would not be affected by the geometrical parameters of the device; however, slight variations have been observed. In the case of nMOS, the current undergoes a negligible increase with an increase in channel length, while the opposite is true for pMOS.

In conclusion, it is evident that the behaviour of the length modulation coefficient is subject

to a decrease in proportion to an increase in channel length. This phenomenon can be attributed to the fact that as the length of the channel is reduced, the area that is subject to the influence of the gate is concomitantly diminished, resulting in the invasion of the drain region extending into a greater proportion of the channel. This results in an accelerated increase in drain current relative to the voltage between the drain and the source, thereby leading to an enhancement in the length modulation coefficient.

5.2 Temperature Scaling

Subsequent to the examination of the scaling outcomes in relation to temperature, the model's response to temperature fluctuations will be analyzed. In order to accomplish this objective, a simulation will be conducted to evaluate the values of the pinch-off voltage, carrier mobility, threshold voltage and slope factor across a broad temperature range extending from -45°C to 130°C.

The study will commence with the model acting as an N-type MOSFET, followed by simulations with the model operating as a pMOS.

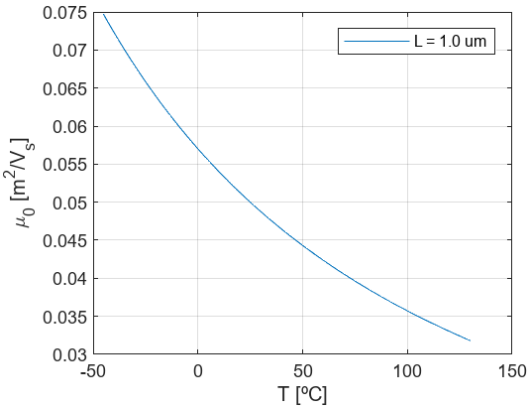

Figure 5.3: The low field mobility in the channel region versus the temperature of the nMOS.

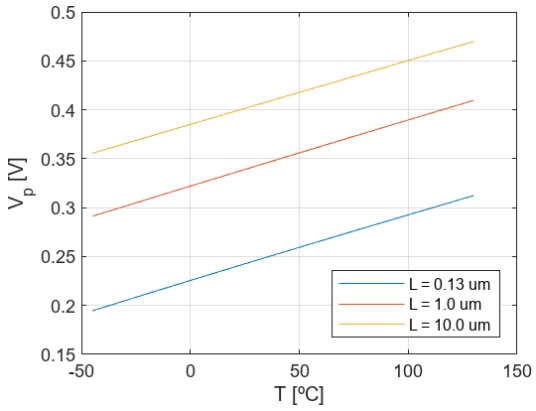

Figure 5.4: The pinch-off voltage versus the temperature of the nMOS.

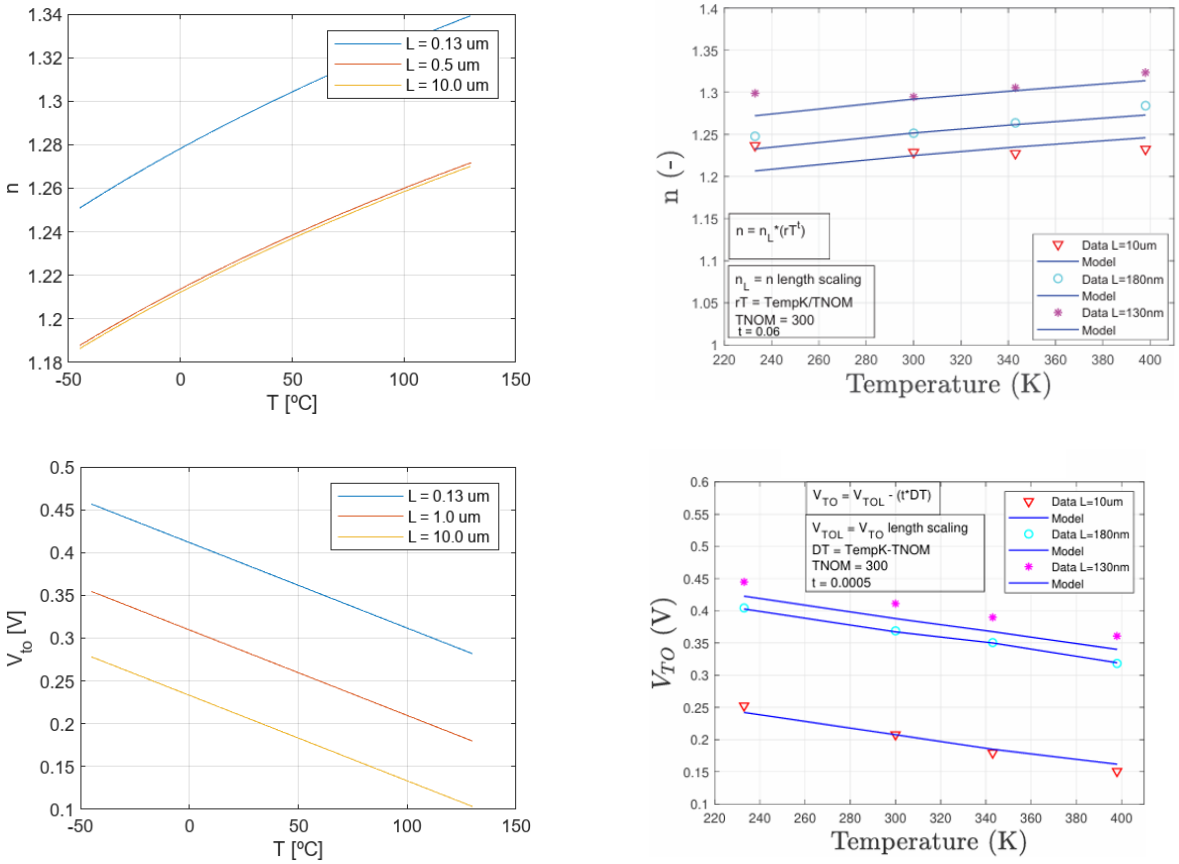

Figure 5.5: The parameters n and V_{to} versus the temperature of the nMOS. The left column shows the result of the model and the right column shows experimental values of the nMOS [16].

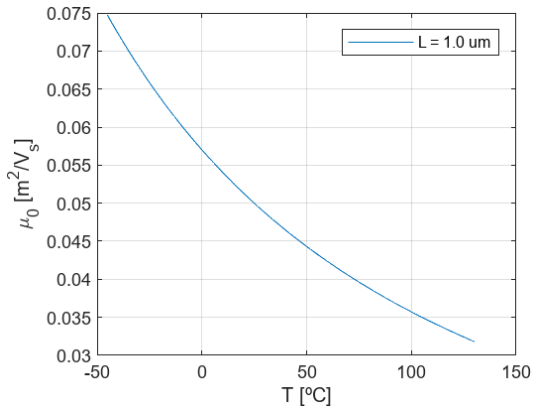

Figure 5.6: The low field mobility in the channel region versus the temperature of the pMOS.

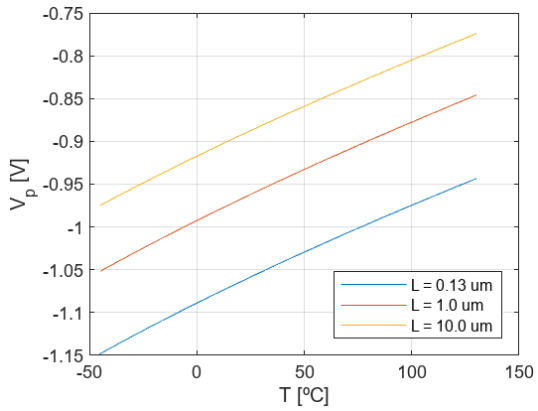

Figure 5.7: The pinch-off voltage versus the temperature of the pMOS.

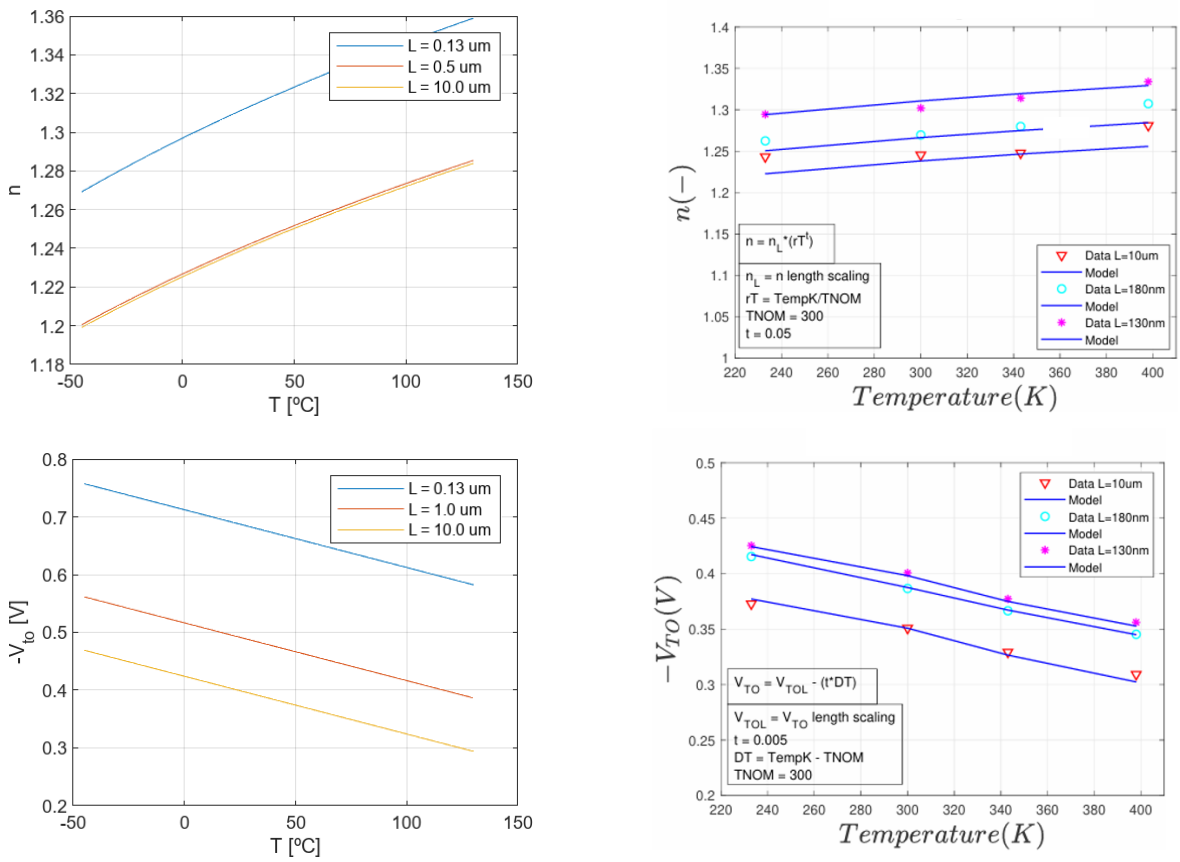

Figure 5.8: The parameters n and V_{to} versus the temperature of the pMOS. The left column shows the result of the model and the right column shows experimental values of the pMOS [16].

As with the scaling of the channel length, in this case there are also experimental values with which to compare the values obtained by the model. It is evident that, with these values of the threshold voltage and the slope factor, the functionality of the designed device is analogous to that of a real one, albeit with certain discrepancies. This is attributable to the fact that the parameters employed for the temperature scaling in the model differ from those utilized to derive the experimental values, as referenced in [16]. In this particular instance, the parameters employed in the Equation 4.13, the method by which the threshold voltage is determined are sourced from the document [11]. As demonstrated in the paper entitled [14], the parameters employed in Equation 4.14 and Equation 4.19 to calculate the slope factor and the low field mobility in the channel region, respectively, are derived from the aforementioned paper.

With regard to the mobility in the MOSFET channel, the results obtained are in agreement with the expectations that have been set, insofar as this magnitude decreases as the temperature

increases, as you can see in 5.3 and 5.6. This phenomenon can be attributed to the observation that as the temperature rises, the frequency of carrier collisions concomitantly increases, thereby diminishing the effective mobility of the channel. In practice, the decline in mobility is significantly more pronounced in the nMOS than in the pMOS. However, the design decision was taken not to incorporate specific parameters for the nMOS or the pMOS when scaling the temperature. Consequently, this magnitude is equivalent for both the nMOS and the pMOS.

It is also noteworthy that mobility, as evidenced by figures 5.3 and 5.6, is independent of channel length. This is analogous to the ideal case, and while in reality, due to secondary effects that affect the device, a discrepancy in mobility should be observed with respect to the length of the channel, in this model, such effects are not considered.

As the temperature rises, the pinch-off voltage concomitantly increases, as is show in 5.4 and 5.7. This is due to the fact that the difference between the voltage V_{gb} and the threshold voltage, if the former remains constant, is equal to the sum of the squares of the voltages.

Conversely, the slope factor exhibits an increase in proportion to the rise in device temperature, as seen in 5.5 and 5.8. This phenomenon can be attributed to the fact that the MOSFET requires greater gain in weak inversion as the temperature rises. This, in turn, is due to the expansion of the deplexing region, resulting in a less precipitous slope for the inversion current.

Finally, the investigation reveals a decline in the absolute value of the threshold voltage with an increase in temperature, exhibiting a slope of -0.5 mV/°C for high-doped devices and -0.2 mV/°C for low-doped devices. This observation indicates that, in an nMOS, the slope is more pronounced due to its higher carrier concentration compared to a P-type device. The decrease in threshold voltage can be attributed to the fact that as T increases, the intrinsic carrier density also increases, thereby reducing the Fermi potential. This, in turn, results in a reduction in the barrier separating the gate from the channel.

5.3 Gate Behaviour

In order to proceed with the verification of the model's behaviour, the subsequent stage of the research will entail the analysis of the MOSFET gate's response to varying currents, capacitances and transconductances.

In order to accomplish this objective, the initial step will be to simulate the behaviour of the gate voltage versus the drain current. The simulation will be conducted using devices of varying gate lengths and different operating temperatures, as well as simulating the model acting as an nMOS and as a pMOS.

The study will commence with the simulation of the current between the drain and the source as a function of the gate voltage. In order to accomplish this objective, it is necessary to procure the model in order to function as an nMOS, with the figures 5.9 and 5.10, and as a pMOS, with the figures 5.11 and 5.12. Furthermore, this procedure will be conducted for three distinct gate lengths, $0.13\mu m$, $1.0\mu m$ and $10.0\mu m$ in addition to three varying operating temperatures, namely -40°C, 37°C and 125°C.

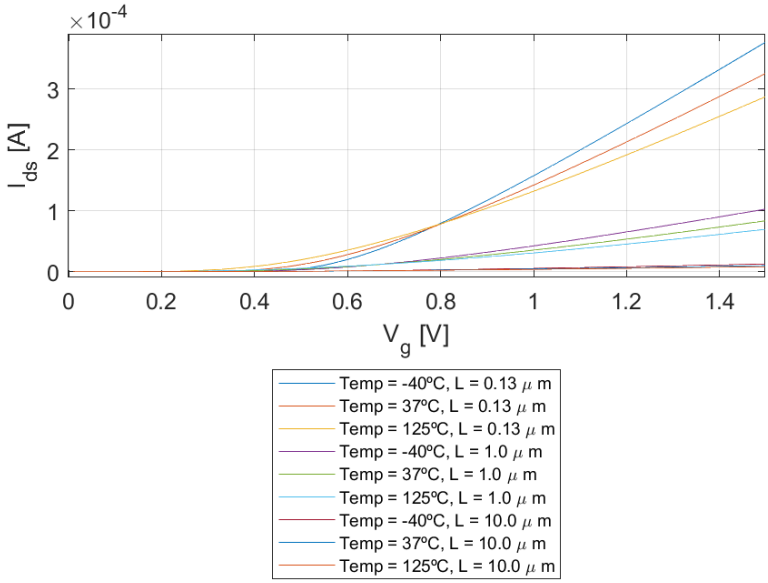

Figure 5.9: The drain current versus the gate voltage of the nMOS. I_{ds} is represented in linear scale.

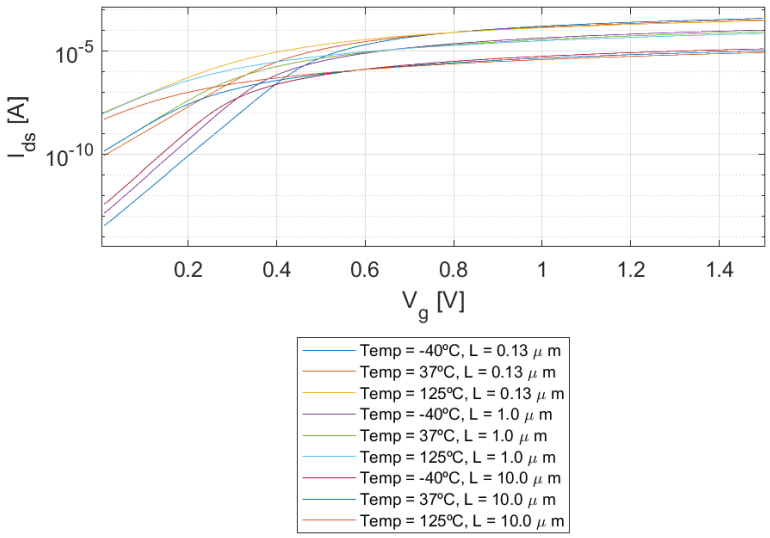

Figure 5.10: The drain current versus the gate voltage of the nMOS. I_{ds} is represented in logarithmic scale.

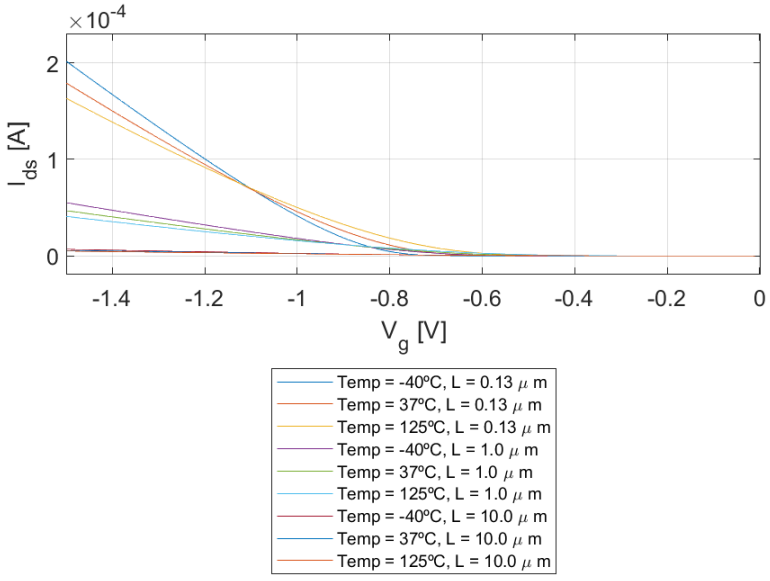

Figure 5.11: The drain current versus the gate voltage of the pMOS. I_{ds} is represented in linear scale.

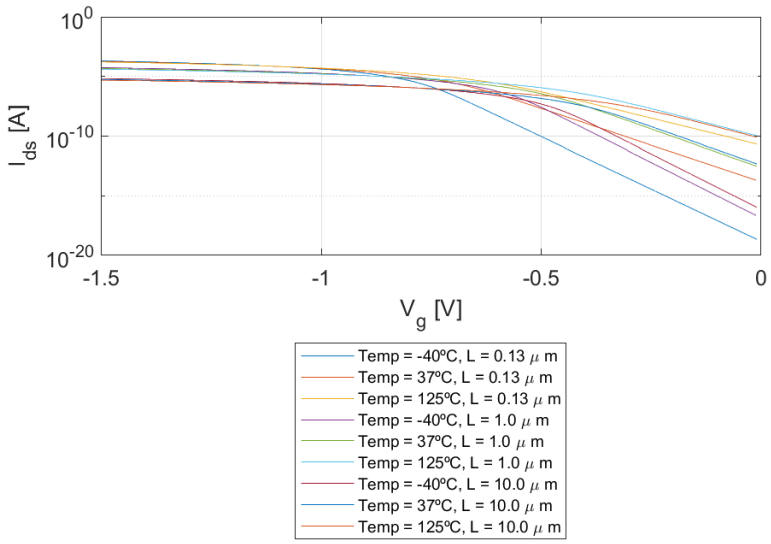

Figure 5.12: The drain current versus the gate voltage of the pMOS. I_{ds} is represented in logarithmic scale.

Following the execution of the simulations, a number of observations can be made. When the current of the drain is presented on a linear scale, the slope of the current is found to be contingent on the length of the channel as opposed to the temperature. This suggests that the shorter the channel length, the greater the slope of Ids when the transistor is in its active region. This observation lends further support to the notion that nanometric devices exhibit high current magnitudes, a phenomenon that is at least partly attributable to the adverse effects of the drain and source being in such close proximity to each other. As illustrated by the logarithmic scale graph, the peak of the drain current is determined by the geometry of the transistor.

Despite the fact that its effect is negligible in comparison to that of the channel length, once more it is evident that the current is elevated at lower temperatures. This phenomenon can be attributed to the impact of carrier mobility within the channel, which, as previously elucidated, diminishes with an increase in temperature.

With regard to the disparities that are evident between the graphs depicting N-type and P-type, it is discernible that the absolute current is elevated for the nMOS, attributable to the augmented mobility of the electrons. Furthermore, the slope exhibits a heightened incline for these transistors, a phenomenon attributable to the diminished slope factor characterizing these devices. Another salient aspect pertains to the leakage current, which is observed to be higher in pMOS devices.

The subsequent stage of the process is to simulate the inversion coefficient, once more with respect to the gate voltage. As previously outlined, the present simulation will be conducted for three distinct cases of temperature and three cases of channel length. The model will be configured to operate as both an nMOS and a pMOS.

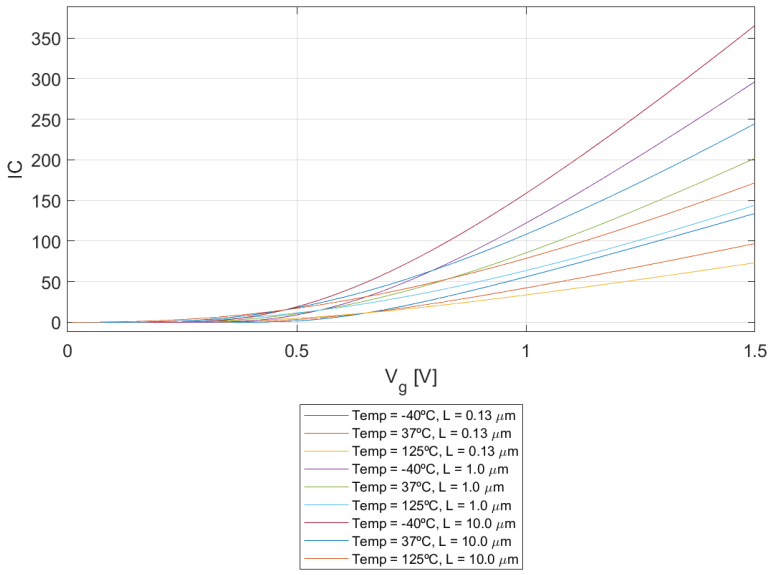

Figure 5.13: The inversion coefficient versus the gate voltage of the nMOS. *IC* is represented in linear scale.

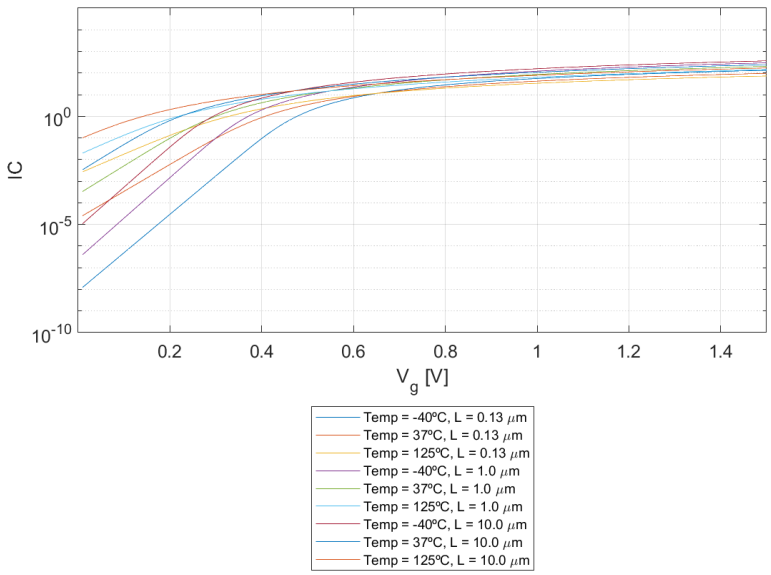

Figure 5.14: The inversion coefficient versus the gate voltage of the nMOS. *IC* is represented in logarithmic scale.

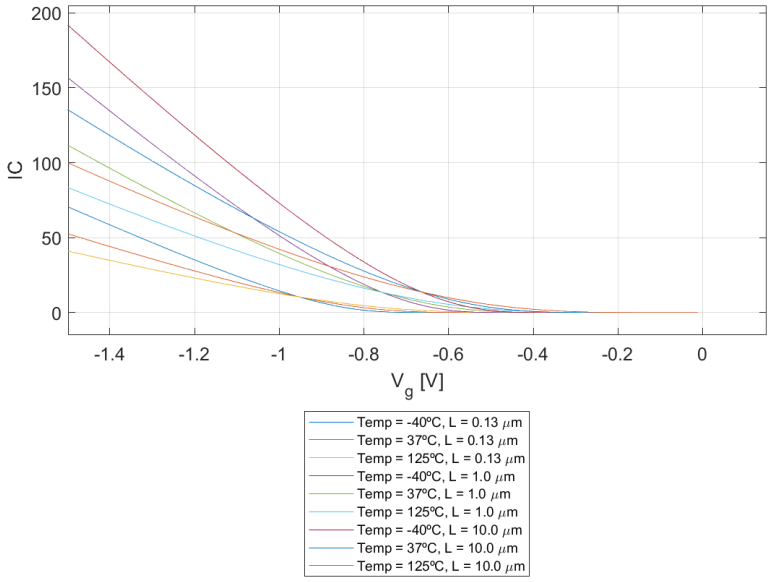

Figure 5.15: The inversion coefficient versus the gate voltage of the pMOS. *IC* is represented in linear scale.

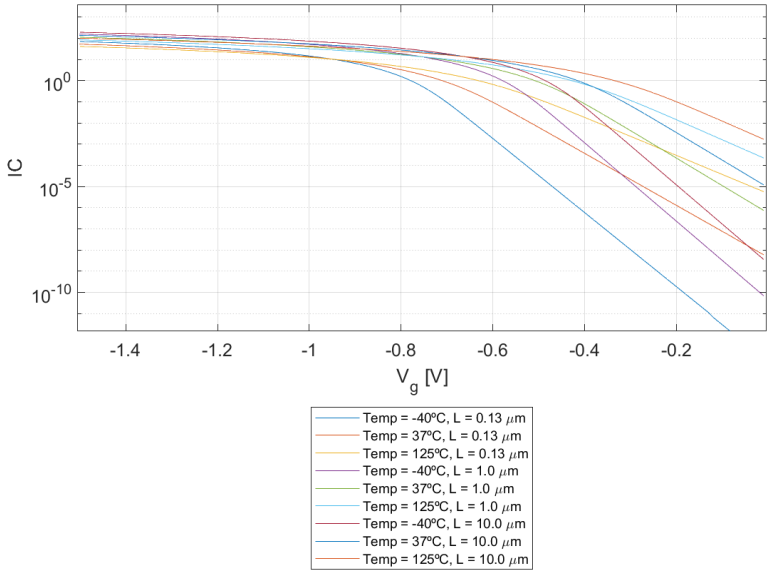

Figure 5.16: The inversion coefficient versus the gate voltage of the pMOS. *IC* is represented in logarithmic scale.

After obtaining the results of the simulations, we can see how the inversion coefficient behaves with respect to the gate voltage. In the respective figures 5.13, 5.14, 5.15 and 5.16, it can be seen how the temperature has more influence on the IC than the geometry of the device. This is one of the objectives that the ekv model aims to achieve, that the device is independent

of the type of technology [9]. Therefore, we can see that for higher temperature values the inversion coefficient for the same value of V_g decreases.

Despite the fact that the model seeks the greatest possible independence of the technology, these simulations have been made with extreme cases with respect to the channel length, so it can be seen that the shorter the channel length, the steeper the slope of the graph.

With regard to the different inversion regions, it can be seen how in weak inversion the domain of the gate voltage is almost null, we can see in the figures with logarithmic scale how the graph is almost a straight line with a slope that is determined by the subthreshold slope. Entering the region of moderate inversion, we see how the gate voltage is gaining more dominance and in the linear scale graphs it starts to change its growth, due to the combination of the diffusion and drift currents. Around the point where IC is one, the crossover point between diffusion and drift can be seen. Finally, in strong inversion, we can see how the drain current becomes a linear function of the gate voltage.

Following the simulation of the gate voltage with respect to the inversion coefficient, the subsequent step will be to simulate the capacitance between the gate and the source with respect to the gate voltage. This will be achieved through the utilization of multiple cases, with the technology and operating temperature being varied.

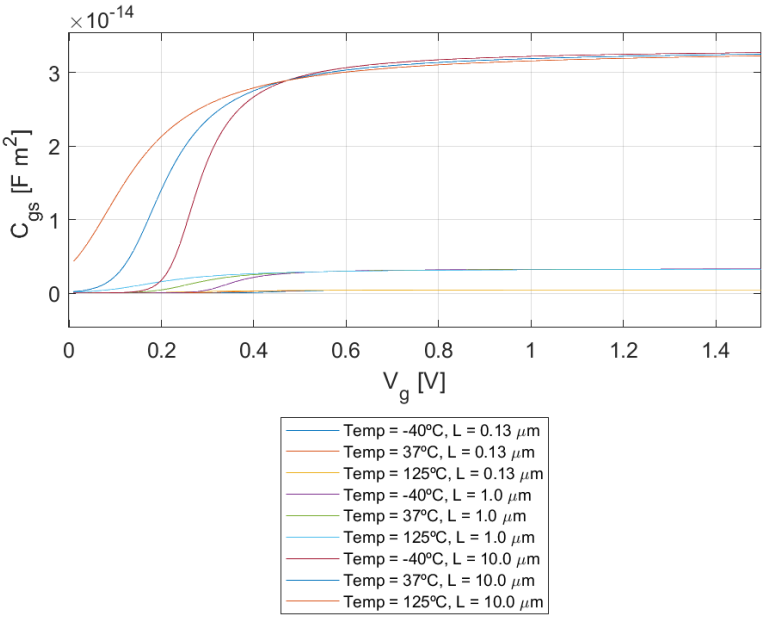

Figure 5.17: The capacitance between the gate to the source versus the gate voltage of the nMOS. C_{gs} is represented in linear scale.

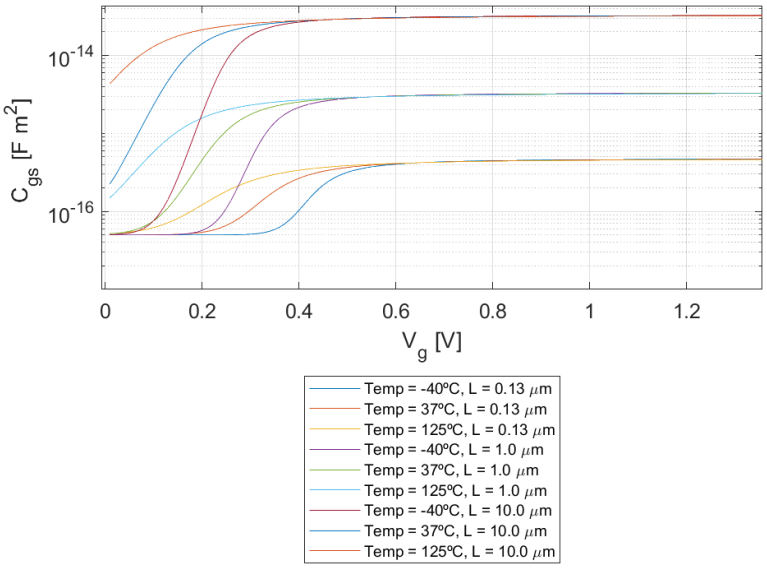

Figure 5.18: The capacitance between the gate to the source versus the gate voltage of the nMOS. C_{gs} is represented in logarithmic scale.

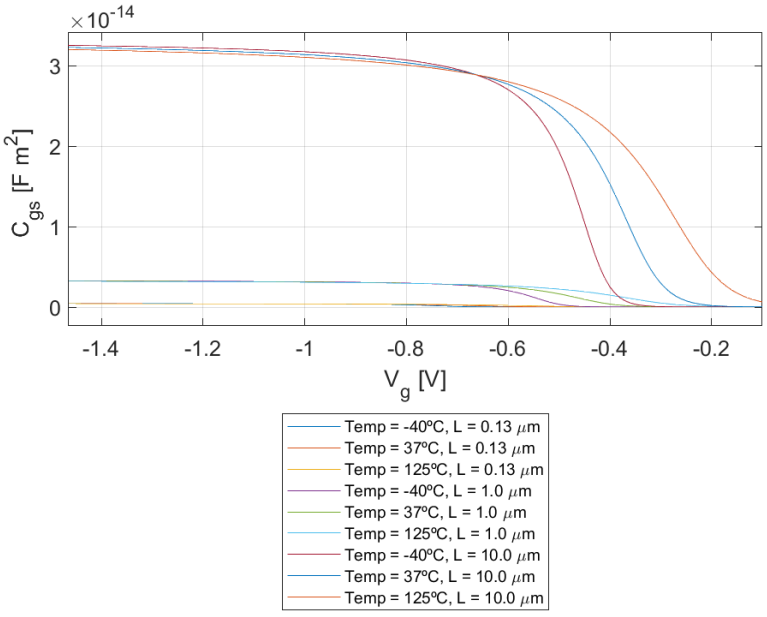

Figure 5.19: The capacitance between the gate to the source versus the gate voltage of the pMOS. C_{gs} is represented in linear scale.

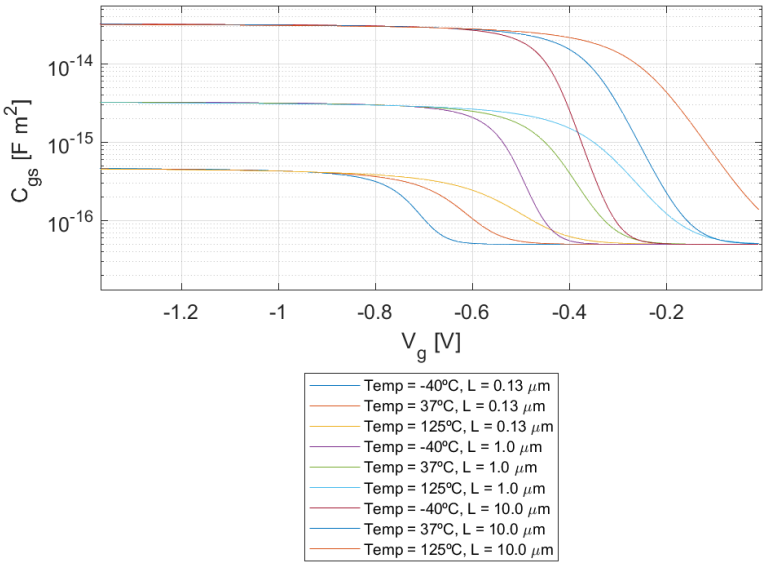

Figure 5.20: The capacitance between the gate to the source versus the gate voltage of the pMOS. C_{gs} is represented in logarithmic scale.

The capacitance between the gate and the source can be analyzed to reveal its reaction to changes in gate voltage, as demonstrated in figures 5.17, 5.18, 5.19 and 5.20. It is evident that the behaviour of this capacitance remains consistent irrespective of the type of transistor, functioning in a manner that is equivalent to both an nMOS and a pMOS.

As demonstrated in the logarithmic graph, the capacitance attains its maximum value contingent on the channel length. It is evident that an increase in channel length corresponds to an elevated capacitance value. The graph also demonstrates the recovery in inversion that the capacitance undergoes at higher gate voltage values. With regard to the slopes of the graphs, a clear dependence on temperature is evident, whereby steeper slopes correspond to higher temperatures. However, it has been observed that the transitions exhibit more pronounced edges in cases where the channel length is reduced.

In addition, it is evident that for disparate values of channel length, the stationary value of the conductance between the gate and the source is expressed as follows in Equation 5.1.

$$C_{gs} = \frac{2}{3} \cdot W \cdot L \cdot C'_{ox} \tag{5.1}$$

Conversely, figures 5.17 and 5.19 demonstrates that as the voltage V_g decreases, the accumulation zone becomes predominant. As this value approaches the threshold voltage, the

accumulation zone begins to enter the deplexing zone, and C_{gs} falls to a minimum. Consequently, as V_g continues to increase, the gate carrier layer reappears and C_{gs} reaches its maximum.

In conclusion, the gate transconductance will be simulated as a function of gate voltage. This will be conducted for a variety of gate lengths and at different temperatures. The model will be operated as both an nMOS and a pMOS.

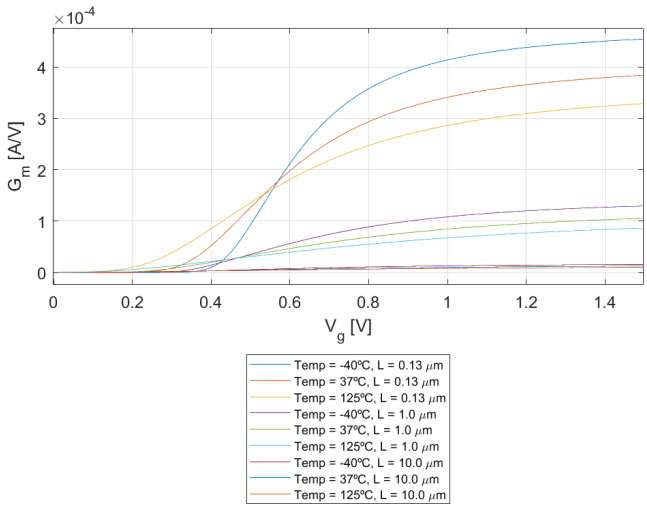

Figure 5.21: The gate transconductance of the nMOS versus the gate voltage. g_m is represented in linear scale.

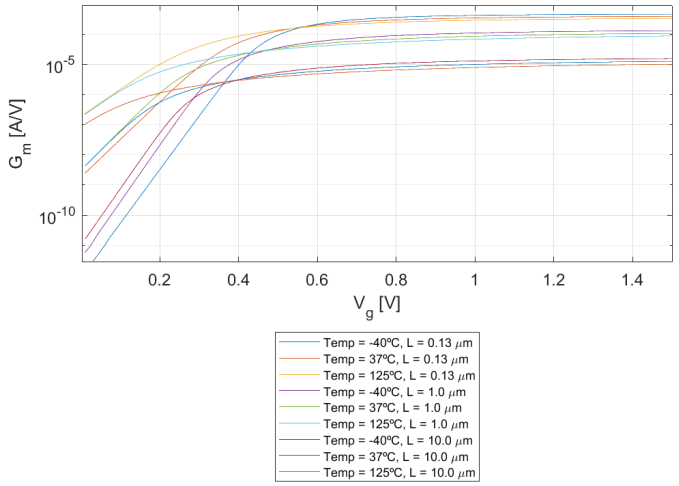

Figure 5.22: The gate transconductance of the nMOS versus the gate voltage. g_m is represented in logarithmic scale.

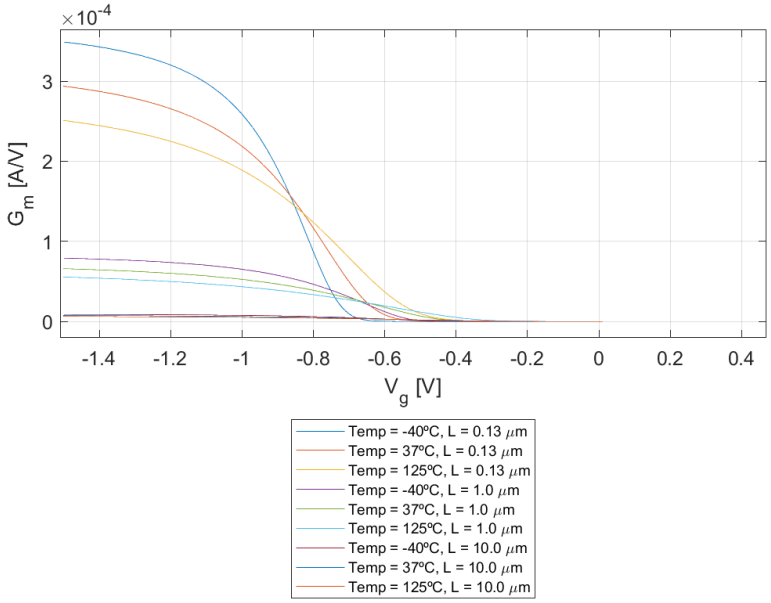

Figure 5.23: The gate transconductance of the pMOS versus the gate voltage. g_m is represented in linear scale.

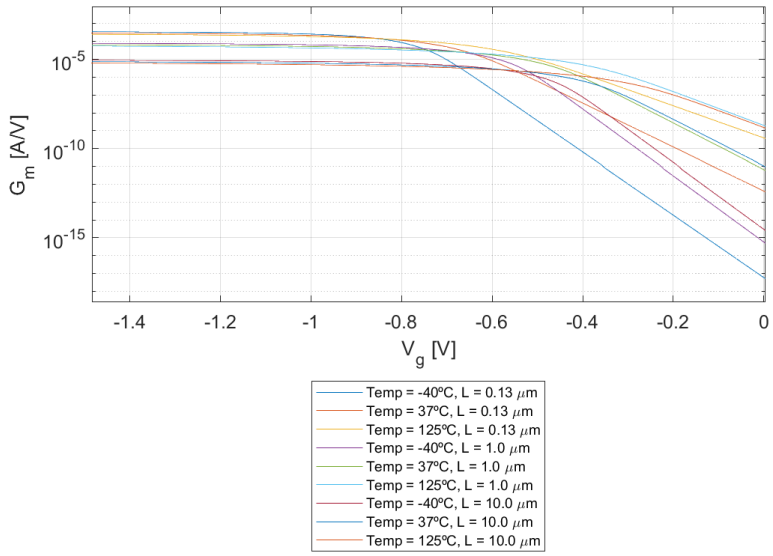

Figure 5.24: The gate transconductance of the pMOS versus the gate voltage. g_m is represented in logarithmic scale.

In conclusion, the gate transconductance will be simulated as a function of gate voltage, once again for various gate lengths, at different temperatures, and with the model acting as an nMOS and as a pMOS.

Following this simulation, the behaviour of G_m versus gate voltage will be obtained, as demonstrated in figures 5.21, 5.22, 5.23 and 5.24. As demonstrated in the graphs above the transconductance on a logarithmic scale, for very low values of V_g, on the sub-threshold region of the transistor, the transconductance is observed to be almost zero. Conversely, as V_g approaches the threshold voltage, the transconductance, designated as G_m, commences to increase. As the V_g increases until the strong inversion is reached, it is observed that G_m grows with respect to the $|V_g - V_t|$ difference.

Conversely, the graphs presented on a logarithmic scale demonstrate the attainment of maximum gate transconductance, thereby indicating its dependence on the length of the channel, so it is evident see that the transconductance increases as the length of the channel decreases.

Furthermore, it is evident that the G_m value exhibits a more precipitous decline in the P-type device when compared to the nMOS.

5.4 Source Behaviour

In order to ascertain the behaviour of the MOSFET in relation to fluctuations in the source voltage with reference to the bulk, a simulation will be conducted in which the current from the drain to the source will be examined in relation to the source voltage. Additionally, the normalized source transconductance will be analyzed against this source voltage. The simulations will be conducted for three distinct temperature values, namely -40°C, 37°C, and 125°C, as is customary in analogous cases. Furthermore, the channel length was varied across three distinct values, all of which were nanometric in size.

The initial stage of the research involved the simulation of the current between the drain and the source in relation to the source voltage. This process yielded the graphs illustrated in figures 5.25, 5.26, 5.27 and 5.28.

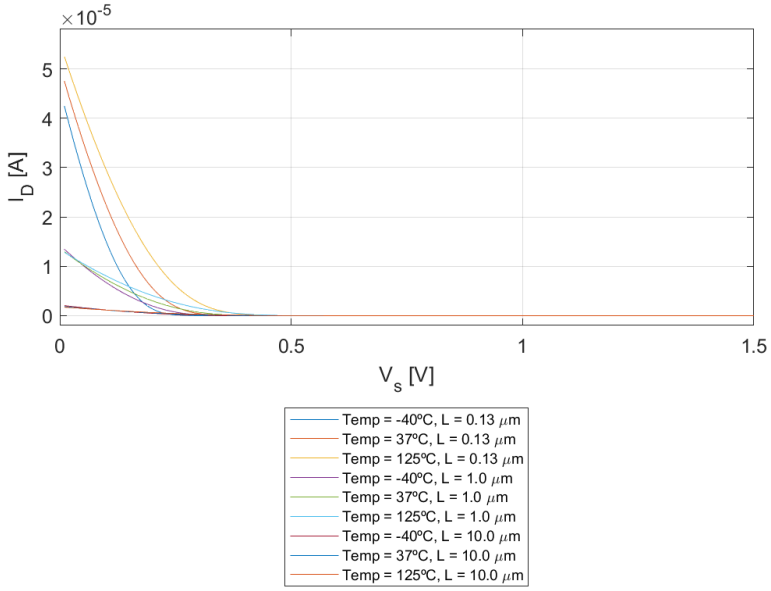

Figure 5.25: The drain current of the nMOS versus the source voltage. I_{ds} is represented in linear scale.

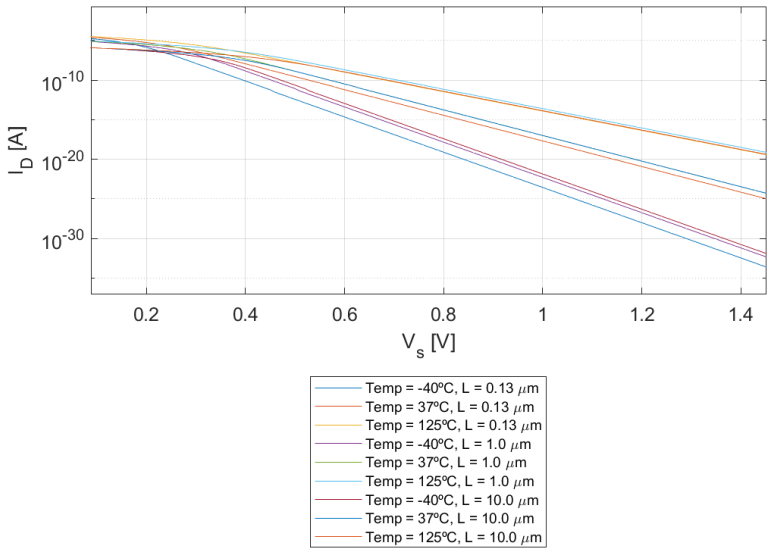

Figure 5.26: The drain current of the nMOS versus the source voltage. I_{ds} is represented in logarithmic scale.

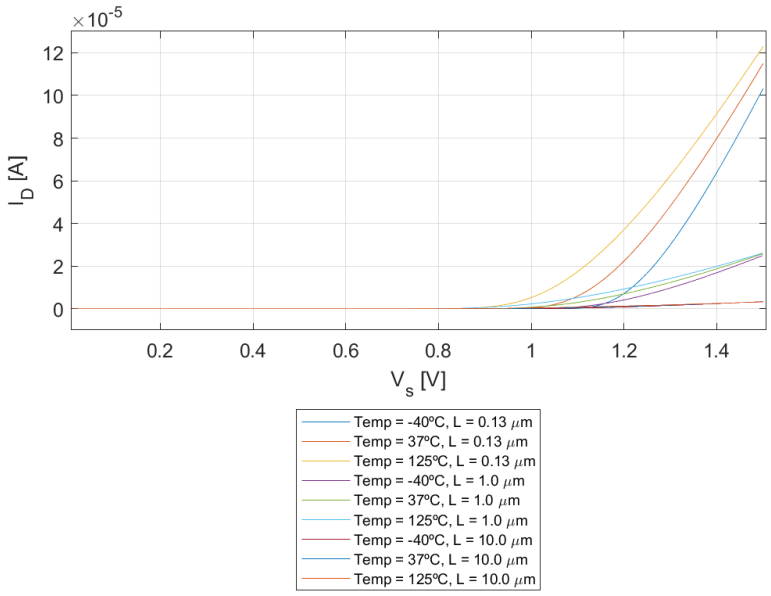

Figure 5.27: The drain current of the pMOS versus the source voltage. I_{ds} is represented in linear scale.

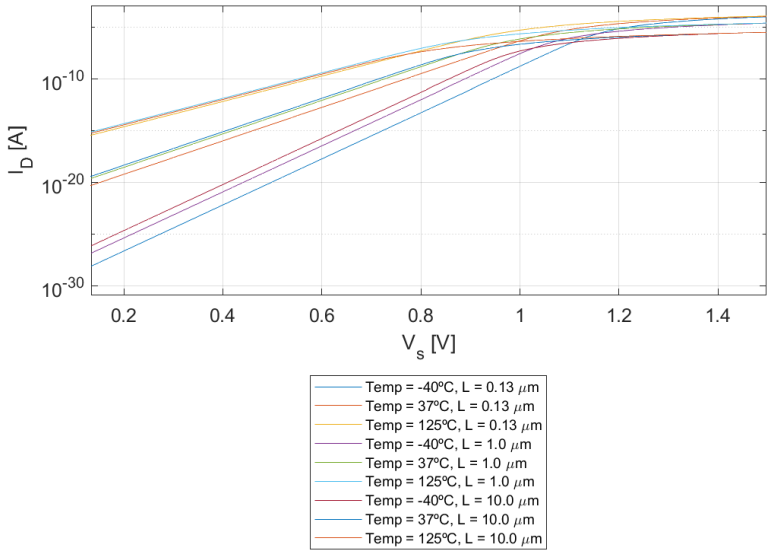

Figure 5.28: The drain current of the pMOS versus the source voltage. I_{ds} is represented in logarithmic scale.

The graphs obtained demonstrate that the device's behaviour is in accordance with expectations. In the nMOS device, an inverse relationship is observed between the current in the drain and the source voltage, with higher values recorded when the source voltage is lower. This is due to the fact that the nMOS will form the channel whenever $V_{gs} > V_t$. Therefore, as the source voltage is increased without an increase in the gate voltage, a moment will occur in which the threshold voltage will exceed the V_{gs} voltage, thus resulting in the transistor entering the cut-off region.

In the case of the pMOS, the opposite is true: this device is activated with negative gate voltages. As the source voltage rises, the voltage across the channel V_{gs} also rises, until the channel is formed and the device starts to conduct. This results in an I_{gs} current.

It is evident that, in both cases, the drain current of both nMOS and pMOS reaches reasonable values, in the order of 10^{-5}, at the point of conduction. It has been demonstrated that, within the specified region of operation, the length of the channel is the determining factor in the value of the current through the channel. However, the differences in current values are not significant, as previously explained. This is due to the fact that the ekv model aims to create devices that are independent of the technology employed.

The subsequent simulation will be the normalized source transconductance versus source voltage. This simulation will be conducted once more, this time incorporating a range of

temperatures and channel lengths. The graphs presented in the figures 5.29, 5.30, 5.31 and 5.32, are obtained through the following process.

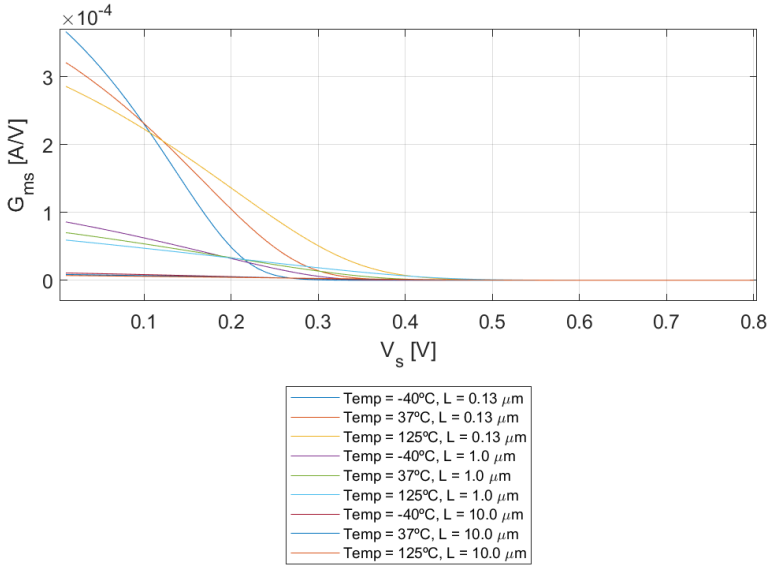

Figure 5.29: The source transconductance of the nMOS versus the source voltage. g_{ms} is represented in linear scale.

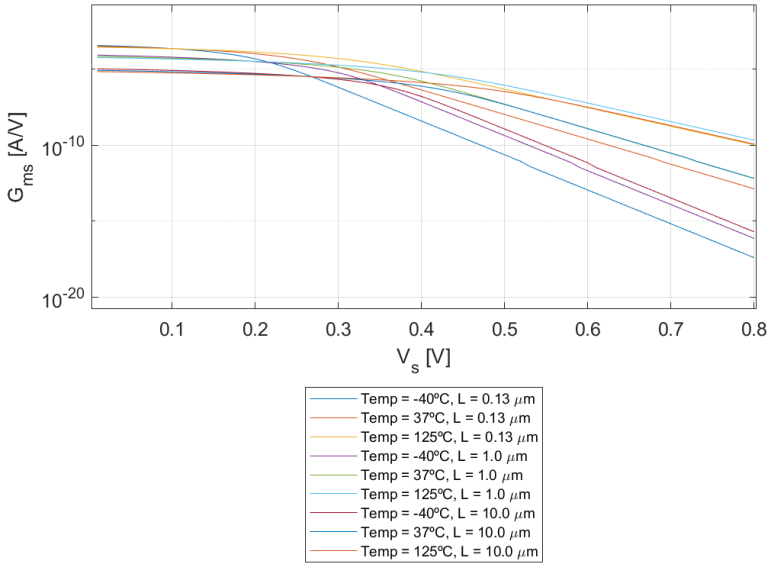

Figure 5.30: The source transconductance of the nMOS versus the source voltage. g_{ms} is represented in logarithmic scale.

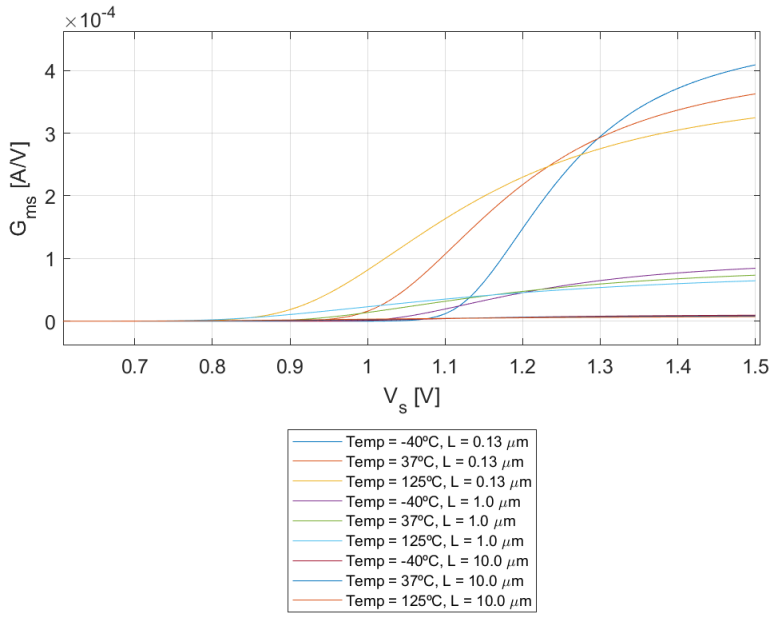

Figure 5.31: The source transconductance of the pMOS versus the source voltage. g_{ms} is represented in linear scale.

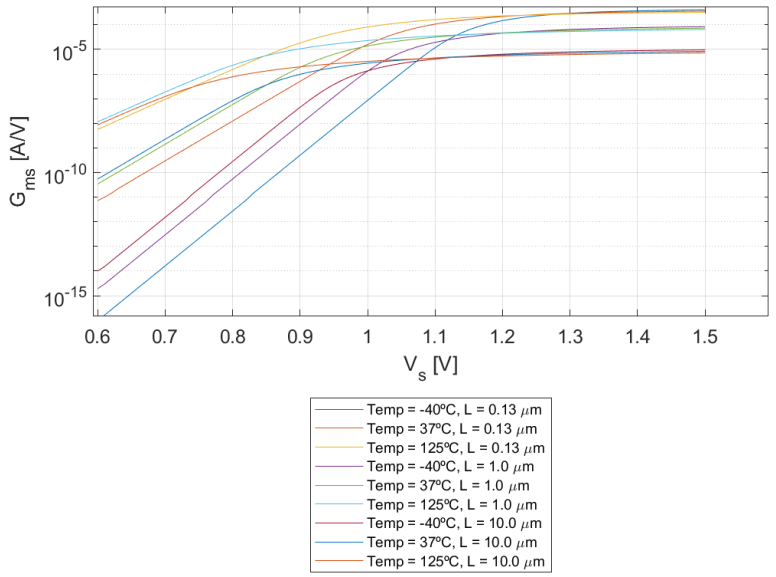

Figure 5.32: The source transconductance of the pMOS versus the source voltage. g_{ms} is represented in logarithmic scale.

The subsequent simulation will be the source transconductance versus source voltage. This simulation will be conducted once more, this time incorporating a range of temperatures and channel lengths. This process yields the graphs presented in the figures above. In a manner analogous to the graphs where the drain current versus source voltage was simulated, it is

evident that the transconductance of the source is practically zero in the MOSFET cut-off region. In the nMOS, this phenomenon occurs for high V_s voltage. Conversely, in the pMOS, the opposite is observed when entering the active region at $V_{sg} > V_t$.

As demonstrated in the graphs, provided the device remains in the cut-off region, no current is conducted through the channel, regardless of the magnitude of the source voltage. Consequently, the efficacy of the source control over the channel current is minimal.

5.5 Common Source Amplifier

The common source amplifier is one of the most widely utilized and elementary configurations in which a MOSFET can be employed. As indicated by its nomenclature, the characteristic feature of this configuration is the connection of the source node to ground, as illustrated in figure 5.33. Consequently, the input and output signals are referenced to the same node. The input of the circuit is applied at the gate of the transistor, while the output is taken from the drain node, usually in the form of a voltage.

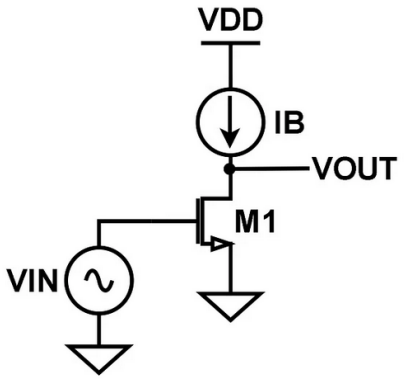

Figure 5.33: Schematic of a Common source amplifier with ideal current source load.

(Nicholas St. John (February 21, 2024) "Introduction to the MOSFET Common-Source Amplifier." *https://www.allaboutcircuits.com/technical-articles/introduction-to-the-mosfet-common-source-amplifier/*)

In order to simulate this circuit, it is necessary to set certain significant values as constants. It is assumed that the current I_B is the drain current, I_{ds}, which is set at $I_B = I_{ds} = 100.0\mu A$. Furthermore, it is assumed that the specific current per square is I_o, and this is set at $500.0nA$. Subsequent to the establishment of these two values, a sweep will be conducted through a range of inversion coefficients to obtain the corresponding channel width values. In order to accomplish this objective, it is necessary to employ the most fundamental equations of the model. Furthermore, the simulation will be conducted for three distinct values of channel

length: $10.0\mu m$, $1.0\mu m$, and $0.13\mu m$. The latter represents the minimum length that a functional MOSFET can possess, in accordance with the stipulated parameters.

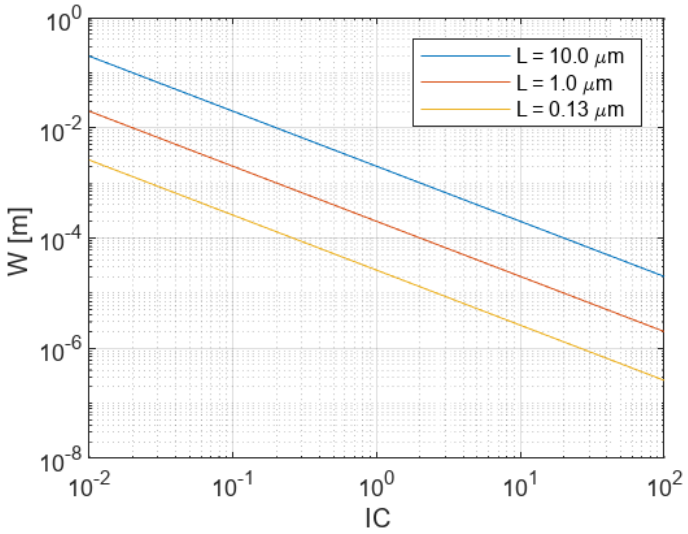

Figure 5.34: The coefficient of inversion versus the wight of the nMOS in a common source amplifier.

The execution of this simulation yields the graph depicted in figure 5.34, which presents the channel width values for the various inversion coefficients. As is evident, the data displays a linear relationship, a consequence of the equation from which this characteristic is derived.

A more detailed analysis reveals that, when IC assumes the values 0.01 or 100, the channel width attains extreme values. Nevertheless, these values remain within the feasible range for the analogue device. As demonstrated in the example where $IC = 0.01$ and $L = 1.0\mu m$, with $W = 20,000\mu m$, this would necessitate the utilization of smaller channel width MOSFETs in parallel placement, constituting an acceptable solution.

5.6 Source Transconductance

In the subsequent stage of the investigation, the response of the normalized source transconductance efficiency to alterations in the device's parameters will be simulated. This will allow the comprehensive study of the model to be continued in Verilog-A.

The normalized source transconductance efficiency will be confronted with the current flowing through the channel, that which goes from the drain to the source. The simulations will be conducted utilizing a range of channel lengths and temperatures, with the model operating in both nMOS and pMOS configurations. The ensuing graphs are 5.35, 5.36, 5.37 and 5.38.

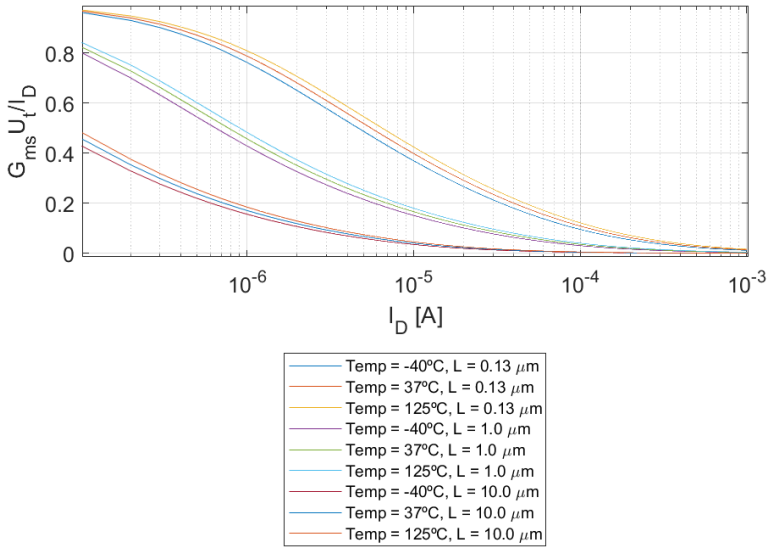

Figure 5.35: $\frac{G_{ms} \cdot U_t}{I_{ds}}$ of the nMOS versus the drain current. $\frac{G_{ms} \cdot U_t}{I_{ds}}$ is represented in linear scale.

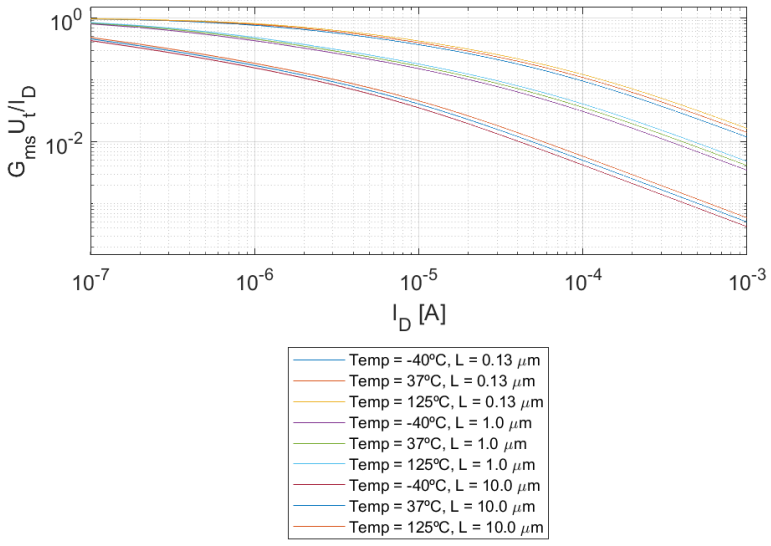

Figure 5.36: $\frac{G_{ms} \cdot U_t}{I_{ds}}$ of the nMOS versus the drain current. $\frac{G_{ms} \cdot U_t}{I_{ds}}$ is represented in logarithmic scale.

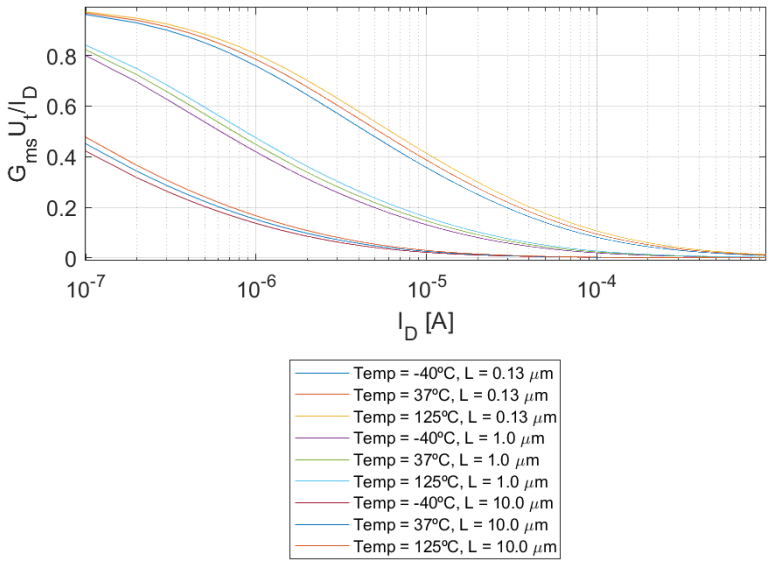

Figure 5.37: $\frac{G_{ms} \cdot U_t}{I_{ds}}$ of the pMOS versus the drain current. $\frac{G_{ms} \cdot U_t}{I_{ds}}$ is represented in linear scale.

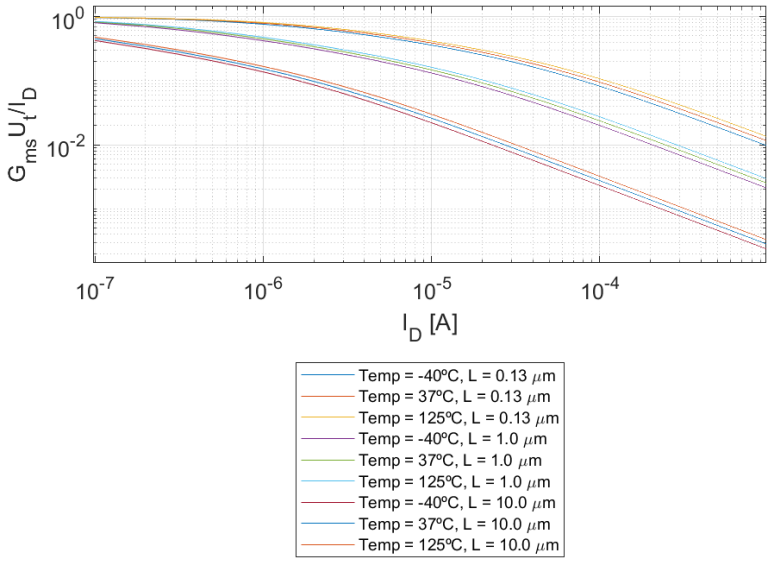

Figure 5.38: $\frac{G_{ms} \cdot U_t}{I_{ds}}$ of the pMOS versus the drain current. $\frac{G_{ms} \cdot U_t}{I_{ds}}$ is represented in logarithmic scale.

As demonstrated in the graphs, the normalized source transconductance efficiency exhibits an inverse relationship with the current through the channel. This phenomenon can be attributed to the fact that, in a state of weak inversion, the transconductance is high while the current is low. Conversely, as the transistor approaches moderate or strong inversion, its behaviour transitions from exponential to non-exponential, leading to a decline in source transconductance.

Furthermore, a discernible divergence in its sensitivity to temperature is evident, as the increase in temperature exerts a substantial influence on mobility. As previously mentioned, the curve of the nMOS transconductance is slightly higher than that of the pMOS. This phenomenon can be attributed to the high mobility of the electrons, which enhances the efficiency of the device.

It is evident that the phenomenon of weak inversion is characterized by the maintenance of a high source transconductance. The moderate inversion phase is marked by a decline in this value, while strong inversion is characterized by a re-establishment of the value at zero.

It is evident that the length of the channel has a direct correlation with the transconductance value of the source, with an decrease in channel length resulting in a higher transconductance value.

Following the simulation of the normalized source transconductance efficiency against the drain current, the same process will be repeated against the inversion coefficient. The following figures, 5.39, 5.40, 5.41 and 5.42, are obtained from the simulation.

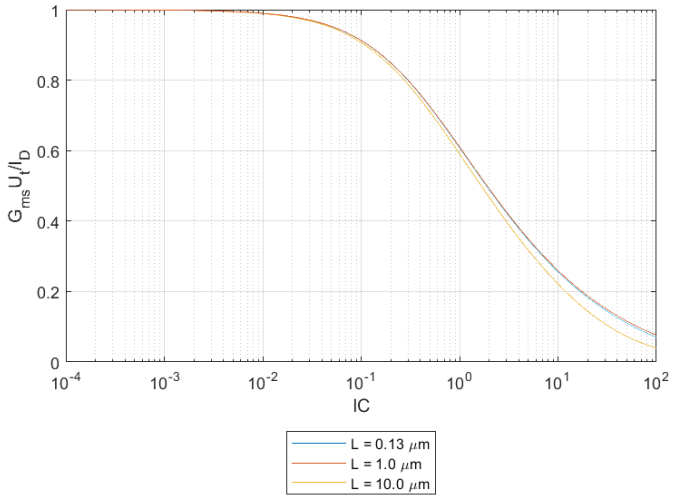

Figure 5.39: $\frac{G_{ms} \cdot U_t}{I_{ds}}$ of the nMOS versus the inversion coefficient. $\frac{G_{ms} \cdot U_t}{I_{ds}}$ is represented in linear scale.

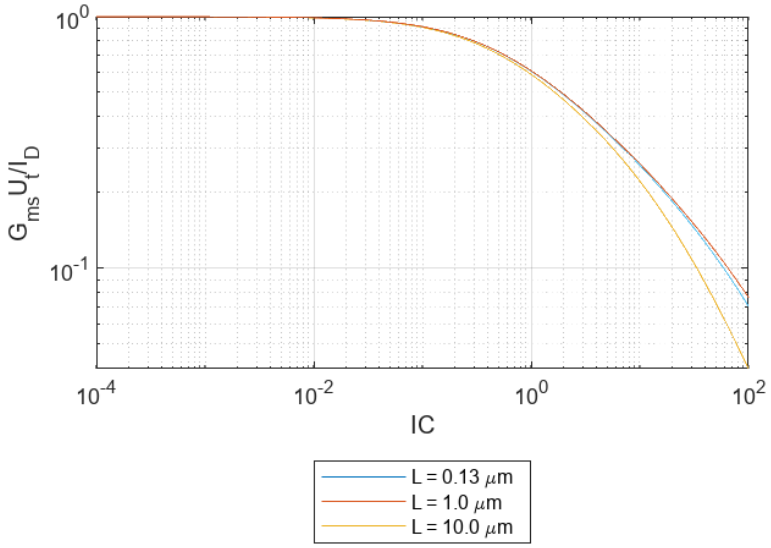

Figure 5.40: $\frac{G_{ms} \cdot U_t}{I_{ds}}$ of the nMOS versus the inversion coefficient. $\frac{G_{ms} \cdot U_t}{I_{ds}}$ is represented in logarithmic scale.

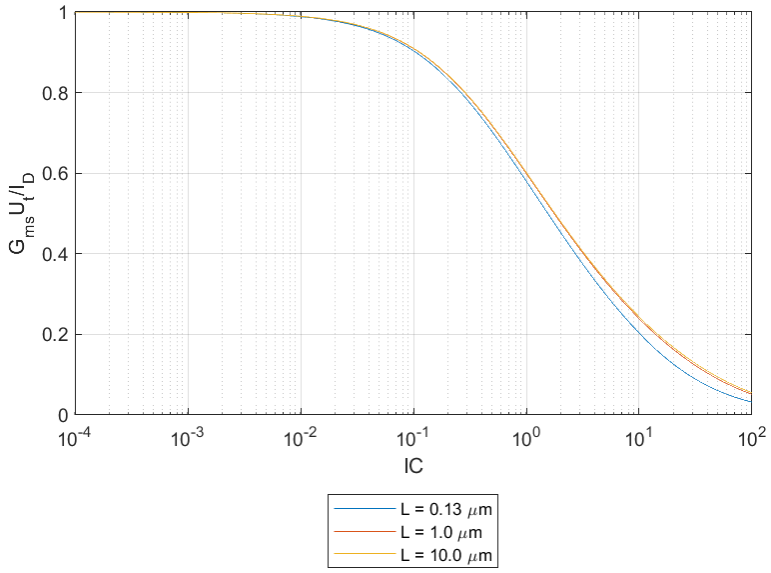

Figure 5.41: $\frac{G_{ms} \cdot U_t}{I_{ds}}$ of the pMOS versus the inversion coefficient. $\frac{G_{ms} \cdot U_t}{I_{ds}}$ is represented in linear scale.

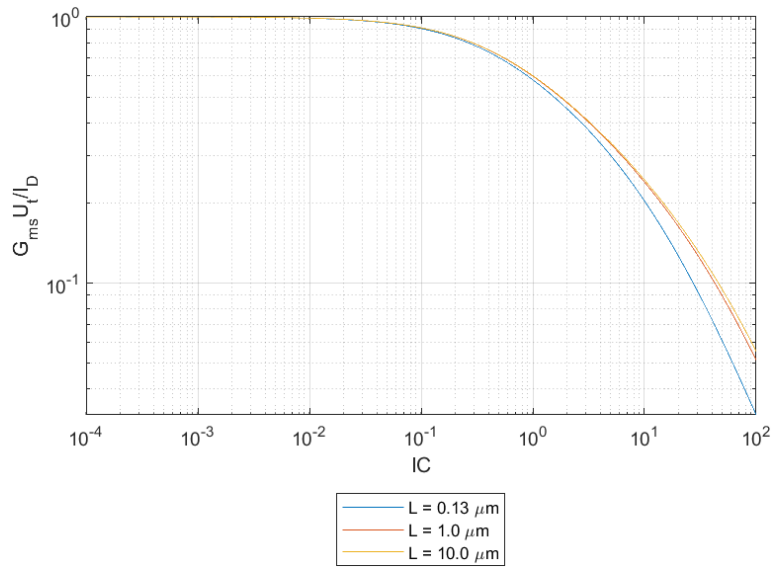

Figure 5.42: $\frac{G_{ms} \cdot U_t}{I_{ds}}$ of the pMOS versus the inversion coefficient. $\frac{G_{ms} \cdot U_t}{I_{ds}}$ is represented in logarithmic scale.

As previously outlined, in the case of weak inversion, the value of transconductance remains elevated, given that elevated values are attained for each unit of current. As demonstrated in previous graphs, the length of the channel has a direct impact on the behaviour of the transconductance of the source. It can be deduced that as the channel length decrease, the secondary effects of the channel resistance versus the conductance gets less pronounced, leading to an increase in the value of the source transconductance in strong inversion. Furthermore, it is evident that the value in the nMOS exceeds that of the pMOS in strong inversion, as previously discussed.

As evidenced by the figures 5.40 and 5.42, the efficiency declines with increasing levels of inversion. This phenomenon can be attributed to the necessity for elevated current levels to achieve equivalent transconductance values.

This is the inverse scenario of the weak inversion, where a high and stable value is observed. This is attributable to the fact that, in this region, the transconductance of the source is contingent on the slope factor. As is understood, this is a parameter that is contingent on the technology type.

5.7 Gate Transconductance

The subsequent stage of the process is to simulate the normalized gate transconductance efficiency, once more with respect to the drain current. As previously outlined, the present simulation will be conducted for three distinct cases of temperature and three cases of gate length. The model will be configured to operate as both an n-channel metal oxide semiconductor, nMOS, and a p-metal oxide semiconductor, pMOS.

The initial stage of the research is the simulation of the transconductance of the gate versus the drain current. The results of this simulation are presented in the graphs shown in figures 5.43, 5.44, 5.45 and 5.46.

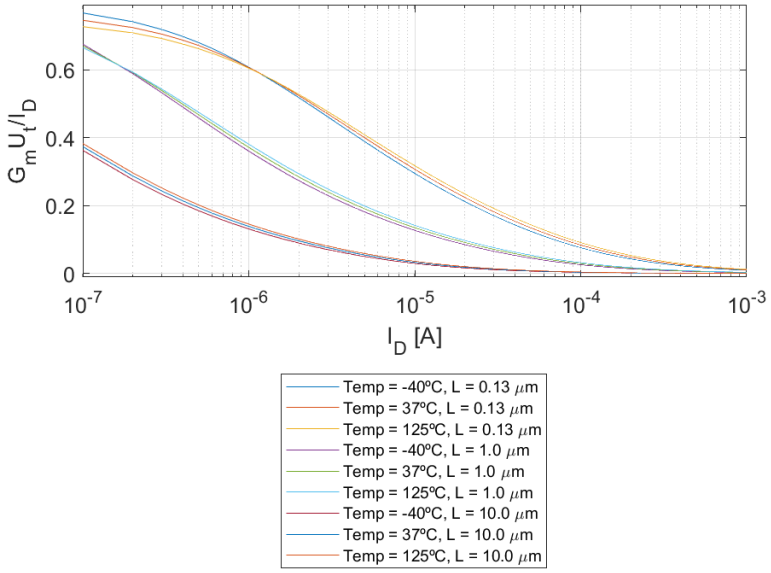

Figure 5.43: $\frac{G_m \cdot U_t}{I_{ds}}$ of the nMOS versus the drain current. $\frac{G_m \cdot U_t}{I_{ds}}$ is represented in linear scale.

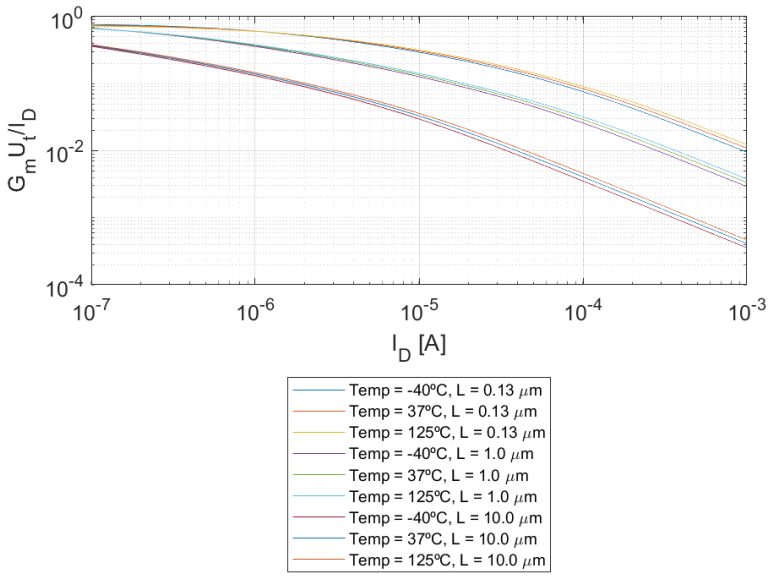

Figure 5.44: $\frac{G_m \cdot U_t}{I_{ds}}$ of the nMOS versus the drain current. $\frac{G_m \cdot U_t}{I_{ds}}$ is represented in logarithmic scale.

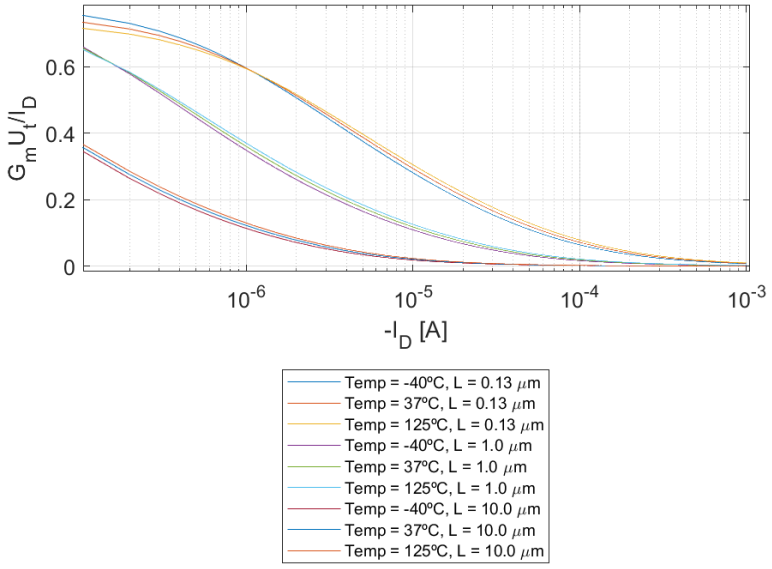

Figure 5.45: $\frac{G_m \cdot U_t}{I_{ds}}$ of the pMOS versus the drain current. $\frac{G_m \cdot U_t}{I_{ds}}$ is represented in linear scale.

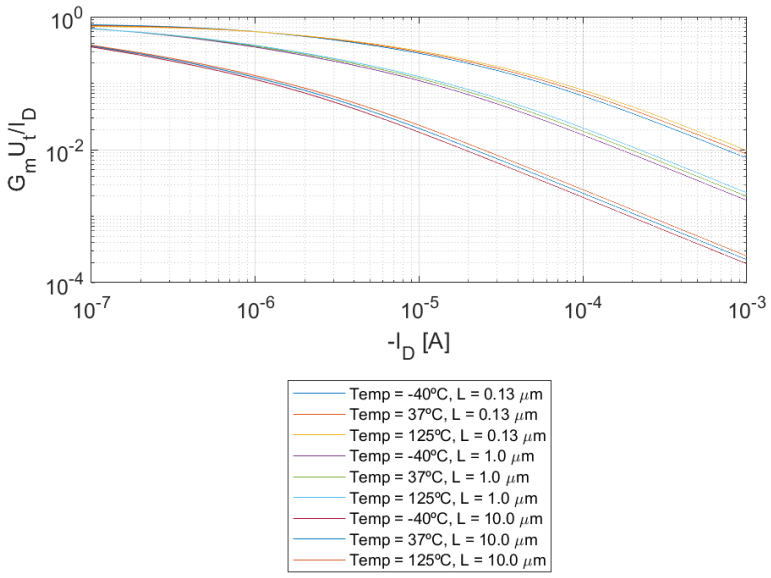

Figure 5.46: $\frac{G_m \cdot U_t}{I_{ds}}$ of the pMOS versus the drain current. $\frac{G_m \cdot U_t}{I_{ds}}$ is represented in logarithmic scale.

This phenomenon can be attributed to the inherent characteristics of this magnitude, which quantifies the variation of I_{ds} as a function of the change in voltage between the gate and the source. It is noteworthy that this voltage assumes greater significance when the device operates in cut-off or in the linear zone. However, as the current increases, the transistor approaches the saturation zone, wherein the gate voltage is incapable of exerting control over the channel, leading to a decline in the normalized gate transconductance efficiency to nearly zero.

This phenomenon is further elucidated in figures 5.44 and 5.46, which demonstrate a direct correlation between the length of the channel and the device's performance. Specifically, it can be concluded that within the nanometric devices, an decrease in channel length corresponds to a corresponding increase in the gate transconductance.

A comparison of the nMOS and pMOS plots reveals minor discrepancies. While the overall behaviour is comparable, it is evident that the nMOS exhibits higher values when the drain current increase, attributable to its superior conductance capacity, thereby facilitating the generation of more substantial currents.

The subsequent simulation to be conducted to evaluate the performance of the MOSFET normalized gate transconductance efficiency will involve the comparison of this magnitude

with the inversion coefficient. This will be undertaken for a range of values of channel length and operating temperature.

The following results are obtained from the execution of the aforementioned simulations, as illustrated in figures 5.47, 5.48, 5.49 and 5.50.

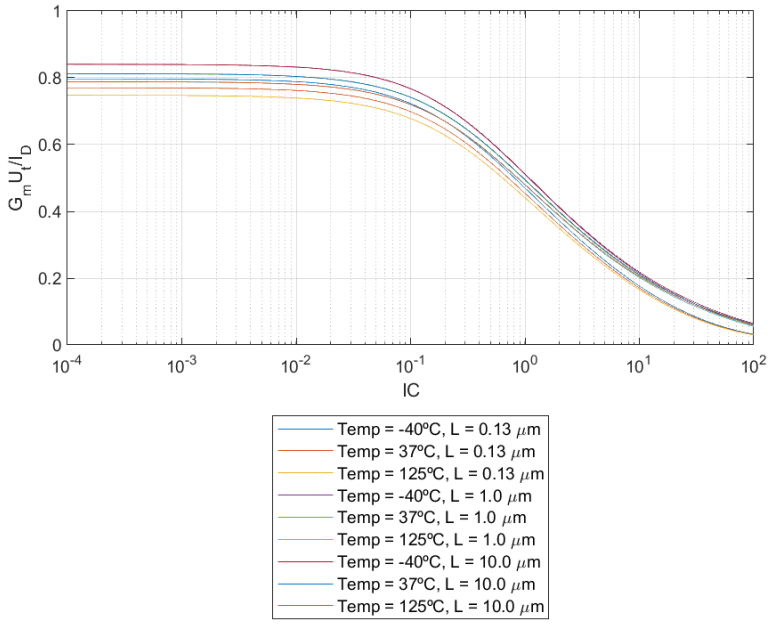

Figure 5.47: $\frac{G_m \cdot U_t}{I_{ds}}$ of the nMOS versus the inversion coefficient. $\frac{G_m \cdot U_t}{I_{ds}}$ is represented in linear scale.

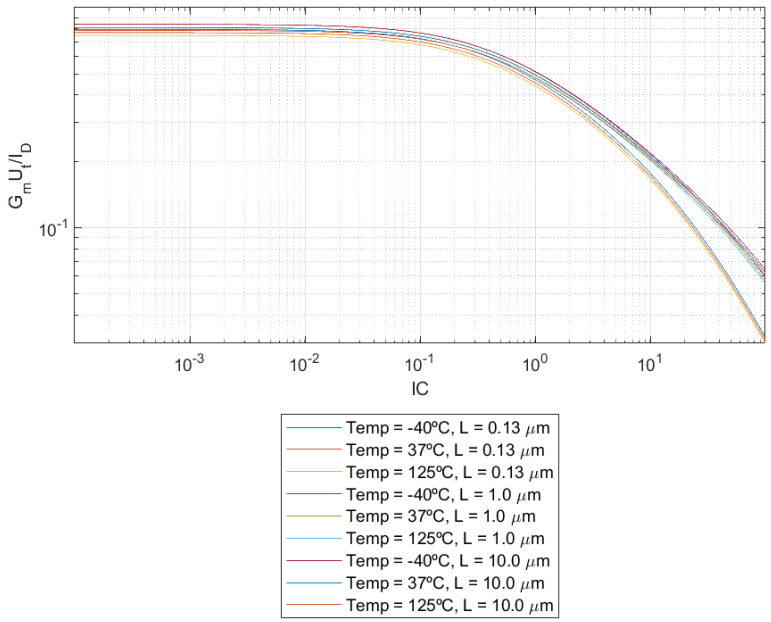

Figure 5.48: $\frac{G_m \cdot U_t}{I_{ds}}$ of the nMOS versus the inversion coefficient. $\frac{G_m \cdot U_t}{I_{ds}}$ is represented in logarithmic scale.

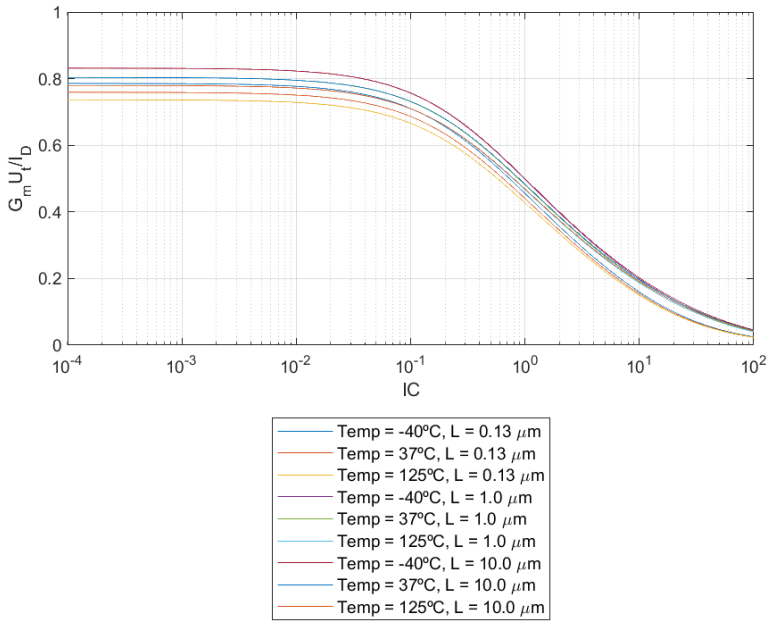

Figure 5.49: $\frac{G_m \cdot U_t}{I_{ds}}$ of the pMOS versus the inversion coefficient. $\frac{G_m \cdot U_t}{I_{ds}}$ is represented in linear scale.

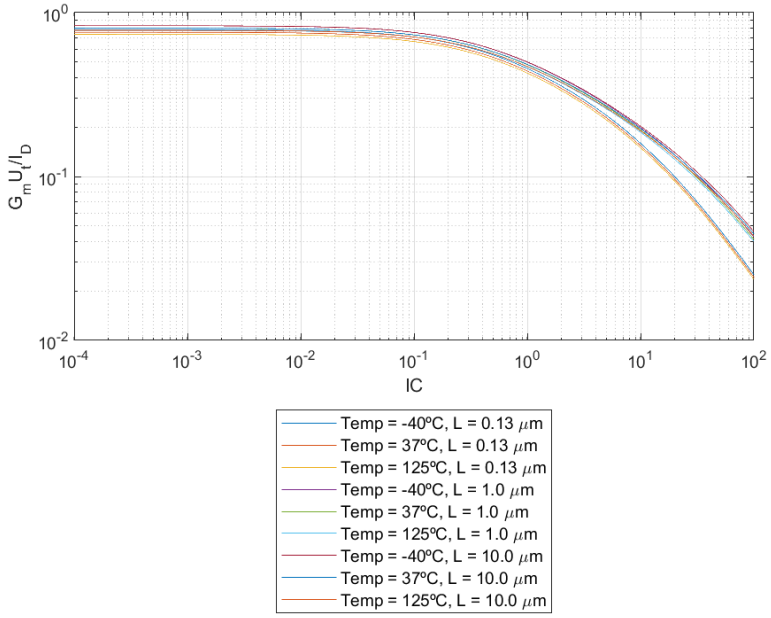

Figure 5.50: $\frac{G_m \cdot U_t}{I_{ds}}$ of the pMOS versus the inversion coefficient. $\frac{G_m \cdot U_t}{I_{ds}}$ is represented in logarithmic scale.

In these simulations, the behaviour is analogous to the previous ones, with the distinction that here the different inversion zones can be discerned more clearly since we are representing the IC directly.

As demonstrated in the accompanying graphs, within the weak inversion region, the transconductance of the transistor is elevated due to the diminished value of the drain current. This effect is further diminished in the strong inversion region, as the MOSFET attains a saturated state, thereby becoming independent of the gate voltage value.

5.8 Flicker Noise

Following the execution of the aforementioned analyses, the verification of the model's operational integrity will be finalized through the simulation of its response to noise, both in the drain current and in the gate voltage.

The utilization of flicker noise in this context signifies the impact of random variations in carriers within the channel on the device. This phenomenon arises due to the attraction and release of carriers by the channel-oxide interface, resulting in an undesired effect.

In order to observe the effect of the flicker noise, the following experiment will be conducted. The flicker noise will be simulated against the inversion coefficient. The noise will be applied

to the gate voltage and also to the current between the drain and the source. Furthermore, the aforementioned simulations will be conducted at varying channel lengths to ascertain the effect of the device geometry on the disturbance.

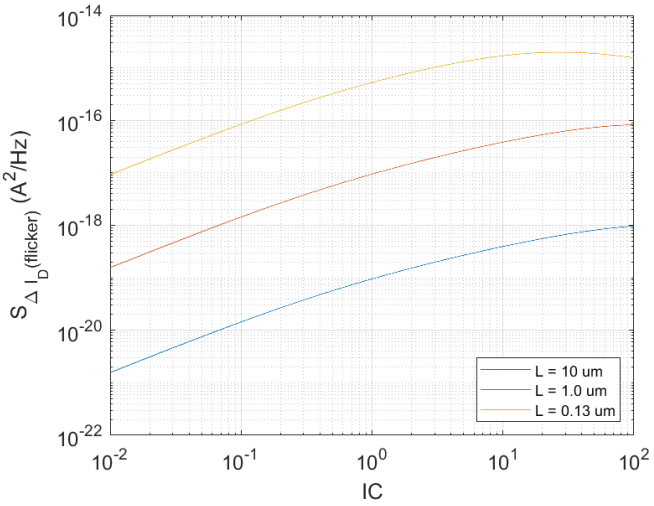

Figure 5.51: Density of the flicker noise in the drain current versus the inversion coefficient of a nMOS with a fixed $W = 0.5\mu m$.

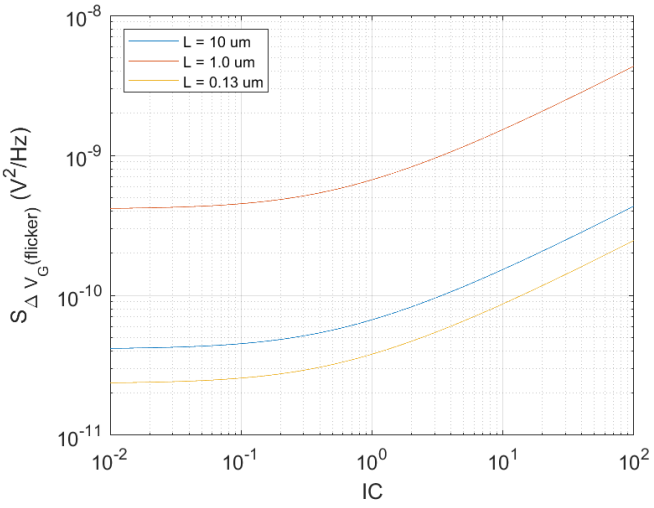

Figure 5.52: Density of the flicker noise in the gate voltage versus the inversion coefficient of a nMOS with a fixed $W = 0.5\mu m$.

As illustrated in figure 5.51, the variation of flicker noise applied to the drain current is demonstrated. Figure 5.52 further elucidates the noise applied to the gate voltage of the device. For both simulations, the model has been implemented as an nMOS with the

geometry fixed, the width remains at $0.5\mu m$ and we simulated for the different values of the channel length. In order to obtain the simulation of the flicker noise versus the inversion coefficient we change the gate voltage, so the drain current suffer a variation and therefore the inversion coefficient.

It is evident that, given this knowledge, an analysis of the noise behaviour can be conducted. This analysis will demonstrate how, in the context of weak inversion, the noise is maintained at reduced values in both cases. This is due to the fact that, in the inversion region where the transconductance is maximum, the noise density applied to the drain current increases by the square root of IC, since the gate area decreases inversely with IC. This phenomenon could be attributed to the fact that, in the context of weak inversion, the carrier density is found to be minimal, thereby leading to a diminished observation of the disturbance.

However, in the case of strong inversion, the noise in the drain current is seen to be balanced by the increase in noise in the gate voltage. This is due to the fact that the decrease in G_m with respect to the increase in IC is counterbalanced by the increase in noise in the gate voltage, since the current noise can be expressed as a dependent function of G_m and the noise in the gate voltage.

It is evident that this effect varies according to the geometry of the device. It is evident that as the channel length is reduced, the flicker noise in the drain current increases in proportion, given that the gate area increases in proportion to the square of L. But in the case of the noise expressed in the gate voltage the effect is completely opposite, this is because as more long is the channel the control of the gate voltage in the conduction is less effective.

Following the execution of the requisite simulations, it can be concluded that the model's behaviour aligns with expectations. It is imperative to reiterate that the subject of discussion is a device that adheres to the EKV model, specifically a nanometric MOSFET in a saturation state.

Chapter 6

CONCLUSIONS AND FUTURE WORK

In this study, a Verilog-A model of a MOSFET following the sEKV model has been constructed, thereby describing a nanometric device that functions in saturation state. In order to achieve this objective, a range of challenges have had to be surmounted in order to ensure the functionality of the model, to adapt to variations in the working conditions or to changes in the geometry and temperature of the device itself.

The model has been constructed using expressions that are valid for all the inversion regions, thus creating a continuity that is very useful when obtaining certain magnitudes that derive from others. Notwithstanding this, the model obtained remains uncomplicated and has been designed to incorporate some additional secondary effects, as well as to be adapted for use at cryogenic temperatures.

The results obtained from the model for variations of currents, voltage or change in the value of the inversion coefficient have been checked either with experimental data or with theoretical values obtained in other studies of the sEKV model. Consequently, it can be concluded that the proposed objective has been accomplished, namely the creation of a simple yet versatile model that facilitates the design of more sophisticated analogue circuits. This model is poised to serve as an invaluable instrument for the study of low-power analogue devices.

In this study, the performance of the model operating as an nMOS and also as a pMOS has been verified for different extreme operating temperatures, as well as for a wide range of channel lengths. It should be noted that the model under consideration is an analogue device operating at the nanometric scale. The accurate adaptation of the model to these conditions is facilitated by the scaling of temperature and channel length. This scaling is achieved through the utilization of parameters obtained through experimentation, as well as those derived theoretically in previous studies.

In terms of future related work, further development of the model would be of great interest. In this manner, the sensitivity to second-order defects that have not been considered in this instance could be incorporated, the effect of other capacitances between terminals that are not represented in this model could also be added, or the repercussion of other noises, beyond flicker noise and thermal noise, could be included.

Furthermore, it would be advantageous to adapt the model created to different technologies, such as FDSOI or FinFET. The model created is capable of representing the majority of aspects of these technologies, as it is based on the EKV model. However, it does not accurately model these devices. An illustration of this is the additional back gate of FinFETs, which is not considered in the EKV model.

An alternative approach would be to assess the performance of the model in actual designs and observe its behaviour in such scenarios. These studies would be of great interest given that the model has features created for a particular technology, such as the case of length scaling, whose parameters have been extracted experimentally using a device with a minimum channel length of $130nm$.

Finally, it is important to note that the model outlined in this study holds significant academic value, particularly in the field of MOSFET behaviour analysis, where it can serve as a valuable research instrument. Furthermore, the dissemination of this study through open sources could facilitate feedback on the model and assist in the development of future studies.

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Appendix A

VERILOG-A MOSFET MODEL

```
//*********************************************************************
//*        EKV MOSFET Model. Technical University of Crete.           *
//*                  Alba Gallego Velazquez                           *
//*                        01/07/2025                                 *
//*********************************************************************

`include "disciplines.vams"
`include "constants.vams"

//*******************************************************/
// Electrical

// Current in amperes
nature Current
    units      = "A";
    access     = I;
    idt_nature = Charge;
`ifdef CURRENT_ABSTOL
    abstol     = `CURRENT_ABSTOL;
`else
    abstol     = 1e-12;
`endif
endnature
// Charge in coulombs
nature Charge
    units      = "coul";
    access     = Q;
    ddt_nature = Current;
`ifdef CHARGE_ABSTOL
    abstol     = `CHARGE_ABSTOL;
`else
    abstol     = 1e-14;
`endif
```

```
endnature
// Potential in volts
nature Voltage
    units      = "V";
    access     = V;
    idt_nature = Flux;
‘ifdef VOLTAGE_ABSTOL
    abstol     = ‘VOLTAGE_ABSTOL;
‘else
    abstol     = 1e-6;
‘endif
endnature
// Flux in Webers
nature Flux
    units      = "Wb";
    access     = Phi;
    ddt_nature = Voltage;
‘ifdef FLUX_ABSTOL
    abstol     = ‘FLUX_ABSTOL;
‘else
    abstol     = 1e-9;
‘endif
endnature
// Conservative discipline
discipline electrical
    potential    Voltage;
    flow         Current;
enddiscipline
//*******************************************************/
// Signal flow disciplines

discipline voltage
    potential    Voltage;
enddiscipline
discipline current
    potential    Current;
enddiscipline
```

```
//*******************************************************/
//      Parameters needed from constants.h

`define P_CELSIUS0 273.15
`define NOT_GIVEN -1.0e21

//*******************************************************/
//  OPP      Operating point parameter

`define OPP(name,uni,       descrip) (*units=uni, desc=descrip*)  real name;

module simple_model6(drain, gate, source, bulk);

    //Device => nMOS or pMOS
    inout drain, gate, source, bulk;        //external nodes
    electrical drain, gate, source, bulk;   //external nodes

    //*******************************************************/
    //      Local variables

    real VG, VS, VD, VGD, VGS, VBS;
    real L_VTO_2, VTO_L, L_NO_2, N_L, L_IO_2, IO_L;
    real delta_T, TCV_delta, VTO_T, Vgb_to, Vp, N;
    real NEXO, NO;
    real kT, Tnom, Temp, Ut, Vp_sb, Vx, tox;
    real L_scaled, W_scaled;
    real L_eff, W_eff;
    real NUV;
    real qs, z1, z2, ln_z1_, vv;
    real qs_2, qs_22, IC_num, qs2, qs2_1, qs2_12;
    real LAMBDA_c_2, LAMBDA_qs, LAMBDA_c1, LAMBDA_c1_4;
    real LAMBDA_C;
    real LAMBDA_qs_4, LAMBDA_qs_sqrt, IC_den, IC;
    real CGOX, Cgd, Cgs, cgd, cgs;
    real qogd, qogs;
    real qs_3, qs2_3, qs_1, qs_12, qs2_3_2, L_qs;
    real KP_T, T_Tnom, UO;
    real Ut_2, Ispecsqr, W_L, Ispec, Ids;
```

```
real IC_sqrt_4, IC_sqrt_421, VDSSAT;
real LAMBDA_C_IC, LAMBDA_C_IC_2, sqrt_LAMBDA_IC, sqrt_LAMBDA_IC_1, LAMBDA_C2_IC;
real LAMBDA_C2_IC2, gms, Gms, Gms_Id, GmsUt_Id;
real LAMBDA_D, LAMBDA_D_IC, LAMBDA_D_IC_2, sqrt_LAMBDA_D_IC, sqrt_LAMBDA_D_IC_1;
real LAMBDA_D2_IC, LAMBDA_D2_IC2, gds, Gds, Gds_Id, GdsUt_Id;
real gm, Gm, Gm_Id, GmUt_Id;
real qs08, qS_num, qS_den, qS_2, qS, QS, qd12, qD_num, qD_den, qD_2, qD, QD;
real S_flicker, I_flicker_noise, V_flicker_noise;
real qs_thermal, GAMMA, I_thermal_noise, V_thermal_noise;

//*****************************************************/
//      Parameters definitions

//Basic model parameters
parameter real L = 0.5E-6 from [0.0:inf]; // Channel length [m]
parameter real W = 0.5E-6 from [0.0:inf]; // Channel width [m]
parameter real VTO = 0.5 from [-inf:inf]; // Long-channel threshold voltage [V]
parameter real k =  1.3807E-23; // Boltzmann constant [J/K]
parameter real q =  1.602e-19; // Electron charge [C]
                               // Gate oxide capacitance per unit area [F]
parameter real COX = 10.0E-3 from [0.0:inf];
parameter real KP = 500.0E-6;   // Mobility multiplied with COX [F/Vs]
parameter real EOX = 3.45E-11;  // Oxide permeability   [F/m]
parameter real SCALE = 1.0;
parameter real TYPE = 1.0;  // nMOS = 1.0, pMOS = -1.0

//Length related parameters
parameter real LAMBDA_C0_N = 0.08;  // LAMBDA_CO for nMOS [-]
parameter real LAMBDA_C0_P = 0.15;  // LAMBDA_CO for pMOS [-]
parameter real LSAT_N = 19.9E-9;   // Channel saturation length for nMOS [m]
parameter real LSAT_P = 19.2E-9;   // Channel saturation length for pMOS [m]
parameter real DL = 0.0;     // Difference between effective and drawn gate length [m]
parameter real DW = 0.0;     // Difference between effective and drawn gate width [m]
parameter real XL = 0.0;    // Optical offset for Gate Length [m]
parameter real XW = 0.0;    // Optical offset for Gate Width [m]
    //Parameters for N-Type Length
parameter real VTO_A_N = 0.117;
parameter real VTO_B_N = -0.19;
```

```
parameter real VTO_C_N = 0.069;
parameter real N_A_N = 0.38;
parameter real N_B_N = -2.81;
parameter real N_C_N = 1.225;
parameter real IO_A_N = -0.51E-7;
parameter real IO_B_N = -1.03;
parameter real IO_C_N = 12.7E-7;
parameter real L_VTO_N = 25.0E-6;
parameter real L_NO_N = 7.0E-8;
parameter real L_IO_N = 1.3E-6;
    //Parameters for P-Type Length
parameter real VTO_A_P = 0.06;
parameter real VTO_B_P = -0.405;
parameter real VTO_C_P = 0.339;
parameter real N_A_P = 1.985;
parameter real N_B_P = -2.9;
parameter real N_C_P = 1.2382;
parameter real IO_A_P = -0.31E-7;
parameter real IO_B_P = -1.8525;
parameter real IO_C_P = 2.24E-7;
parameter real L_VTO_P = 10.0E-6;
parameter real L_NO_P = 4.15E-8;
parameter real L_IO_P = 0.187E-6;

//Temperature related parameters
parameter real TEMP = 37.0;  // Device temperature [C]
parameter real TNOM = 25.0; // Nominal temperature [C]
                    // Threshold voltage temperature coefficient [V/K]
parameter real TCV = 1.0E-3;
                    // Long Channel Slope factor with the nominal temperature [-]
parameter real NO_TNOM = 1.0;
                    // Exponential temperature dependence of the slope factor [-]
parameter real NEX = 0.12;
parameter real BEX = -1.5;  // Exponential temperature dependence of KP [-]

//Capacitances related parameters
parameter real LOV = 10.0E-9;   // Length of the overlap area [m]
```

```
//Transconductance related
parameter real SIGMA_D = 0.6;   // Body effect DIBL Coefficient [-]

//Noise related parameters
parameter real AF = 1.0 ;   // Flicker noise exponent [-]
parameter real KF = 1.0E-25;  // Flicker noise coefficient [-]

//*****************************************************/
//      Variables for operating point

`OPP(Id_op,"A"            ,"Drain Current")
`OPP(IC_op," "            ,"Inversion coefficient")
`OPP(Cgs_op,"F"            ,"Gate-source capacitance")
`OPP(Cgd_op,"F"            ,"Gate-drain capacitance")
`OPP(cgs_op," "            ,"Gate-source normalized capacitance")
`OPP(cgd_op," "            ,"Gate-drain normalized capacitance")
`OPP(Gm_op,"A/V"            ,"Gate transconductance")
`OPP(Gms_op,"A/V"            ,"Source transconductance")
`OPP(Gds_op,"A/V"            ,"Output transconductance")
`OPP(gm_op," "            ,"Normalized gate transconductance")
`OPP(gms_op," "            ,"Normalized source transconductance")
`OPP(gds_op," "            ,"Normalized output transconductance")
`OPP(Gm_Id_op,"1/V"            ,"Gate transconductance efficiency")
`OPP(Gms_Id_op,"1/V"            ,"Source transconductance efficiency")
`OPP(Gds_Id_op,"1/V"            ,"Output transconductance efficiency")
`OPP(GmUt_Id_op," "            ,"Normalized gate transconductance efficiency")
`OPP(GmsUt_Id_op," "            ,"Normalized source transconductance efficiency")
`OPP(GdsUt_Id_op," "            ,"Normalized output transconductance efficiency")
`OPP(I_flicker_noise_op,"A^2/Hz","Density of the flicker noise in the drain current")
`OPP(V_flicker_noise_op,"V^2/Hz", "Density of the flicker noise in the gate voltage")
`OPP(I_thermal_noise_op,"A^2/Hz", "Density of the thermal noise in the drain current")
`OPP(V_thermal_noise_op,"V^2/Hz", "Density of the thermal noise in the gate voltage")


analog begin
    //EKV model supposed a saturation situation

    //*****************************************************/
```

```
//  Main voltages

VG = TYPE * V(gate, bulk);    // Gate voltage refered to bulk [V]
VD = TYPE * V(drain, bulk);   // Drain voltage refered to bulk [V]
VS = TYPE * V(source, bulk);  // Source voltage refered to bulk [V]

VBS = -VS;      // Voltage from bulk to source [V]
VGD = VG-VD;    // Voltage from gate to drain [V]
VGS = VG-VS;    // Voltage from gate to source [V]

//*****************************************************/
//  Length scaling

if (TYPE > 0) begin     //nMOS Scaling
    L_VTO_2 = pow((L/L_VTO_N), VTO_B_N);
                            //  Threshold voltage with length scaling [V]
    VTO_L = (VTO_A_N * L_VTO_2) + VTO_C_N;

    L_NO_2 = pow((L/L_NO_N), N_B_N);
    N_L = (N_A_N * L_NO_2) + N_C_N;      //  Slope factor with length scaling [-]

    L_IO_2 = pow((L/L_IO_N), IO_B_N);
                            //  Specific square drain with length scaling [A]
    IO_L = (IO_A_N * L_IO_2) + IO_C_N;

    LAMBDA_C = ( LSAT_N/L ) + LAMBDA_C0_N;   // Length modulation coefficient [-]

end
else begin              //pMOS Scaling
    L_VTO_2 = pow((L/L_VTO_P), VTO_B_P);
                            //  Threshold voltage with length scaling [V]
    VTO_L = (VTO_A_P * L_VTO_2) + VTO_C_P;

    L_NO_2 = pow((L/L_NO_P), N_B_P);
    N_L = (N_A_P * L_NO_2) + N_C_P;      //  Slope factor with length scaling [-]

    L_IO_2 = pow((L/L_IO_P), IO_B_P);
                            //  Specific square drain with length scaling [A]
```

```
    IO_L = (IO_A_P * L_IO_2) + IO_C_P;
    LAMBDA_C = ( LSAT_P/L ) + LAMBDA_C0_P;   // Length modulation coefficient [-]
end

L_scaled = L * SCALE + XL;
W_scaled = W * SCALE + XW;

L_eff = L + DL;     // Effective length of the channel [m]
W_eff = W + DW;     // Effective width of the channel [m]

//*******************************************************/
//  Temperature scaling

Tnom = TNOM + 'P_CELSIUS0;
Temp = TEMP + 'P_CELSIUS0;

kT = k * Temp;
Ut = kT / q;   // Termodinamic voltage [V]

delta_T = Temp - Tnom;
TCV_delta = TCV * delta_T;
VTO_T = VTO_L - TCV_delta;   // Threshold voltage temperature dependent [V]

T_Tnom = Temp / Tnom;
N = N_L * (pow(T_Tnom, NEX));    // Slope factor temperature dependent [-]

NEXO = NEX;
                        // Long Channel Slope Factor Fine Tuning [-]
NO = NO_TNOM * (pow(T_Tnom, NEXO));

KP_T = KP * pow(T_Tnom, BEX);
    // Low field mobility in the channel region temperature dependent [m^2/Vs]
UO = KP_T / COX;
Vgb_to = (VG - VTO_T);
Vp = Vgb_to / N;   // Pinch-off voltage [V]


//*******************************************************/
```

```
//    Normalized source inversion charge: qs [-]
// (Vp - Vsb) / Ut = 2 * qs + ln(qs)

Vp_sb = Vp - VS;
Vx = Vp_sb/Ut;  // Tension for de Lambert function [-]
tox = EOX / COX;    // Thickness of the oxide [1/m]

NUV = NO;

//  Function LambertW

vv = Vx / NUV;
if (vv > -0.6)
begin
    z1   = 0.25 * (vv - 1.4 + sqrt(vv * (vv - 0.394036) + 9.662671));
    ln_z1_   = ln(z1);
    z2   = (vv - (2.0 * z1 + ln_z1_)) / (2.0 * z1 + 1.0);
    qs   = z1 * (1.0 + z2 * (1.0 + 0.070 * z2)) * NUV;
end
else
begin
    ln_z1_   = 0.5 * (vv - 0.201491 - sqrt(vv * (vv + 0.402982) + 2.446562));
    z1   = exp(ln_z1_);
    z2   = (vv - (2.0 * z1 + ln_z1_)) / (2.0 * z1 + 1.0);
    qs   = z1 * (1.0 + z2 * (1.0 + 0.483 * z2)) * NUV;
end

//*****************************************************/
//   Inversion coefficient

qs_2 = qs * qs;
qs_22 = qs_2 + qs;
IC_num = qs_22 * 4;

qs2 = qs * 2;
qs2_1 = qs2 + 1;
qs2_12 = qs2_1 * qs2_1;
LAMBDA_c_2 = LAMBDA_C * LAMBDA_C;
```

```
LAMBDA_qs = LAMBDA_c_2 * qs2_12;
LAMBDA_c1 = LAMBDA_C + 1;
LAMBDA_c1_4 = LAMBDA_c1 * 4;
LAMBDA_qs_4 = LAMBDA_qs + LAMBDA_c1_4;
LAMBDA_qs_sqrt = sqrt(LAMBDA_qs_4);
IC_den = 2 + LAMBDA_C + LAMBDA_qs_sqrt;

IC = IC_num / IC_den;   // Inversion coefficient [-]

//*****************************************************/
//  Capacitances

CGOX = W * L * COX;    // Gate oxide capacitance [F m^2]

Cgd = COX * W * LOV;  // Gate-drain capacitance [F m^2]
cgd = Cgd / CGOX;     // Normalized gate-drain capacitance [-]

qs_3 = qs / 3;
qs2_3 = qs2 + 3;
qs_1 = qs + 1;
qs_12 = qs_1 * qs_1;
qs2_3_2 = qs2_3 / qs_12;
L_qs = L * qs_3 * qs2_3_2;
Cgs = COX * W * ( L_qs + LOV );     // Gate-source capacitance [F m^2]
cgs = Cgs / CGOX;     // Normalized gate-source capacitance [-]

qogd = Cgd * VGD;   // Charge between gate and drain [C]
qogs = Cgs * VGS;   // Charge between gate and source [C]

//*****************************************************/
//  Drain current

Ut_2 = Ut * Ut;
Ispecsqr = 2 * N * UO * COX * Ut_2;     //  Specific current per square [A]

W_L = ( W / L);
Ispec = Ispecsqr * W_L;    //  Specific current [A]
Ids = Ispec * IC;       // Drain current [A]
```

```
//*******************************************************/
//  Charges
//  In saturation qd << qs

qs08 = 0.8 * qs;
qS_num = ((1 + qs08) * qs_2);
qS_den = 2 * qs_12;
qS_2 = qs2 + (qS_num / qS_den);
qS = (N / 3) * qS_2;            //  Normalized intrinsic source charge [-]
QS = CGOX * Ut * qS;            //  Total source charge [C]

qd12 = 1.2 * qs;
qD_num = ((1 + qd12) * qs_2);
qD_den = 2 * qs_12;
qD_2 = qs + (qD_num / qD_den);
qD = (N / 3) * qD_2;            //  Normalized intrinsic drain charge [-]
QD = CGOX * Ut * qD;            //  Total drain charge [C]

//*******************************************************/
//  Velocity saturation voltage

IC_sqrt_4 = sqrt(IC + 0.25);
IC_sqrt_421 = ( IC_sqrt_4 + 0.5 ) + 1;
VDSSAT = 2 * Ut * IC_sqrt_421;      // Velocity saturation voltage [V]

//*******************************************************/
//  Transconductances

LAMBDA_C_IC = (LAMBDA_C * IC) + 1;
LAMBDA_C_IC_2 = LAMBDA_C_IC * LAMBDA_C_IC;
sqrt_LAMBDA_IC = sqrt(LAMBDA_C_IC_2 + (4*IC));
sqrt_LAMBDA_IC_1 = sqrt_LAMBDA_IC - 1;
LAMBDA_C2_IC = LAMBDA_C_IC * LAMBDA_C;
LAMBDA_C2_IC2 = LAMBDA_C2_IC + 2;
                          // Normalized source transconductance [-]
gms = sqrt_LAMBDA_IC_1 / LAMBDA_C2_IC2;
Gms = gms * Ispec / Ut;     // Source transconductance [A/V]
```

```
Gms_Id = Gms / Ids;     // Source transconductance efficiency [1/V]
GmsUt_Id = Gms_Id * Ut;    //  Normalized source transconductance efficiency [-]

LAMBDA_D = LAMBDA_C;
LAMBDA_D_IC = (LAMBDA_D * IC) + 1;
LAMBDA_D_IC_2 = LAMBDA_D_IC * LAMBDA_D_IC;
sqrt_LAMBDA_D_IC = sqrt(LAMBDA_D_IC_2 + (4*IC));
sqrt_LAMBDA_D_IC_1 = sqrt_LAMBDA_D_IC - 1;
LAMBDA_D2_IC = LAMBDA_D_IC * LAMBDA_D;
LAMBDA_D2_IC2 = LAMBDA_D2_IC + 2;
                            // Normalized output conductance [-]
gds = (SIGMA_D / N) * (sqrt_LAMBDA_D_IC_1 / LAMBDA_D2_IC2);
Gds = gds * Ispec / Ut;     // Output conductance [A/V]
Gds_Id = Gds / Ids;     // Output transconductance efficiency [1/V]
GdsUt_Id = Gds_Id * Ut;    // Normalized output transconductance efficiency [-]


gm = gms / N;     // Normalized gate transconductance [-]
Gm = Gms / N;     // Gate transconductance [A/V]
Gm_Id = Gms_Id / N;     // Gate transconductance efficiency [1/V]
GmUt_Id = GmsUt_Id / N;    //  Normalized gate transconductance efficiency [-]

//*******************************************************/
//  Noise effects

//  Flicker noise
S_flicker = (KF * Gm * Gm) / (W * L * CGOX);
    // Power spectral density of the flicker noise in the drain current [A^2/Hz]
I_flicker_noise = flicker_noise(S_flicker, AF, "flicker");
    // Power spectral density of the flicker noise in the gate voltage [V^2/Hz]

V_flicker_noise = I_flicker_noise / (Gm * Gm);
//  Thermal noise
qs_thermal = (qs + (3/4))/(qs + 1);
GAMMA = (2/3) * qs_thermal;    // Thermal noise parameter [-]
    // Power spectral density of the thermal noise in the drain current [A^2/Hz]
I_thermal_noise = 4 * k * Temp * Gms * GAMMA;
    // Power spectral density of the thermal noise in the gate voltage [V^2/Hz]
```

```
V_thermal_noise = I_thermal_noise / (Gm * Gm);

I(drain,source) <+ I_thermal_noise + I_flicker_noise;

//*******************************************************/
//  Operating point values

begin : OPval
   Id_op = Ids;
   IC_op = IC;
   qs_op = qs;
   Cgs_op = Cgs;
   Cgd_op = Cgd;
   cgs_op = cgs;
   cgd_op = cgd;
   Gm_op = Gm;
   Gms_op = Gms;
   Gds_op = Gds;
   gm_op = gm;
   gms_op = gms;
   gds_op = gds;
   Gm_Id_op = Gm_Id;
   Gms_Id_op = Gms_Id;
   Gds_Id_op = Gds_Id;
   GmUt_Id_op = GmUt_Id;
   GmsUt_Id_op = GmsUt_Id;
   GdsUt_Id_op = GdsUt_Id;
   I_flicker_noise_op = I_flicker_noise;
   V_flicker_noise_op = V_flicker_noise;
   I_thermal_noise_op = I_thermal_noise;
   V_thermal_noise_op = V_thermal_noise;
end

//*******************************************************/
//  Transient currents with extrinsic capacitances

I(gate,drain) <+ TYPE * ddt(qogd);
I(gate,source) <+ TYPE * ddt(qogs);
```

```
        I(drain,source) <+  TYPE * Ids;

    end
endmodule
```