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VNiVERSiDAD D SALAMANCA

MASTER'S FINAL THESIS
Master's Degree in Semiconductors
and Electronic Technologies

Design of a testbench for the evaluation of memristors based on organic compounds

Lydia Bush Espinosa
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Supervisor: Salvador Dueñas Carazo
Co-Supervisor: Rodrigo Picos Gayá
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Author: Lydia Bush Espinosa

Department: Electronics Department

Supervisor: Salvador Dueñas Carazo, Electronics Dept.

Co-Supervisor: Rodrigo Picos Gayá

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First, I want to thank my parents, Carmen and Richard, for never letting go of my hand and always giving me the little push one needs when things go off track. Without you, I wouldn't have achieved even half of what I've dreamed of reaching.

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ABSTRACT

This Master's Thesis presents the design and simulation of a fully integrated testbench for the evaluation of memristive devices, with a specific focus on organic memristors. Unlike conventional systems that inject voltage and measure current, this work proposes a novel approach based on current injection and voltage sensing, offering better control over the excitation signal and ensuring compatibility with sensitive, low-voltage devices.

Organic memristors, known for their low-power operation, scalability, and compatibility with flexible electronics, require non-invasive readout techniques due to their sensitivity to electrical stress, as any memristor. The system is divided into three main functional blocks: a programmable current source capable of supplying a wide range of currents; a memristor selector that enables polarity and device control; and a logic block that manages selection signals and test modes.

Designed using 0.18 µm CMOS technology, the circuit allows safe readout through low-voltage, short-duration current pulses. Extensive simulations validate the system's robustness, precision, and adaptability, offering a promising solution for the future integration and characterization of emerging memristive technologies.

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CHAPTER 1

INTRODUCTION

1.1 Overview

This introductory chapter provides the theoretical and conceptual basis required to understand the context and motivations behind the proposed readout system for memristive devices. It begins with a review of memristor theory, covering its modeling approaches, memory-dependent behavior, passivity, and classification. The chapter then shifts focus toward organic memristors, reinforcing their advantages and relevance in actual electronic applications. It also discusses the importance of non-invasive readout techniques, especially in sensitive organic devices.

Finally, it presents an overview of the proposed system architecture, describing briefly its three main functional blocks, followed by a description of the design methodology, the objectives pursued in this work, and a summary of the document structure.

1.2 Introduction to Memristor devices

Classical circuit theory, as is widely recognized, is built upon four electrical variables: voltage (V), current (I), charge (q) and flux linkage (ϕ). These variables allow for six possible pairwise combinations, five of which have been thoroughly studied. Two of them are as given by (1.1) and (1.2), while the other three correspond to the traditional passive circuit elements: the resistor (R), the capacitor (C) and the inductor (L), as shown in (1.3) to (1.5).

$$i(t) = \frac{dq(t)}{dt} \tag{1.1}$$

$$v(t) = \frac{d\phi(t)}{dt} \tag{1.2}$$

$$v(t) = i(t) \cdot R \tag{1.3}$$

$$v(t) = L\frac{di(t)}{dt} \rightarrow \phi(t) = L \cdot i(t) \tag{1.4}$$

$$i(t) = C\frac{dv(t)}{dt} \rightarrow q(t) = C \cdot v(t) \tag{1.5}$$

In 1971, Chua [2] introduced what would later become the fourth missing element in classical circuit theory, which fulfills the last remaining relationship between the charge and the flux-linkage. This two-terminal component is widely known as *Memristor*, short for *Memory Resistor* (M), whose symbol is the one presented in Fig. 1.1. The next subsections will present some properties and features of this element.

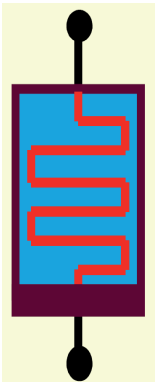

Figure 1.1: Symbol of the memristor proposed by Chua in [3] (Fig. 1)

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1.2.1 Memristor Modeling and Classification

At this point, by definition [2], the memristor can be expressed by a relation between the flux phi and the charge q. There are two equivalent ways to model a memristor, depending on the independent variable used to define the relationship between the charge $q(t)$ and the flux $\phi(t)$. A memristor is said to be **charge-controlled** if that relationship can be expressed as a unique function of the charge, that is, $\phi = \phi(q)$. In this way, the voltage across a charge-controlled memristor is expressed as in (1.6), where the memristance is defined as in (1.7).

$$v(t) = M(q(t)) \cdot i(t) \tag{1.6}$$

$$M(q) = \frac{d\phi(q)}{dq} \tag{1.7}$$

However, if the relationship could be expressed as a unique function of the flux-linkage, $q = q(\phi)$, the device is referred to as a **flux-controlled memristor**. In this case, the current through the device is described by (1.8), where $W(\phi)$ is the memductance (the opposite of the memristance) and is expressed as in (1.9).

$$i(t) = W(\phi(t)) \cdot v(t) \tag{1.8}$$

$$W(\phi) = \frac{dq(\phi)}{d\phi} \tag{1.9}$$

These formulations capture the nonlinear and memory-dependent behavior of memristive systems, but they do not account for internal physical dynamics or parasitic elements. For that reason, more advanced modeling approaches have been proposed.

A comprehensive classification of memristors, introduced by Corinto et al. [4], divides them into three categories based on their complexity and internal dynamics:

-Ideal: is the one defined in 1.6 or 1.8. In this case, there are no internal state variables and no parasitic effects are considered.

-Generic: This approach includes a state vector $\mathbf{z}$ governed by:

$$\dot{z} = f(i, \mathbf{z}) \tag{1.10}$$

$$v = g(i, \mathbf{z}) \tag{1.11}$$

It generalizes the ideal model by introducing internal dynamics, yet still neglecting high-order parasitic effects. This class is usually used to model analog nonvolatile memory behavior.

-Extended: is the most complete class. It includes parasitic inductive or capacitive effects, and its behavior is described by an implicit relation:

$$h(q, \phi, \mathbf{z}) = 0 \tag{1.12}$$

$$\dot{z} = f(u, \mathbf{z}) \tag{1.13}$$

where $u(t)$ is the excitation signal (current or voltage). These models are suitable for accurately capturing complex dependencies that arise from materials, geometry, or physical limitations.

This classification helps to determine the most appropriate model depending on the application and the level of detail required. While ideal models are useful for theoretical analysis, practical implementations—especially in the context of organic or hybrid materials—often require generic or extended formulations to capture the full behavior of the device.

1.2.2 History-dependent

One of the most fundamental features of memristive systems is their dependence on the past evolution of the input signals—an inherent memory effect that stems directly from their mathematical formulation.

As described in the previous section, both ideal and non-ideal memristor models involve internal state variables whose dynamics are governed by differential equations. In the simplest case, the state depends on either the time integral of the current (i.e., the total charge) or the voltage (i.e., the total flux linkage). Specifically:

$$q(t_0) = \int_{-\infty}^{t_0} i(\tau)\, d\tau \tag{1.14}$$

$$\phi(t_0) = \int_{-\infty}^{t_0} v(\tau)\, d\tau \tag{1.15}$$

These expressions indicate that the state of the device at time t_0 is determined by the accumulated excitation—not by the instantaneous value of voltage or current. As a result,

the device "remembers" its excitation history, and its resistance (or memristance) evolves accordingly.

This memory-dependent nature is what gives the memristor its name: memory resistor. It also explains its unique behavior in circuits, where the current-voltage relationship reflects not only present inputs but the complete trajectory followed by the system over time. This property is crucial for applications such as synaptic emulation, learning systems, and non-volatile memory storage.

In more complex models—such as generic and extended memristors—the dependence on history is captured through differential equations of the form:

$$\dot{z} = f(u, \mathbf{z}) \tag{1.16}$$

where z represents the internal state and $u(t)$ the input signal. These models allow the system to exhibit a wide range of memory-related phenomena, such as hysteresis, adaptation, and time-dependent plasticity.

Understanding this behavior is essential when designing readout and excitation circuits, especially for organic memristors, which tend to be more sensitive to cumulative electrical stress.

1.2.3 Passivity

As just said, the memristor is a passive element, said to be such only if its incremental memristance is nonnegative [2]:

$$M(q) \geq 0 \tag{1.17}$$

This condition ensures that the instantaneous power dissipated by the memristor is also always nonnegative:

$$p(t) = i(t) \cdot v(t) \tag{1.18}$$

$$p(t) = i^2(t) \cdot M(q(t)) \geq 0 \tag{1.19}$$

Therefore, a passive memristor will never be able to deliver power to the circuit but only store or dissipate it, remaining consistent with energy-conservation passive systems.

1.2.4 Fingerprint

As defined in [3], one of the most distinctive features of memristors is their characteristic current-voltage (I-V) behavior under periodic excitation of zero mean, commonly known as their "fingerprint". This characteristic manifests itself as a pinched hysteresis loop that always passes through the origin of the I-V plane. The shape of the loop varies depending on the amplitude and frequency of the input signal, as shown in Fig. 1.2, while the pinched behavior remains even for more general bipolar periodic excitations. This property is considered the main rule to classify an element as a memristor.

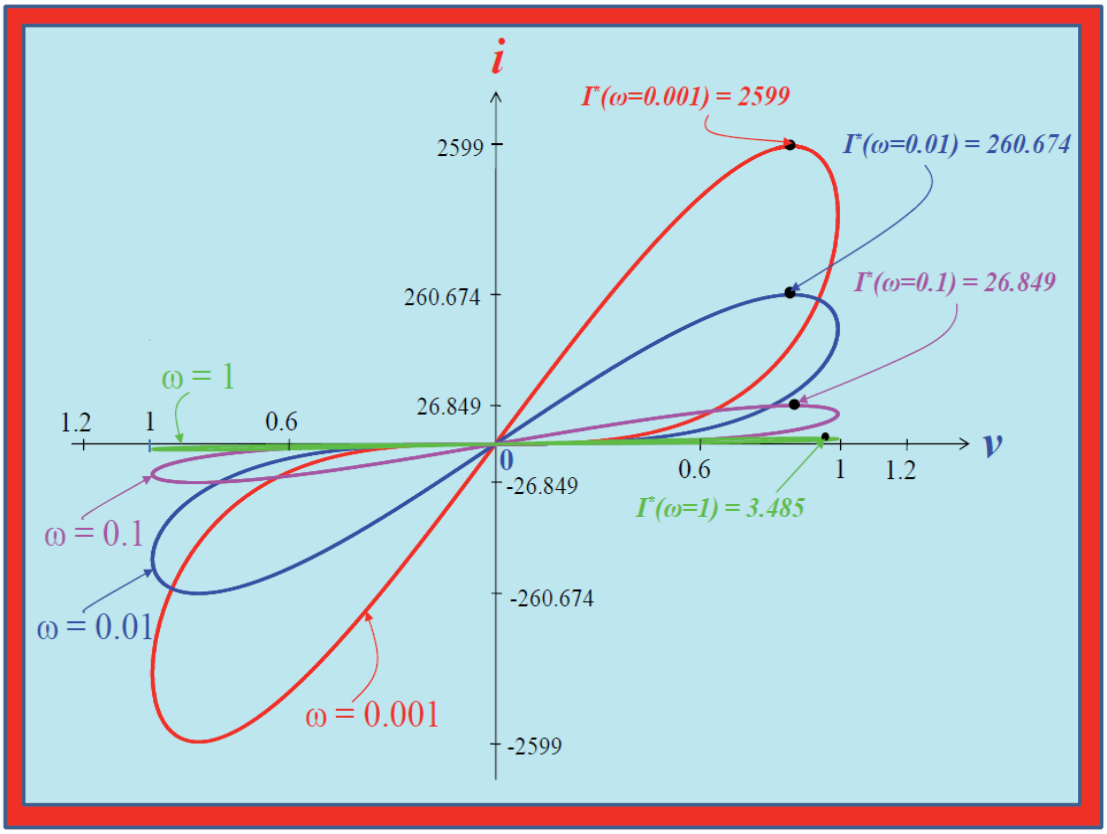

Figure 1.2: Pinched hysteresis loops from a memristor defined in [3] (Fig. 34), with $v = A \cdot sin(\omega t)$, $A = 1$, $x(0) = 1$, for $\omega = 1$, 0.1, 0.01, and 0.001, respectively.

1.3 Organic Memristive Devices

This master thesis focuses on the design of a redout system for memristive devices, especifically with a forward vision to organic memristor implementation. Although this work does not involve the direct deposit or characterization of these devices, the system has been constructed with the functional requirements needed for their future integration.

Organic memristors are devices that have attracted significant attention due to their low power consumption, simple two-terminal structure, easy fabrication, and compatibility with printed and flexible electronics [6]. Such features place them at the forefront of next-generation electronics, specifically in fields such as wearable devices, smart textiles, flexible sensors, and neuromorphic computing systems [9] [11].

One of the most attractive properties of organic memristors is their potential for scalable and eco-friendly fabrication. Unlike traditional memory technologies, which usually require high-temperature and vacuum processes, organic memristors can be produced in standard environments using techniques such as inkjet printing, spin coating, or screen printing. This opens the door to low-cost, high-volume production, and integration into unconventional substrates.

Moreover, their fast switching speeds, high endurance, and excellent scalability make them suitable for actual computing paradigms such as in-memory computing and neuromorphic computing, studied in depth in [5]. Their electrtical behavior (showing stability switching

between high- and low-resistance states) makes them perfect candidates to emulate biological synapses in artificial neural networks [11], with applications starting from real-time data processing ending in energy-efficient AI systems. Nonetheless, organic memristors exhibit a certain degree of volatility, which makes them a point of concern when considering their use in memory applications, where special care must be taken to ensure reliable performance [7] [10] [1].

Although the present work does not include their detailed study, as research in this field continues to advance rapidly, organic memristors are expected to play a key role in shaping the future of flexible, efficient, and intelligent electronics, a reason enough to take them into account in this circuit and system design.

1.4 Non-Invasive Readout of Memristors

Memristors' characteristics have demostrated that they result to be a versatile and promising candidates for many applications. However, due to their intrinsic physic features, they result to be sensitive to electrical stimuli, making it crucial to develop readout methods that preserve their internal state. A well-established and effective technique is the application of short, low-amplitude voltage pulses, during which the current is measured to infer the resistance. This readout method becomes specifically critical in organic memristors, which are more sensitive to thermal and electrical stress.

Underlying Physical Mechanisms

Switching in organic memristors typically occurs via:

- **Filamentary mechanisms:** such as Ag^+ migration and reduction, creating conductive paths
- **Charge trapping/detrapping:** in nanocomposites or nanoparticle-doped films

Both are highly nonlinear and field-dependent processes. By operating well below these thresholds and limiting the energy delivered, the read operation can sample the device's state without inducing state change.

Principle of operation

The concept behind short-pulse readout is to apply a voltage pulse that is well below the threshold, both in amplitude and in duration, to switch the state of the memristsor. The resulting current is used to calculate the device's resistance using Ohm's law. The objective is to remain within the non-disturbing regime, where the physical configuration responsible for the memristance remains stable. Typical parameters include:

- **Pulse amplitude**: 0.1 V to 0.5 V
- **Pulse duration**: 1-10 μs
- **Rise/fall time**: tens to hundreds of nanoseconds

This methodology was successfully demonstrated in [12] by Yakopcic, who concluded that memristors can be read safely and repeatedly using short-duration pulses under threshold

voltages without altering the device state. This is especially relevant when using them in neuromporphic or analog computing systems, where endurance and precision are critical. A simple experiment about the short-pulse reading is shown in Fig. 1.3.

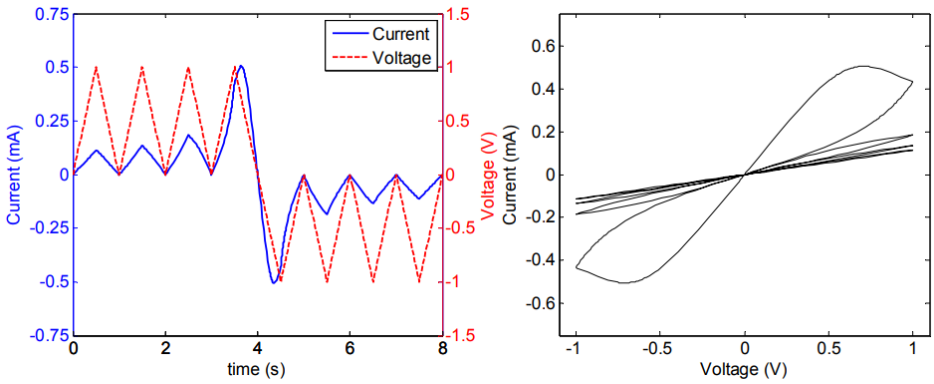

Figure 1.3: Simulated I-V characteristic using a memristor model from [8] where the plots show the voltage and current input (left), and the corresponding I-V characteristic of the memristor (right). (Fig. 2.1 in [12]). Negligible change can be observed when short pulse is applied, while a change in resistance is induced with a higher pulse (from 0.5 V to -0.5 V).

Organic Memristors: Thresholds and Sensitivity

According to [7], organic and hybrid organic-inorganic memristors show remarkable performance metrics such as:

- **Switching speeds** below 15 ns
- **Retention** >10^6 seconds
- **Endurance** >10^{12} cycles
- **Low SET voltages** ranging from 0.18 V to ~2.8 V
- **ON/OFF resistance** ratios exceeding 10^5

Such low-voltage operation reinforces the importance of careful pulse shaping for non-invasive readout. For example, in an Al/polymer/Au device with Au nanoparticles embedded in the polymer matrix, switching occurs at ± 2.8 V and -1.8 V. However, a stable readout was performed with +0.5 V pulses, which did not affect the resistance state of the device. These characteristics make organic memristors ideal for flexible electronics, but they also demand precise control over readout parameters.

1.5 Proposed System

The system schematic is shown in Fig 1.4. The technology used for this design is 0.18 μm MOS technology. The minimum channel length (L) has been set to 0.6 μm, while the channel width (W) may vary depending on the user's preference, as long as the aspect ratios presented in the schematic design sections are respected.

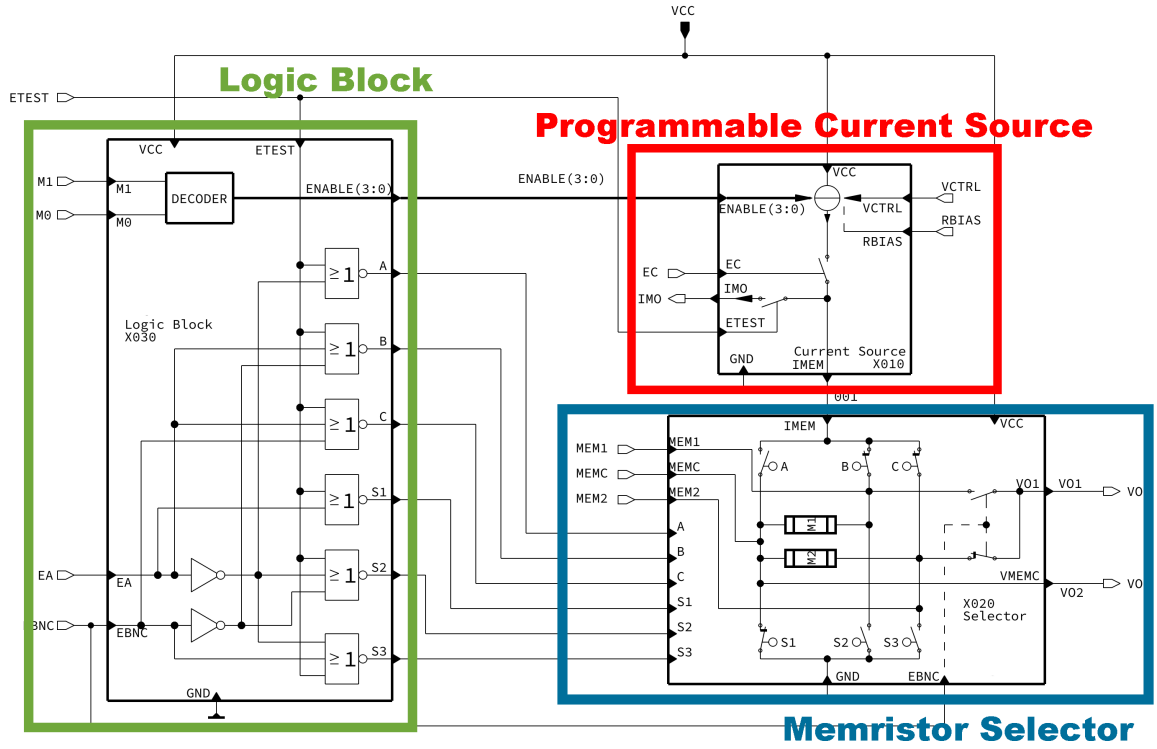

Figure 1.4: Full System Schematic

The main purpose of the circuit is to measure the voltage across the organic memristors when they are excited with different types of current. To do so, the system is divided into three main blocks:

- **Programmable Current Source**
- **Memristor Selector**
- **Logic Block**

Following that, each functional block will be explained next, without going into the schematic definitions, which will be described in their respective chapters.

1.5.1 Programmable Current Source

This first block, in general terms, is responsible for supplying current to the memristors. It could be considered the main block of the system, and its design has been the most laborious, as it requires the highest level of funcionality and precision.

The intrinsic physics of the memristors required the ability to operate with precision in current levels ranging from nanoamperes (nA) to milliamperes (mA), which is quite a wide range for current sources. The operation is based on the injection of a control voltage (between 0V and 1V) that regulates the amount of current supplied to the memristors. The design was intended to be as robust as possible against voltage variations, while also ensuring consistent performance under AC and even high-frequency pulsed control signals, not just DC. The full architecture and functionality will be studied in more depth in Chapter 2.

1.5.2 Memristor Selector

Once the injection current is obtained, it must flow through the memristors in such a way that they generate a voltage drop that can later be read. The memristors will be found in this block, but the main reason for creating a separate block for this is to enable two key features: on the one hand, having two deposited memristors and being able to select which one receives the injected current; and on the other hand, being able to control the direction in which the current flows through them. This latter capability is crucial, since memristors are highly sensitive to the polarity of the current that crosses them. In fact, it is the direction of the current that determines whether their resistance increases or decreases.

To achieve this features, multiple switches are used to connect or disconnect either side of the memristor to the ground or to the injection node, as well as to select which memristor is active. The decision of which switches to activate/deactivate is the responsibility of the next and final block. For a more in-depth explanation of the block's design and operation, refer to Chapter 3.

1.5.3 Logic Block

As introduced in the previous subsection, this block contains the logic responsible for determining which switches will be activated or deactivated in each case. To fully understand its operation and the logic used, Chapter 4 should be consulted. However, in general terms, it consists of two inputs: one that selects which memristor is being tested and another that determines its polarity.

Nevertheless, although the previous is the main function of this block, there is another duty that required logic design, which has been implemented here as well: the current mirror decoder. To enable the possibility of having enough resolution either in the nanoamperes range and the milliamperes range, four different current mirrors have been designed. Each will offer stability and robustness for each range and will be selected externally using two bits. The decoder receives the binary input corresponding to the desired current mirror and enables it, providing the appropriate current output.

1.6 Design Flow

As described in Fig. 1.5, the system design has gone through a series of development stages. In any basic circuit design, the process begins with a set of specifications and fundamental system requirements. In this case, the goal was to develop a system capable of current injection and voltage measurement. The system was designed to operate with a supply voltage between 0 and 5 V (standard values), which indicated that, for the time being, ultralow-power (ULP) technology (typically limited to voltages below 3.3 V) was not a requirement. Nevertheless, minimizing power consumption is always a key objective in circuit design.

In more technical specifications, the system was required to deliver currents ranging from 0 to 3 mA while maintaining stability across an output voltage range of at least 0 to 2 V. This led to a focus on designing the first block: the current source. The design began with basic current mirror topologies, which were simulated under various conditions (supply variations, voltage fluctuations at the output node, temperature changes, etc.) and gradually refined until the final architecture was achieved. Initially, the bias signal was still implemented as a current input, without yet introducing the control voltage.

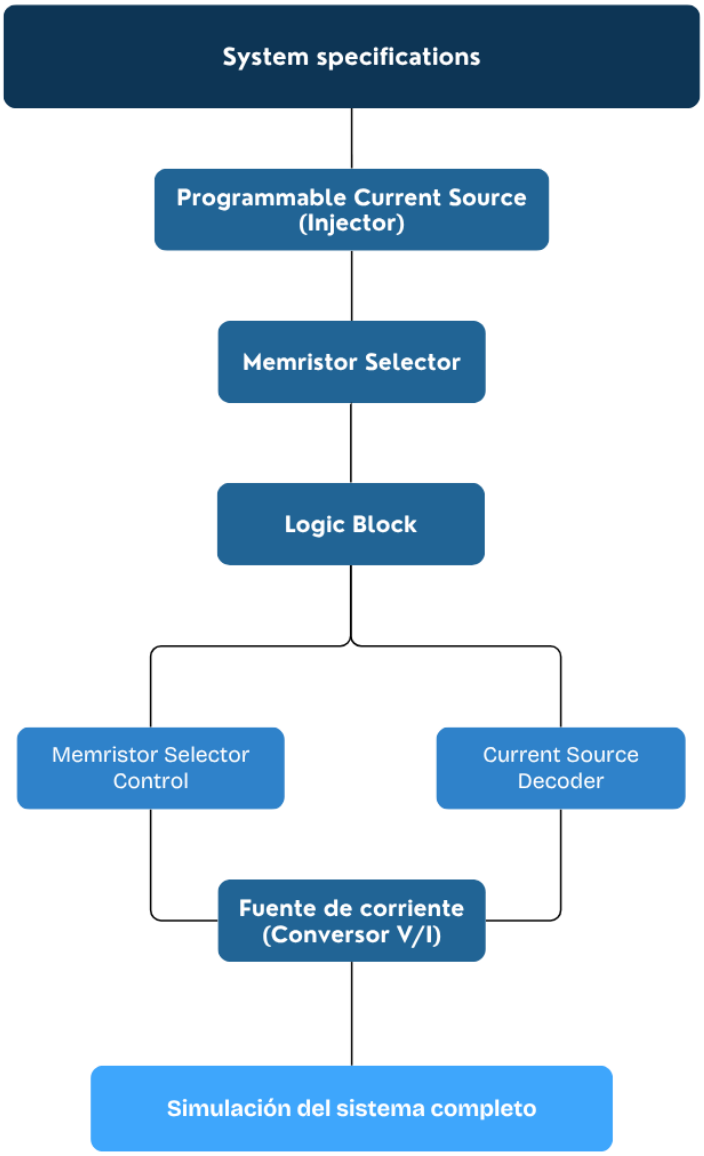

Figure 1.5: Design Flow Schema followed during the study

Once the current injector was mostly designed, the next step was the memristor selector. The goal was to enable the selection between two memristors and to reverse the polarity of the current through them, as explained in the previous section. It was important that the switching transistors could withstand the maximum current the system could provide (in this case, 3 mA). Although this led to oversizing when handling very low currents (around 100 nA), the solution to that would involve designing four separate memristor switches adapted to each current range. However, that approach would have required an even greater sacrifice of chip area, which ultimately led to the core design idea—one that also ensured reliable functionality under all operating conditions. The design of this block was relatively straightforward, allowing

for a quick transition to the final block.

In the logic block, it was necessary to account for all desired and undesired configurations, which led to the creation of a truth table covering all possible cases. This block includes six outputs (connected to the six inputs of the memristor switcher) for controlling the switchers, and an additional 4-bit output for the current source encoder. Three inputs were used to determine the switching logic: one for selecting the TEST mode (explained in Chapter 2), and the other two for selecting the memristor and its polarity. From these, logical expressions for the outputs were derived, prioritizing the use of NOR gates over AND gates to save space in the further layout, resulting in the required logic for correct circuit operation.

Once this point was reached, and before simulating the full system, the V/I converter of the Current source was designed. The objective was to excite the circuit between 0 and 1 V providing the maximum possible current, which would then be appropriately distributed among all current mirrors, while always aiming to balance the trade-offs between area and performance.

With these elements completed, the full design of the system was finalized. Simulations of the entire system were performed and presented in the respective chapters.

1.7 Objectives

The main objectives of this Master's Thesis are as follows:

- Gain experience in the analog design of readout systems for memristive devices, with a focus on organic memristors, while ensuring adaptability to other memristor technologies.
- Understand non-invasive measurement techniques for memristors, aiming to characterize their resistive state without altering it.
- Become familiar with the flow of analog circuit design, identify critical stages in the process, recognize key performance parameters, and learn when trade-offs are necessary between metrics such as precision, power, and area.
- Achieve a qualitative and quantitative understanding of each designed circuit block, including the rationale that began the architectural and technological choices made throughout the design process.
- Contribute to the exploration of readout techniques based on current injection and voltage sensing, as opposed to the conventional voltage injection/current sensing approach predominant in the current literature.
- Design a system architecture that enables direct deposition of memristors onto the readout circuitry, aiming at a fully integrated solution that can be readily used in practical applications and future developments.
- Ensure robustness and precision in the readout system without compromising power efficiency, making the circuit suitable for embedded and low-power applications.

1.8 Structure of the Work

The following chapters will provide a detailed description and in-depth development of the three main functional blocks. Each of these chapters will be structured into three main sections:

- The **first section** will define the specifications and requirements of the block.
- The **second section** will focus on the schematic design and the rationale behind the key design decisions.
- The **third section** will present the set of simulations considered necessary to verify the correct operation of each block (in Chapter 4 this section was not considered necessary).

The work will conclude with a final chapter summarizing the general conclusions and main takeaways derived from the study.

CHAPTER 2

PROGRAMMABLE CURRENT SOURCE

2.1 Overview

This chapter focuses on the schematic-level design and simulation of the programmable current source. The implementation is based on a modular architecture composed of a Voltage-to-Current (V/I) converter followed by multiple current mirror stages. Each sub-block was designed with simplicity, scalability, and functionality in mind, and is tailored to operate within different current ranges. The schematic is discussed in detail, including the internal operational amplifier structure, biasing strategy, and feedback mechanisms used to stabilize and control the generated current.

In addition, the chapter presents the simulation setup and results used to validate the performance of the system. Simulations include DC sweeps, transient analysis, and corner cases across a range of temperatures and supply voltages. Key performance metrics such as output current linearity, stability, voltage headroom, and mirror accuracy are analyzed and compared against design specifications.

Through this schematic and simulation-driven approach, the current source is shown to meet the intended precision and robustness requirements for practical use in test environments, including TEST mode functionality for external calibration and debugging.

2.2 Specifications

2.2.1 Design criteria

The objective of this block, highlighted in Fig. (2.1), is to inject current into the memristors, as described in Chapter 1. The main specifications include:

- Current injection from 0 to 3 mA.
- Capability to provide accurate current delivery across a wide range (from nA to mA).
- Robustness against voltage variations from 0 to, at least, 2 V.

but these are not the only purposes.

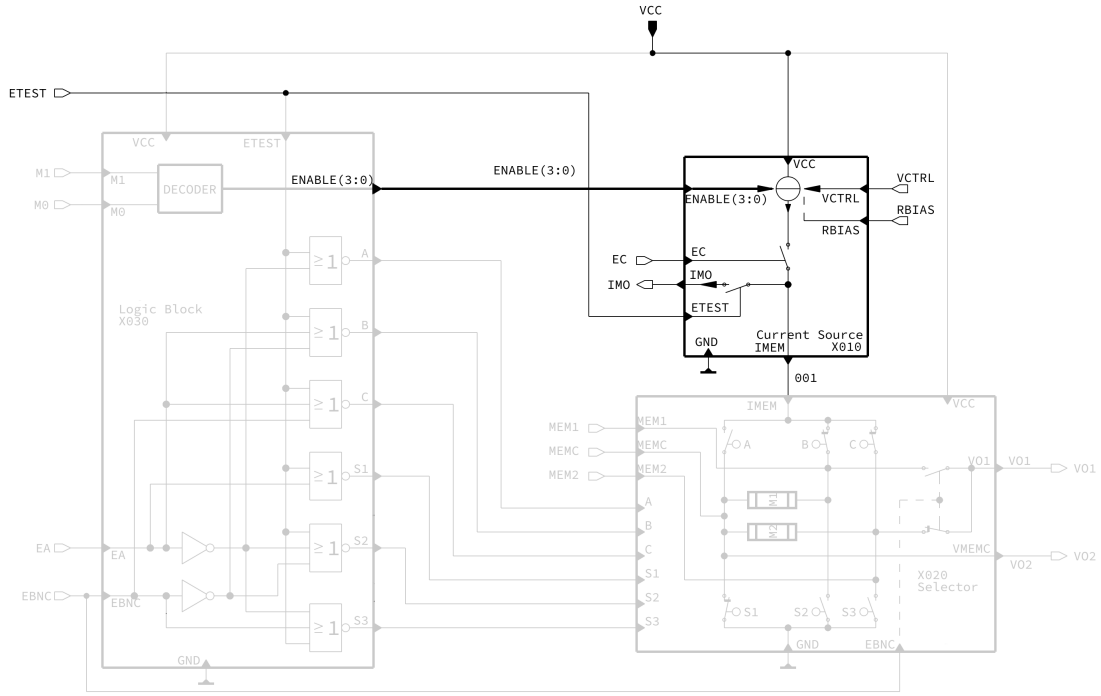

Figure 2.1: Programmable Current Source symbol in the full system schematic.

To start, in analog design, minimizing power consumption is always a desirable goal, even if it is not the primary objective in this case. Therefore, a standard supply voltage range (0 V to 5 V) has been chosen, with a focus on optimizing the trade-off between area and performance as much as possible.

Additionaly, multiple simulations have been carried out under various temperature conditions. The aim is to ensure that the system is as robust as possible against non-standard environmental scenarios, although this criterion is not considered the highest priority.

That said, the most critical requirement was to achieve a precise and robust system in the presence of voltage variations at the output node of the block, as this is where the memristors will be connected to receive the supplied current. The target memristors operate approximately within a 0 to 2 V range when a current between 0 and 3 mA is applied. Therefore, this voltage headroom has been used as the design reference.

The block has been specifically designed for this application, although it may also be suitable for other similar use cases. However, more advanced applications would require more sophisticated and accurate designs. The current source developed includes laboratory-level mechanisms, with the objective of testing its functionality and allowing future iterations and improvements over time.

2.2.2 Why a Current Source

One of the key value propositions of this system lies in the type of measurement employed. In the current literature, the vast majority of memristor charaterization systems rely on voltage-driven schemes to observe the current response. After reviewing and analyzing several papers

and technical articles, it was concluded that incorporating current injection systems could add significant value to the project. As a result, this approach was adopted.

Consequently, the memrisotr required a current injector - specifically, a P-type injector - that would be both robust and versatile. This block turned out to be the most complex component and the one that required the most development time, as it represents the core innovation of the project -alongside the inspiration drawn from organic memristors. The aim was to evaluate the memristor's behavior under continuous, alternating, and pulsed signals with a wide range of amplitudes. Therefore, special emphasis was placed on covering all possible use-cause scenarios a user might encounter. In fact, the design also includes the ability to directly measure the current prior to injection, as long as the system is operating in TEST mode.

TEST MODE

This mode was developed with the purpose of enabling external verification of the generated current, allowing for direct measurement of the actual values delivered by the circuit. This helps ensure more accurate and realistic results during subsequent memristor characterization.
Although the ultimate goal would be to automate the control of this mode via a DLP or a similar platform, it is sufficient to activate it manually by applying 5 V to its dedicated pin.

2.3 Schematic Design

The schematic design of the Programmable Current Source is presented in Fig. (2.2), while the pinout of the block is described in Table 2.1.

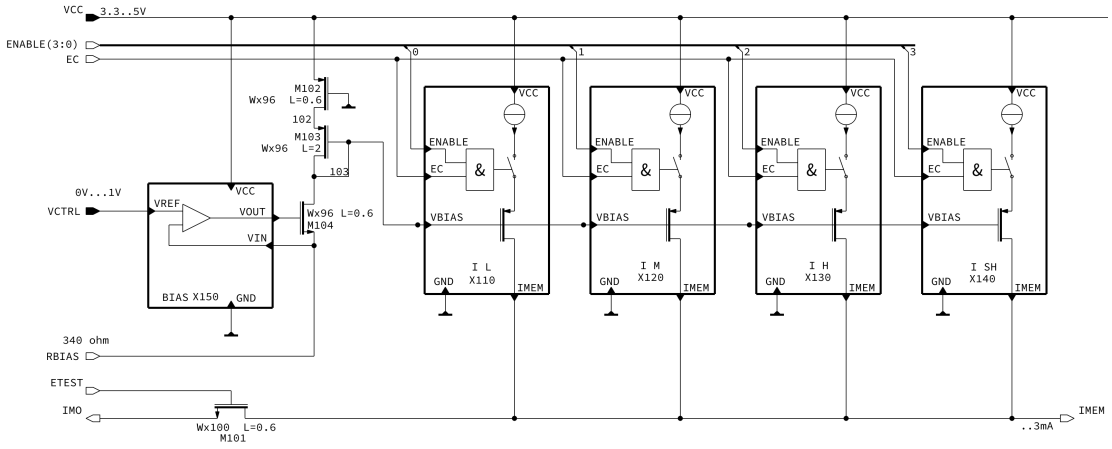

Figure 2.2: Schematic design of the Programmable Current Source

The current generation system is divided into two types of sub-blocks, whose symbols are shown in Fig. (2.3) and Fig. (2.4). The generated current will flow through the memristors (in the IMEM node) or be routed externally (via the IMO node), depending on whether the system is operating in TEST mode or not, by switching the state of the M101 transistor in Fig. 2.2.

Pin	I/O	Funcionality
VCTRL	Input	Control voltage input
VCC	Input	Power Supply Voltage
GND	Input/Output	Ground
EC	Input	Current activation signal
ETEST	Input	TEST mode activation signal
RBIAS	Input/Output	Bias resistor
IMEM	Output	Output current to memristor
IMO	Output	Output current when TEST mode is enabled

Table 2.1: Programmable Current source pinout description

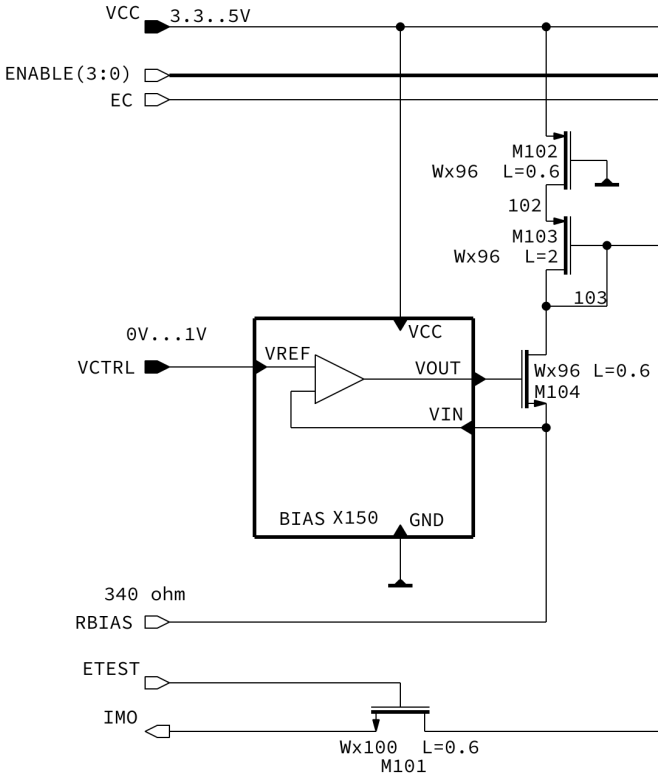

Figure 2.3: Symbol of the V/I Converter in the Programmable Current Source schematic.

2.3.1 Voltage-to-Current Converter (V/I Converter)

This sub-block, as its name suggests, is responsible for converting the main input of the circuit—the control voltage—into a reference current, which will serve as the master current for the subsequent current mirror stages.

A simple operational amplifier-based topology was chosen for this block, as shown in Fig. (2.5). In the OPAMP, the bias current is generated through the resistor R1A0, and then mirrored to the bias transistor M1A5 via transistor M1A0. Then, a simple P-type differential pair (M1A3–M1A6) is used, with active N-type load transistors (M1A4–M1A7). The currents from the differential branches are mirrored to the output transistors (M1A8–M1A9), which

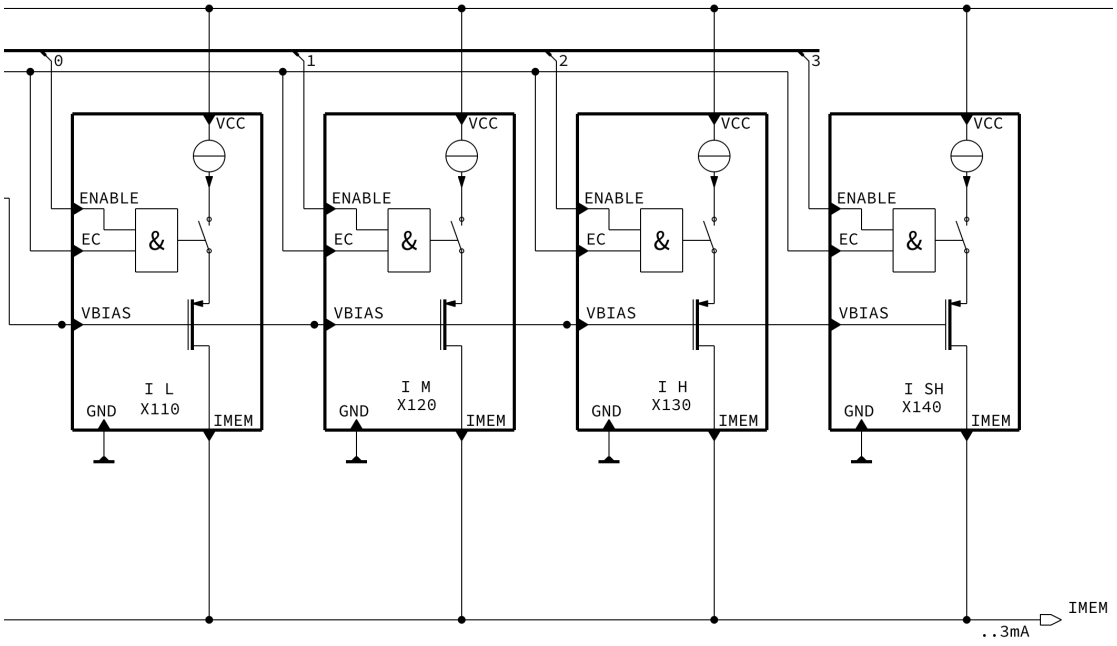

Figure 2.4: Symbols of the Current Mirrors in the Programmable Current Source schematic.

adjust the voltage at the capacitive output node (VOUT).

As illustrated in Fig. (2.3), the output of the operational amplifier is connected to the gate of an N-type transistor (M104), while its source is fed back to the amplifier's input to establish a negative feedback loop. The use of feedback ensures that the transistor M104 operates in saturation, allowing precise current regulation. The voltage in the RBIAS pin is directed to a bias resistor, which will induce a current by Ohm's law. Recommended bias resistor values for each current mirror and their corresponding current ranges are presented in Table 2.2.

This current then flows through a P-type transistor (M103), which has a longer channel length to improve the matching performance with the posterior mirrored branches. Finally, transistor M102 is included as a dummy device to compensate for threshold voltage shifts introduced by the switching mechanisms in that current mirror stages. This helps maintain balance and accuracy across the mirrored outputs.

A summary of the sub-block elements and their functionality is presented in Table 2.3.

Design decisions

- A P-type differential input stage was selected to operate effectively within an input voltage range of 0 V to 1 V. This configuration increases the voltage headroom of the circuit, making it more suitable for low-voltage applications.
- Although the use of R1A0 for master current generation is not the most sophisticated technique, it offers sufficient stability within the operating range required by this circuit.

Design decisions

- To minimize matching loss during voltage-to-current conversion, long-channel transistors have been used - specifically, L = 5.
- The number of transistors in parallel (which defines the total W) has been sized to ensure optimal current ratios. This allows the OPAMP, once configured in a feedback loop and biased at its operating point, to generate an output voltage that is low enough to avoid saturating the transistors in the subsequent stage (M102-M103) and high enough to ensure proper conduction of the feedback transistor (M104).

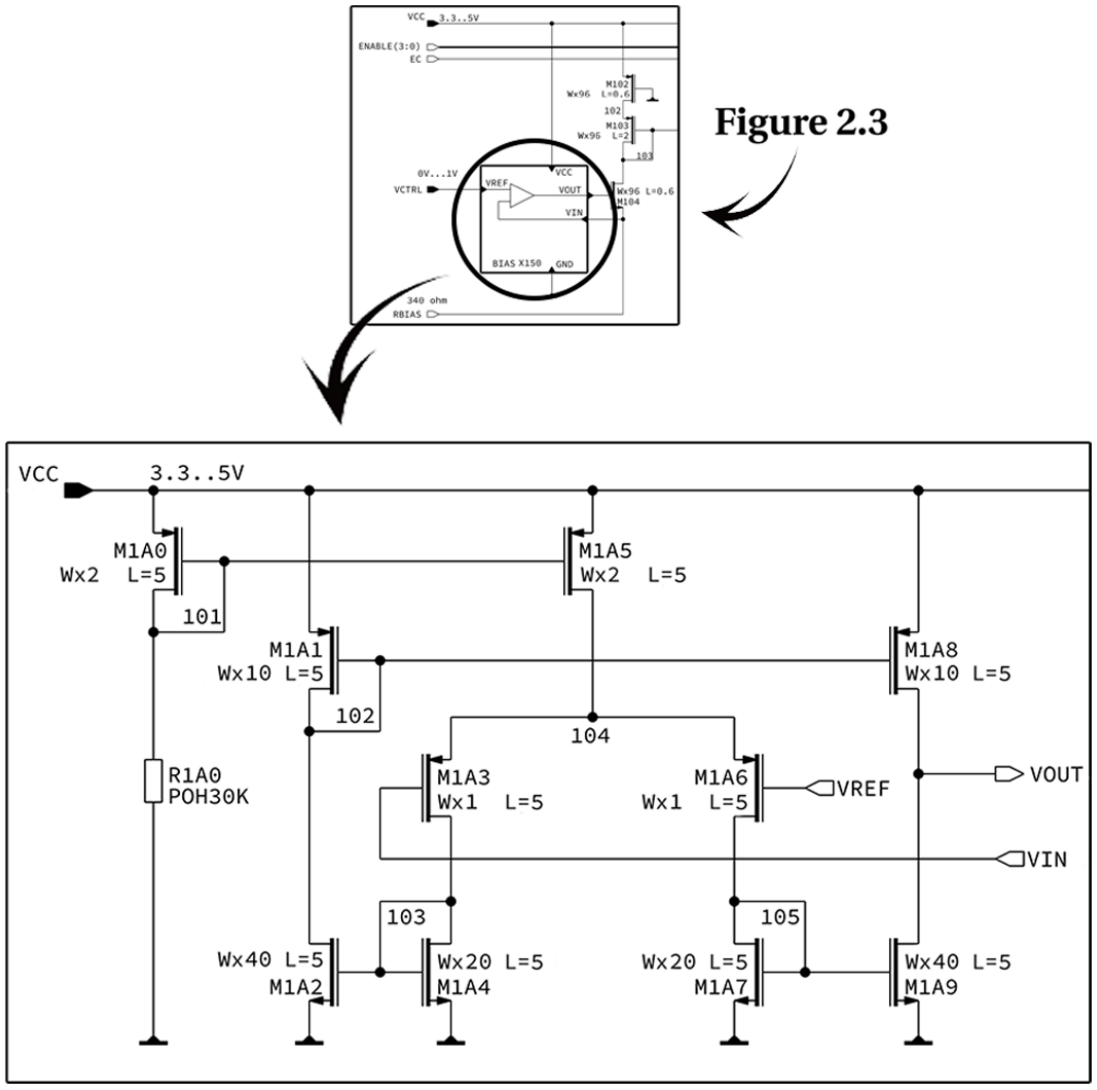

Figure 2.5: Schematic of the OPAMP of the V/I converter.

Current Mirror	Current Range (A)	Bias Resistor (Ω)
E0	17.4 n – 445 n	340 k
E1	314 n – 7.26 µ	34 k
E2	5.92 µ – 146 µ	3.4 k
E3	112 µ – 2.84 m	340

Table 2.2: Recommended bias resistor values for different current mirror configurations and the corresponding current range offered by them.

Component	Funcionality
M102	Dummy transistor
M103	Master current transistor
M104	Feedback lineal-ensurer transistor
RBIAS	Master current-biasing resistor
M1A0	Master current transistor (of the OPAMP)
M1A1	Mirroring transistor (of the OPAMP)
M1A2	Mirroring transistor (of the OPAMP)
M1A3	Differential pair transistor (-)
M1A4	Active charge (of the OPAMP)
M1A5	Master current mirroring transistor (of the OPAMP)
M1A6	Differential pair transistor (+)
M1A7	Active charge (of the OPAMP)
M1A8	Second Stage transistor (of the OPAMP)
M1A9	Second Stage transistor (of the OPAMP)
R1A0	Master current-biasing resistor (of the OPAMP)

Table 2.3: Name and funcionality of the components of the V/I converter sub-block in the Programmable Current Source block.

2.3.2 Current Mirror

The second sub-block used in the design is the current generator. This sub-block has been replicated four times, each instance with different sizes, as shown in Fig. 2.6. Each of them is activated by a corresponding bit of the ENABLE signal, which provides the system with its programmability feature.

The current generated in the previous sub-block is mirrored into each of these sub-blocks via the VBIAS input. The current mirror circuit aims to drive the appropriate current to the IMEM node, according to the aspect ratio between the master transistor from the V/I converter and the transistors in the IMEM output branch.

All the circuits belong to the same type of sub-block but differ in transistor sizing. Therefore, the explanation will be based on the circuit shown in Fig. 2.6, which corresponds to Mirror 1, activated by the ENABLE(1) bit. To ensure optimal operation, transistor M1A7 mirrors the current of the output transistor M1A8. Meanwhile, the M1A4–M1A5–M1A3–M1A2–M1A1 branch forms a cascode structure, which defines the voltage swing and enhances the stability of the output transistor.

In addition, a logic gate has been included to control whether the current path is enabled. The current is allowed to flow only when the corresponding ENABLE bit is set and the excitation input EC is active. To ensure proper matching, the threshold voltages accumulated from the power supply to transistor M1A2 must be identical to those from the power supply to transistor M1A8. The M1A0 transistor is included as a dummy device to preserve this matching accuracy, compensating for the presence of the additional switching transistor introduced by the logic gate.

A summary of the sub-block elements and their functionality is presented in Table 2.4.

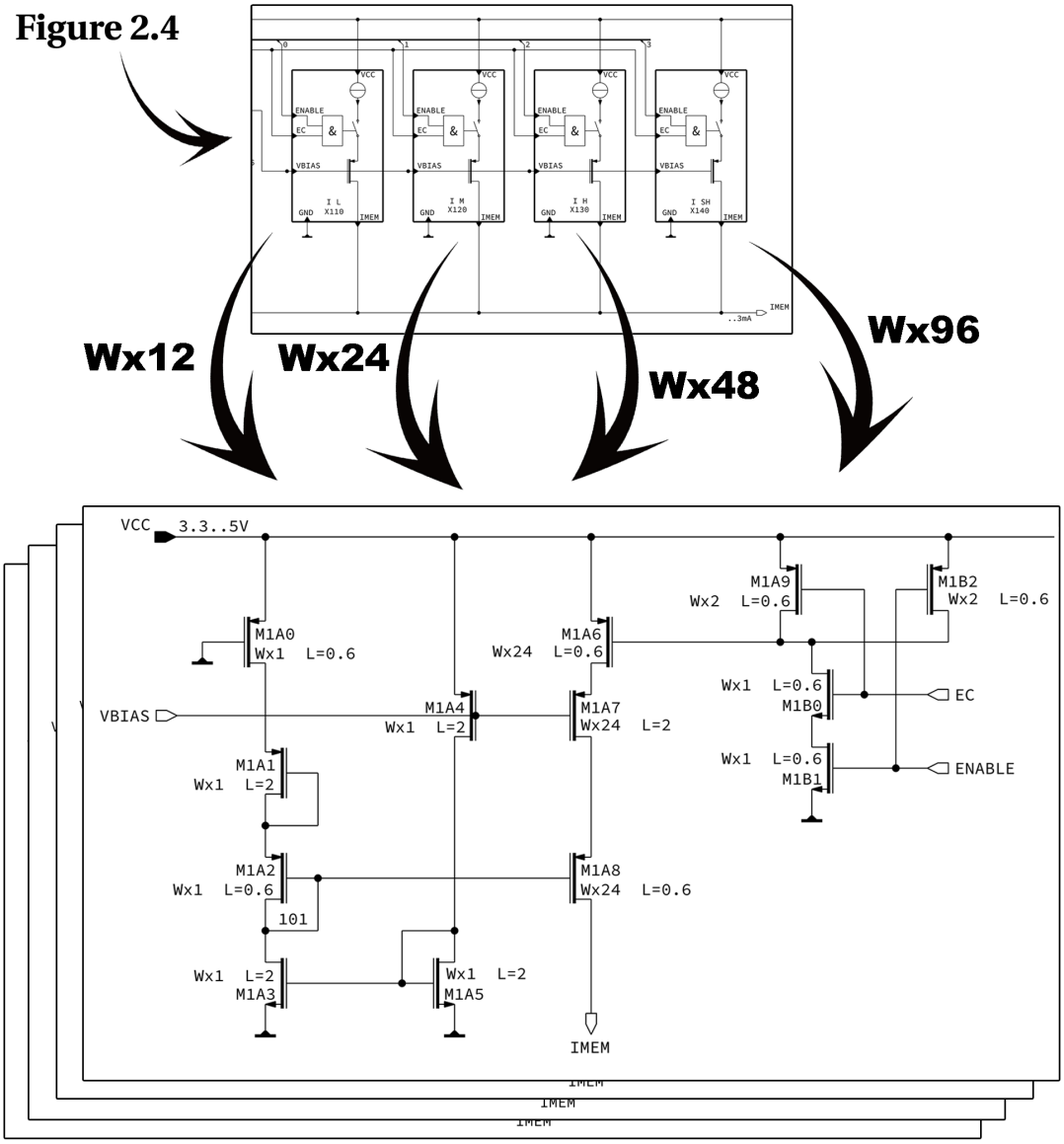

Figure 2.6: Current Mirror schematic. The schematic is presented for the third current mirror (where the current is 96:24). Each schematic is the same but the relations in M1A6, M1A7 and M1A8 change depending on which, being (96:96), (96:48), (96:24), (96:12).

Design decisions

In analog circuit design, one of the primary objectives is to minimize the area occupied by the circuit. Therefore, wherever a high degree of matching is not required, smaller transistor widths (W) and minimum channel lengths (L) are preferred. This approach not only saves space but also reduces parasitic capacitances due to the smaller surface area.
On the one hand, in this design, transistors responsible for receiving and mirroring the master current, such as M1A4 and M1A7, have been implemented with a channel length of 2 μm to improve matching. This choice helps to minimize the relative impact of channel length modulation effects, which become proportionally less significant as the channel length increases.
On the other hand, for transistors that perform less critical roles in terms of precision-like cascodes, dummies and logic transistors- the minimum channel length of 0.6 μm has been used to reduce area and improve efficiency.

Component	Funcionality
M1A0	Dummy transistor (for switch transistor compensing)
M1A1/M1A3	Cascode transistor
M1A2	Voltage biasing transistor
M1A4/M1A5/M1A7	Mirroring transistor
M1A6	Switch transistor
M1A8	Output transistor
M1A9/M1B0/M1B1/M1B2	Logic gate transistor

Table 2.4: Name and funcionality of the components of current mirror sub-block in the Programmable Current Source block.

2.4 Simulation

In order to test the Programmable Current Source block, two different tests have been performed. First, for a fixed resistance (following the ones in Table 2.2), the output current control by VCTRL has been checked. The results can be seen in 2.7, where the output current in terms of the control voltage is shown on a logarithmic scale. The maximum range for the currents is 2.84 mA, 146μA, 7.26μA, and 445 nA for the selected sub-blocks Mirror0, Mirror1, Mirror2 and Mirror3. The selection is performed by the Logic block (see Chapter 4).

As a second test, a corner analysis of the design was performed. An example is shown in Fig. 2.8, where the current in MIRROR3 versus VCTRL is shown for the considered corners (Slow-Slow SS, Typical TT, Fast-Fast FF, and Slow-Fast SF). The data for the maximum current, considering these same corners, is shown in Table 2.5 for the four current mirrors.

	MIRROR0	MIRROR1	MIRROR2	MIRROR3
SS	492 nA	8.02 μA	161 μA	3.14 mA
TT	445 nA	7.26 μA	146 μA	2.84 mA
FF	459 nA	7.48 μA	150 μA	2.92 mA
SF	415 nA	6.76 μA	136 μA	2.64 mA

Table 2.5: Maximum current values of the current mirrors, considering the corner analysis.

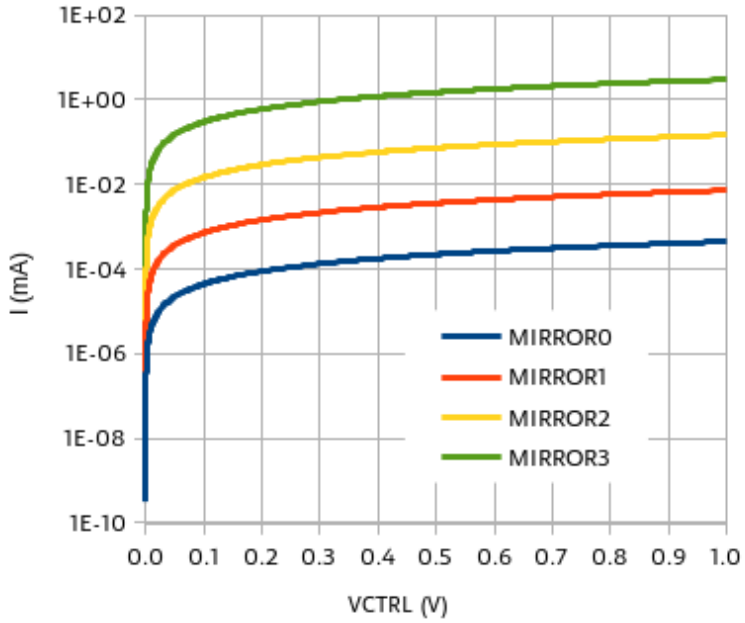

Figure 2.7: Current output of the different mirrors in the programmable source

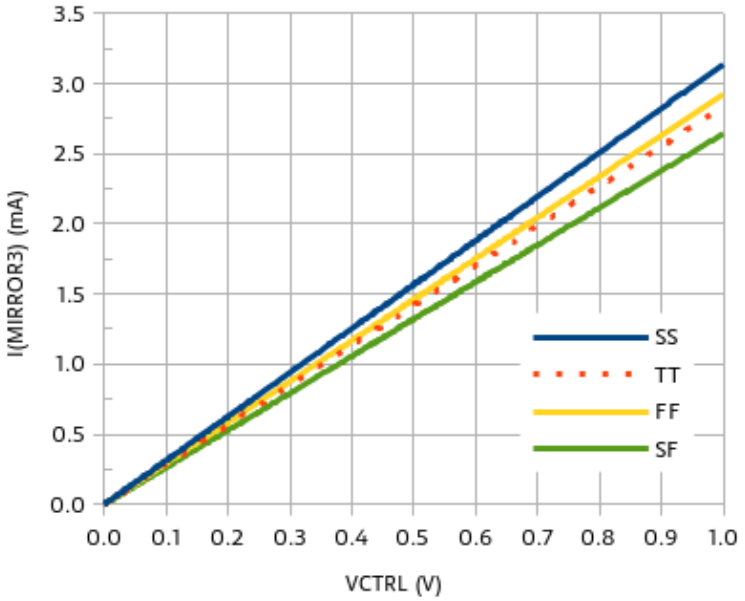

Figure 2.8: Corner analysis of the current in MIRROR3 versus VCTRL

CHAPTER 3

MEMRISTOR SELECTOR

3.1 Overview

This chapter presents the design and functionality of the Memristor Selector block, a key component in the measurement system developed for the characterization of organic memristors. Its primary purpose is twofold: to dynamically select between two memristors and to control the polarity of the applied current—an essential feature, given that the resistive state of memristors depends on current direction.

The chapter outlines the functional specifications and schematic design of the circuit, emphasizing its structure based on switchable transistor branches that establish a valid current path for each selected memristor. Design considerations are also discussed, focusing on robustness under fast pulsed signals and the minimization of parasitic capacitances.

Lastly, simulation results are provided to validate the selector's performance in terms of switching time and the equivalent resistance of the transistors, confirming that their contribution to the overall measurement is negligible.

3.2 Specifications

The main purpose of this block, highlighted in Fig. 3.1, is twofold: (1) to enable or disable the necessary transistors in order to select which of the two memristors will be used, and (2) to control the polarity applied to the selected memristor by activating or deactivating the corresponding switches. Then, the summary of the main specifications include:

- Capability of memristor selection.
- Ability of memristor polarity selection.
- Robustness against fast-pulsed signals.

When the current injected by the Programmable Current Source enters the system, it is routed through the selected memristor in either direction, depending on the configuration.

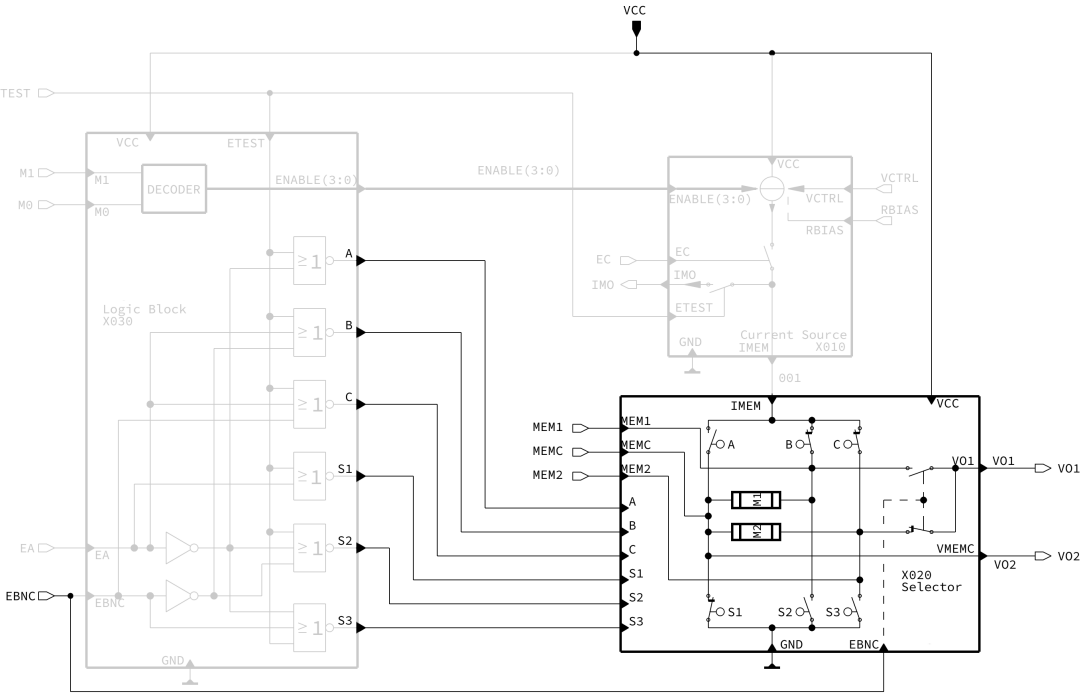

Figure 3.1: Memristor Selector symbol in the Full System schematic.

This bidirectional control is essential, as the resistance state of the memristor depends on the polarity of the applied current. To support this, the block was designed with switching logic capable of dynamically connecting each memristor terminal either to ground or to the current injection node. After current injection, two output nodes allow for measuring the resulting voltage drop across the memristor, enabling precise characterization of its electrical behavior.

Moreover, the circuit was specifically designed to maintain robustness under fast-pulsed signal conditions, mitigating the impact of parasitic capacitances introduced by the switching transistors. It is worth noting that organic memristors are relatively slow devices, meaning that even pulsed signals with a period of 200 μs are already considered fast for their response time.

3.3 Schematic Design

The schematic design of the Memristor Selector is presented in Fig. 3.2, while the pinout of the block is described in Table 3.1.

The internal configuration of this block may initially appear complex, but its structure is quite straightforward. The system consists of three branches:

- One connected to the common node (M201–M202)
- One connected to Memristor 1 (M203–M204)
- And one connected to Memristor 2 (M205–M206)

Each branch includes a pair of transistors. Depending on which transistor is activated—either the even-numbered (M202, M204, M206) or odd-numbered (M201, M203, M205)—each node

is connected either to the current injection node (odd) or to ground (even). This arrangement allows dynamic control over both the selection of the memristor and its polarity, simply by enabling the appropriate switches.

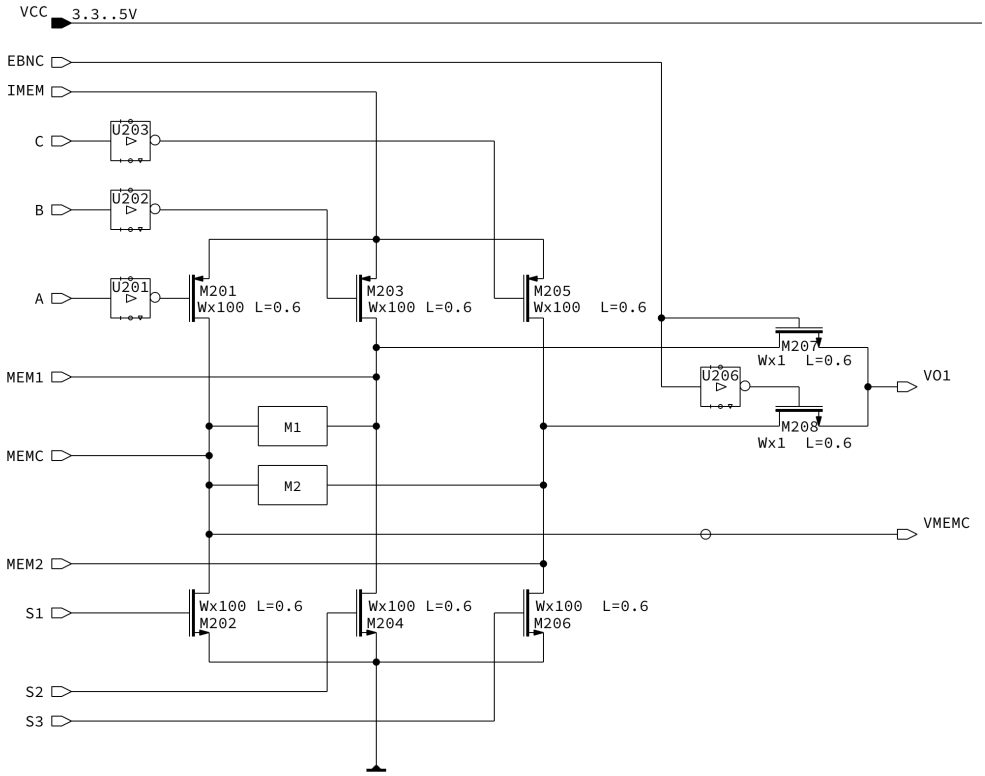

Figure 3.2: Schematic design of the Memristor Selector

Pin	I/O	Funcionality
VCC	Input	Power Supply Voltage
GND	Input	Ground
IMEM	Input	Current injection node
EBNC	Input	Memristor output selection
A-B-C	Input	Injector to memristor branch selector
S1-S2-S3	Input	Ground to memristor branch selector
MEM1	Input	Memristor 1 node
MEM2	Input	Memristor 2 node
MEMC	Input	Common memristors node (input)
VMEMC	Output	Common memristors node (output)
VO1	Output	Memristor output

Table 3.1: Memristor Selector pinout description

The key design objective is to ensure that, at any given moment, the selected memristor has one terminal connected to the injection node and the other to ground, establishing a valid

current path. Meanwhile, the unselected memristor remains electrically disconnected and plays no role in the system's behavior.

Following the switching stage, a sensing stage is implemented. It includes two complementary transistors that connect the non-common terminal of the selected memristor to the voltage output node (VO1), based on the control signal EBNC. This configuration enables voltage monitoring during memristor operation.

While the switch matrix may seem involved, the Logic Block (see Chapter 4) abstracts all the complexity by handling both the memristor selection and polarity control by only two pins.

Table 3.2 provides a summary of the transistors involved in the block along with their specific functions.

Component	Funcionality
M201/M203/M205	Injector node to memristor switches
M202/M204/M206	Ground to memristor switches
M207	MEM1 to output (VO1) switch
M208	MEM2 to output (VO1) switch
M1	Memristor 1
M2	Memristor 2

Table 3.2: Name and funcionality of the components of Memristor Selector block

Design decisions

- During the design phase, it was essential to ensure that the transistors could handle the maximum expected current. This scenario corresponds to the case where 96 transistors are connected in parallel (Wx96), each with a minimum channel length of 0.6 μm. Given that sufficient layout area is expected to be available, the design was intentionally overdimensioned to account for possible current peaks, using a total of 100 parallel transistors for added robustness.
- To manage the activation and deactivation of the switching transistors, inverters were placed at control pins A, B, and C. This configuration, when combined with the logic implemented in the Logic Block, results in an optimized number of total logic gates. In this block, the VCC pin does not play a major functional role, other than biasing the bulks and wells of the transistors. However, due to the presence of the inverter gates, its inclusion has become necessary.
- For the output transistors (M207–M208), which are used solely to sense the voltage at node VO1 (i.e., no current is expected to flow through them), the sizing was minimized. This means reducing the number of transistors in parallel in order to save area and minimize parasitic capacitance, thus preserving signal integrity in the sensing path.

3.4 Simulation

Since the current can be pulsed and set to various levels and flows through the switching transistors in addition to the memristor, the key performance parameters are the equivalent resistance of the system, the switching time, and the charge injection. The two later problems are addressed by simulating an injected 10 μs current pulse, with an amplitude of 10 μA, with the switch connected to a 10 kΩ resistor. The corresponding simulation is shown in Fig. 3.3[1]. The graphic has been processed with Matlab, where the commutation time had shown to be 0.34 μs, which is sufficient for the system purposes.

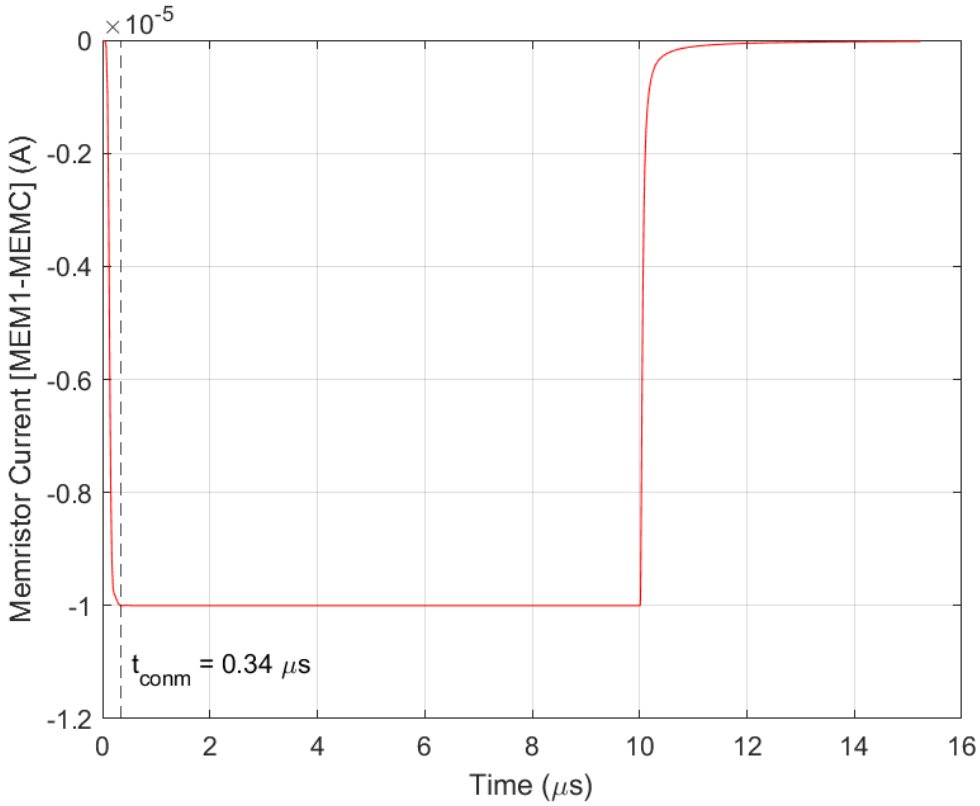

Figure 3.3: Current output through switch M201 in the typical case, when undergoing a 10 μs current pulse, with an amplitude of 10 μA, with the switch connected to a 10 kΩ resistor.

In order to evaluate the resistance of the switching transistors, the voltage drop across them must be analyzed. A corner analysis was performed on the M204 transistor, assuming that Memristor 1 is connected to the MEM1 node tied to the ground and MEMC connected to the current injection node. A current ramp from 0 to 3 mA was applied (covering the full operational range) and the resulting voltage drop was recorded.

The voltage drop, shown in Fig. 3.4, demonstrate a linear behavior. The slope of the line corresponds to the equivalent resistance of the switch, which can be estimated by calculating

[1]The current in Fig. 3.3 is negative because the switches are connected in order that the current flows from MEMC to MEM1, which is the opposite polarity of the one established in the simulation, where the positive node of the memristor is MEM1 and the negative node is MEMC.

the ratio between the maximum current and voltage values. The results are shown in Table 3.3.

The equivalent resistance of the switches is less than 1.2Ω, which results in a total of approximately 2.4Ω, considering that two transistors are always active in the current path. Given that the equivalent resistance of the organic memristors ranges from 1 kΩ to 1 MΩ, the contribution of the switches is negligible. Therefore, the design meets the requirements without introducing significant errors or performance degradation.

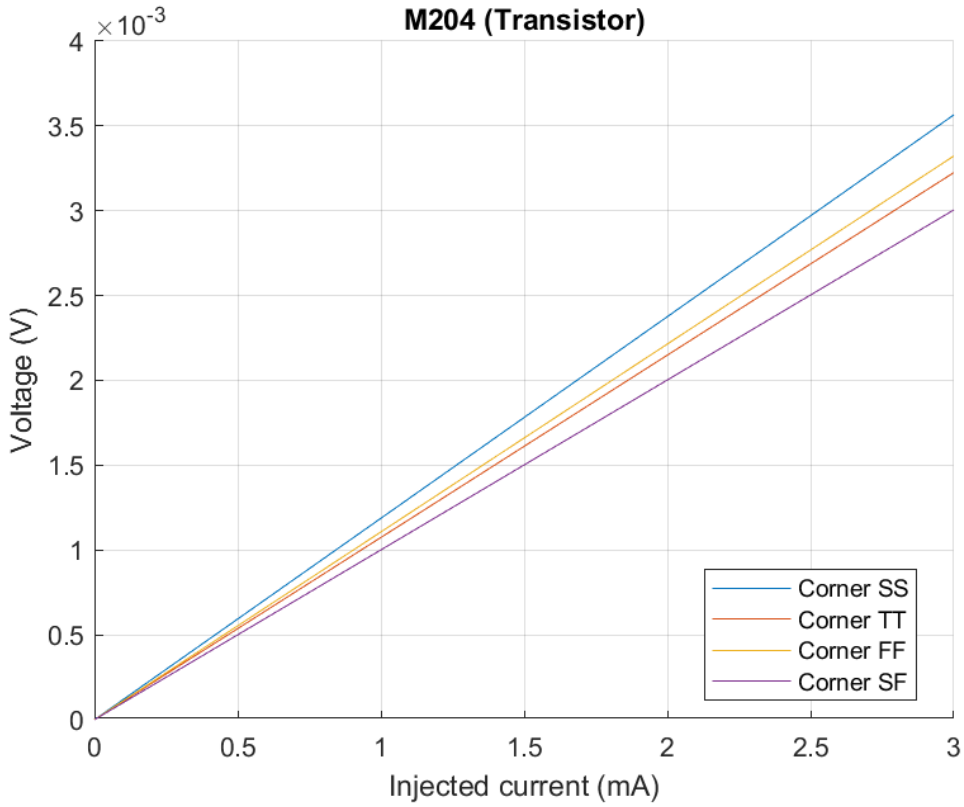

Figure 3.4: Voltage drop in M204 transistor when a current ramp from 0 to 3mA is applied.

Corner	V_{max} (mV)	Req (Ω)
SS	3.57	1.19
TT	3.22	1.07
FF	3.32	1.11
SF	3.01	1.00

Table 3.3: Maximum voltage and equivalent resistance per corner for transistor M204. A current ramp from 0 to 3 mA was applied; the minimum voltage is not specified, as it is 0 by definition.

CHAPTER 4

LOGIC BLOCK

4.1 Overview

This chapter presents the Logic Block, which manages the control logic for current mirror selection and memristor operation. It generates the required output signals from a minimal set of input bits, including the ETEST signal for test mode.

The chapter details the block's schematic design, divided into two sub-blocks: one for decoding the current mirror selector inputs, and another for controlling the switches in the Memristor Selector. Truth tables and implementation logic are provided to illustrate the behavior and simplicity of the design.

4.2 Specifications

The main objective of this block, highlighted in Fig. 4.1, is to manage the overall system logic. Specifically, it controls two key aspects: (1) the selection of the current mirror to be used, (2) and the activation or deactivation of the transistors required to perform the intended functions in the Memristor Selector block. The specifications for this block were relatively simple:

- Accomplishment of the logic functions.
- Minimizing of area.

This is the simplest block in the system. The main challenge was to derive logical functions that would produce the required output states using only two input bits, while minimizing the number of logic gates used.

In addition, this block also takes into account the ETEST bit. As described in Chapter 2, this bit is responsible for setting the system in TEST mode, in which the injection current bypasses the memristors and is routed directly to the IMO pin. To implement this behavior, the logic block needs not only to activate the transistor connected to IMO, but also to disable current flow through the IMEM path.

The simplest and most effective way to achieve this is by turning off all switches in the Memristor Selector block, thereby preventing any valid current path through the memristors and forcing the entire injected current to exit via the IMO pin.

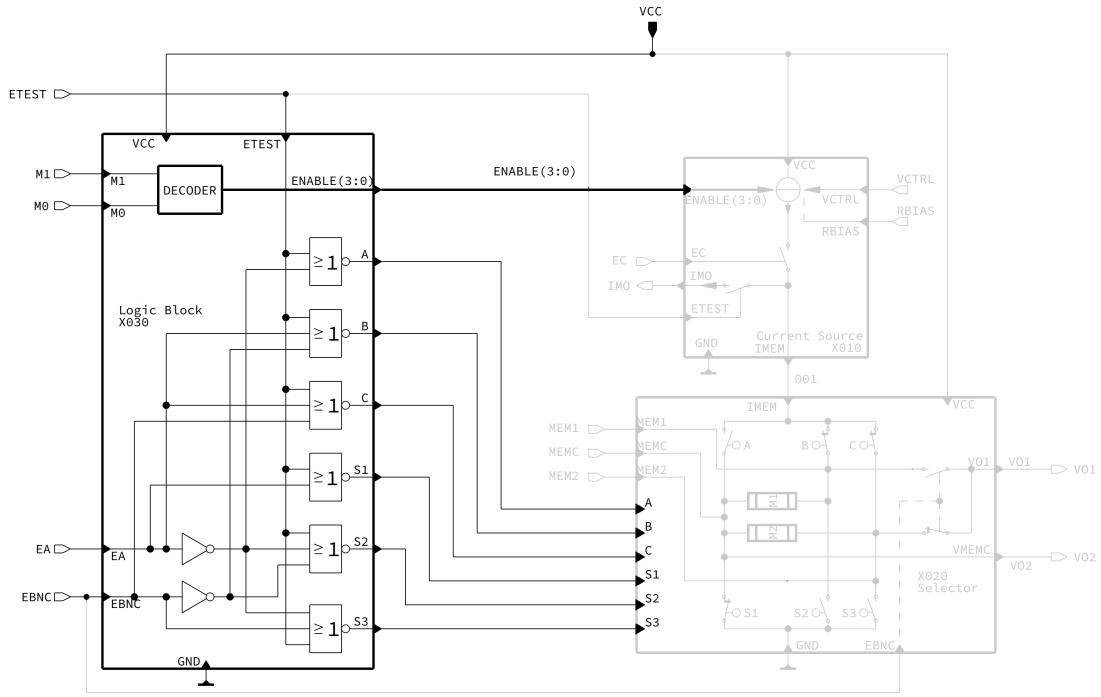

Figure 4.1: Logic Block symbol in the Full System schematic.

4.3 Schematic Design

The schematic of this block is shown in Fig. 4.2, while the pinout of the block is described in Table 4.1. As explained before, the design of the Logic block is divided in two sub-blocks: the Current Mirror decoder and the Memristor Selector Logic.

The Current Mirror Decoder receives a 2-bit binary word (M1-M0) that activates the corresponding bit of the ENABLE signal associated with the selected current mirror. This also ensures that only one mirror is active at any given time. The corresponding truth table for this logic sub-block is shown in Table 4.2.

On the other hand, the Memristor Selector Logic has two control inputs: Enable A (EA) and Enable B Not C (EBNC). The EBNC bit determines which memristor is selected: when EBNC = 1, Memristor 1 is active; when EBNC = 0, Memristor 2 is selected. The EA bit controls the activation of the transistor connected to node A. When EA = 1, the selected memristor is reversed biased by connecting node MEM1 or MEM2 to ground and node MEMC to the injection path. Conversely, when EA = 0, the memristor is forward biased (i.e., MEM1 or MEM2 is connected to the injector and MEMC to ground). If the ETEST bit is active, all switching transistors are turned off and no current flows through the memristor path. Instead, the injection current is redirected entirely to the IMO pin. The truth table corresponding to this logic sub-block is shown in Table 4.3.

Pin	I/O	Funcionality
VCC	Input	Power Supply Voltage
GND	Input	Ground
EBNC	Input	Memristor selection
EA	Input	Polarity selection
M1-M0	Input	Current mirror selector
A-B-C	Output	Injector to memristor branch selector
S1-S2-S3	Output	Ground to memristor branch selector
ENABLE(3)	Output	Mirror 3 enabler
ENABLE(2)	Output	Mirror 2 enabler
ENABLE(1)	Output	Mirror 1 enabler
ENABLE(0)	Output	Mirror 0 enabler

Table 4.1: Logic Block pinout description

Inputs		Outputs			
M1	**M0**	**E3**	**E2**	**E1**	**E0**
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Table 4.2: Current Mirror Decoder truth table

Inputs			Outputs					
ETEST	**EA**	**EBNC**	**A**	**B**	**C**	**S1**	**S2**	**S3**
0	x	x	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0
1	0	1	0	1	0	1	0	0
1	1	0	1	0	0	0	0	1
1	1	1	1	0	0	0	1	0

Table 4.3: Memristor Selector Logic truth table.

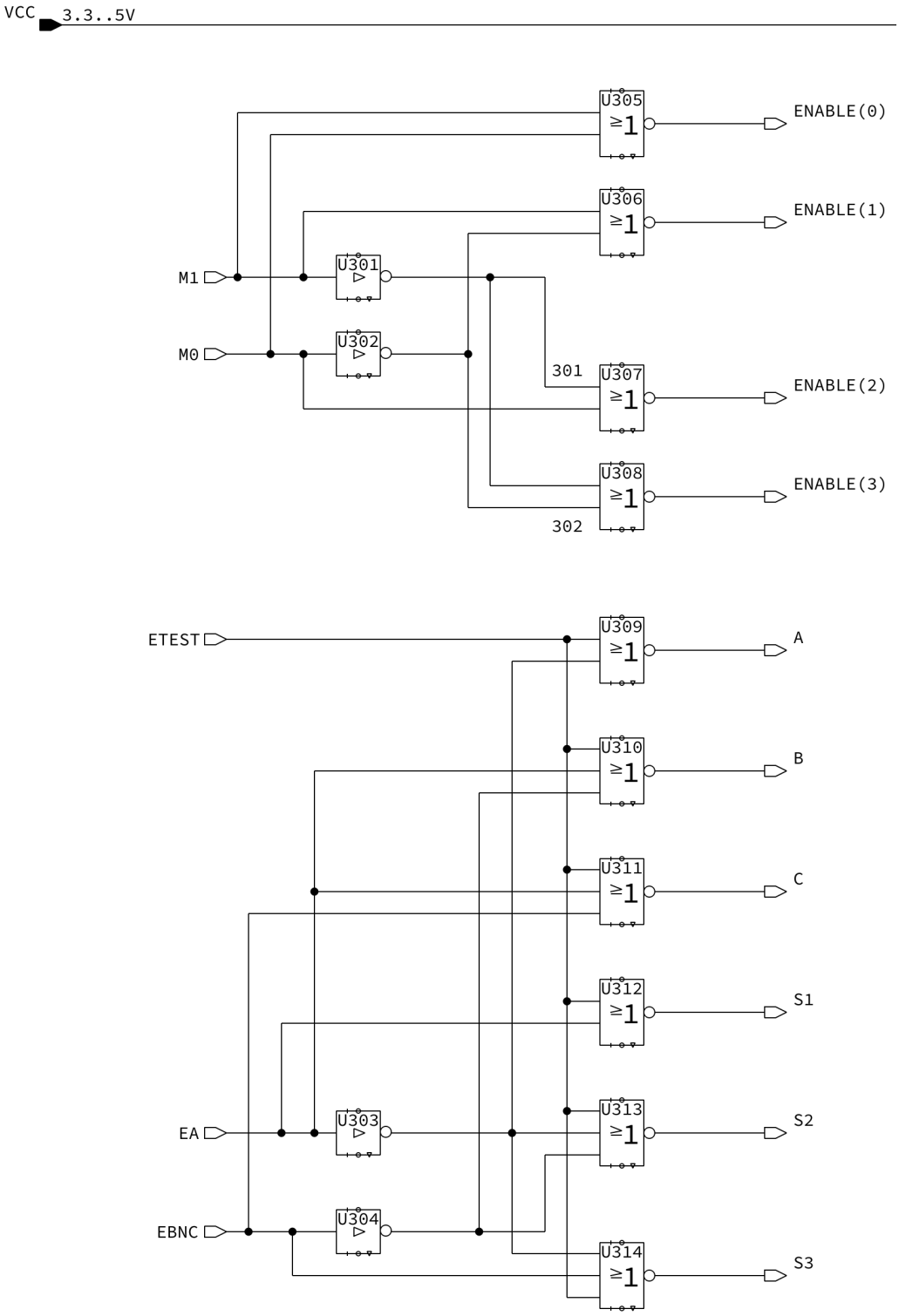

Figure 4.2: Logic Block schematic

CONCLUSION

Objectives and Scope of the Study

The primary objective of this Master's Thesis was to design an integrated readout system for memristive devices, with special attention to organic memristors. The work focused on developing a programmable, low-invasiveness testbench based on current injection and voltage sensing—an alternative to traditional voltage-driven readout approaches. The scope included the complete schematic-level design of three functional blocks (current source, memristor selector, and logic controller) using 0.18 µm CMOS technology. While the system has been optimized through simulation, the physical layout phase remains as a future step.

Key Findings

The system has proven its capability to deliver a wide range of controlled currents (from hundreds of nA to a few mA) with high linearity and robustness, even under temperature and process variation scenarios. The current injection strategy ensures safe, non-disturbing readout of the memristor's resistive state. Additionally, the selector block enables dynamic switching between two memristors and allows current polarity control—crucial for resistive tuning. The inclusion of a TEST mode enhances calibration flexibility, allowing external validation of the injected current.

Theoretical Analysis

The theoretical work included the definition of electrical specifications, topology selection, and detailed schematic design of each block. The current source design was particularly challenging, requiring high precision across multiple current ranges. Simulation analyses (DC, transient, and corners) confirmed the intended behavior of the system under various conditions. Voltage-to-current conversion was achieved with an operational amplifier and carefully dimensioned mirror stages, ensuring accurate current delivery over the target voltage window.

The logic block was optimized for minimum complexity and gate count, using a truth table-based design to control both the selector switches and the current mirror configuration. Signal integrity and logic correctness were validated through functional simulation.

Simulated Evaluation

While no physical implementation was carried out, extensive simulated testing was performed to evaluate the experimental feasibility. The selector block was tested with pulsed signals of short duration (10 µs), confirming sub-microsecond switching times and negligible ON resistance (<2.4 Ω total), which ensures accurate measurement without affecting the memristor's behavior. The overall system was tested under multiple excitation conditions to simulate

real-world scenarios. These results serve as a strong foundation for future physical prototyping and validation.

Applications and Future Potential

The system is designed to be compatible with direct deposition of memristors, enabling on-chip characterization in research and prototyping environments. Applications include neuromorphic hardware, low-power embedded systems, flexible electronics, and in-memory computing. Its non-invasive and programmable nature makes it well-suited for testing fragile memristor technologies, particularly those based on organic materials.

Looking forward, the next step involves the layout design of the full system. This phase will reveal physical constraints such as parasitic effects, routing challenges, and mismatch impacts. Post-layout simulations will be essential to refine the system and bring it closer to fabrication readiness. Once completed, the platform could be used not only as a characterization tool but as a component in larger mixed-signal or neuromorphic architectures.

In conclusion, this work provides a solid and innovative foundation for the safe and accurate characterization of memristive technologies. It fulfills all the initial objectives and opens the door to a wide range of future experimental and applied developments.

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