Electrical Properties and Nanoresistive Switching of Ni-HfO_2-Si Capacitors

ECS Transactions, 72 (2) 335-342 (2016)
10.1149/07202.0335ecst ©The Electrochemical Society

Electrical Properties and Nanoresistive Switching of Ni-HfO_2-Si Capacitors

H. García[a], M. B. González[b], C. Vaca[a], H. Castán[a], S. Duenas[a], F. Campabadal[b], E. Miranda[c], and L. Bailón[a]

[a] Department of Electronics, University of Valladolid, 47011 Valladolid, Spain.
[b] Institut de Microelectrònica de Barcelona (IMB-CNM), CSIC, Campus UAB, 08193 Bellaterra, Spain
[c] Universitat Autònoma de Barcelona, 08193 Bellaterra, Spain

Ni/HfO_2/Si ReRAM devices were extensively characterized. In the pristine state, they show adequate performance with low leakage currents and moderate interfacial state density. Leakage current is dominated by Poole-Frenkel mechanism. Activation energies of conduction processes and soft-optical phonons in the insulator bulk are 80 and 50 meV, respectively. Both are usual values in high-k dielectrics. Devices show unipolar resistive switching behavior, with two well-defined resistance states. They can switch properly at temperatures as low as 77 K. Transitions between both resistance states are electric field and temperature dependent.

Introduction

Resistive random access memory (ReRAM) devices based on HfO_2 are studied intensively because of its high compatibility with CMOS process beyond the 22 nm node (1). These devices exhibit a resistive switching (RS) behavior, occurring upon applying voltage without any phase changes, but because of the creation of one or several conductive filaments (CF) that act as a circuit breaker/switch between the electrodes. These ReRAM devices are considered to be the most promising candidates to replace the current flash memories or other proposals in the nonvolatile memory realm, because of their potential for low power consumption, high integration density, fast-speed, endurance, and viability for 3D memory stacks. In fact, the breaking and forming of a CF occurs over a nanometer-scale region in a timespan of nanoseconds (2). Among a wide range of transition metal oxides, HfO_2 presents excellent switching properties (3). One of the major difficulties to HfO_2 integration into silicon technology is the presence of electrically active defects, which can play an important role in the final device operation. Atomic layer deposition (ALD) has been demonstrated as a very suitable technique for obtaining uniform layers with a precise control of film composition and thickness as the growth proceeds one monolayer at a time on an atomic scale (4, 5). This is a method of cyclic deposition, where alternately supplied precursors react on a surface in a self-limiting manner. In spite of this good characteristics, metal-oxide-semiconductor (MOS) structures fabricated with ALD deposited oxide films can exhibit low-quality interfaces. So, it is mandatory to carry out a complete electrical characterization of ReRAM devices in order to determine the final film quality and properties. On the other hand, there is a lack of low-cost high-density and endurable non-volatile memories for aerospace and low-temperature applications. Therefore, in order to explore the potential applications of ReRAM devices, it is imperative to investigate their cryogenic performance (6).

For Ni/HfO_2-based devices in unipolar operation, the formation and dissolution of CF is attributed to Ni migration from the metal electrode, and to thermally enhanced diffusion induced by Joule heating, respectively (7, 8). In this work, a complete electrical characterization of Ni/HfO_2/Si ReRAM devices was performed, focusing on interface quality and defect density in the dielectric. To do this, current-voltage (I-V), capacitance-voltage (C-V), conductance-voltage (G-V), conductance transient analysis (G-t), deep-level transient spectroscopy (DLTS), and flat-band voltage transient at constant capacitance (V_{FB}-t) techniques were used. In addition, resistive switching has been evaluated in the range of 77-473 K, by means of the application of repeated sweep voltages with appropriate current compliance.

Experimental

The MOS devices were fabricated on (100) n-type CZ silicon wafers with resistivity in the range 7-13 mΩ·cm. All fabrication details have been previously published (9). The main technological aspects are the following: After a standard wafer cleaning, a wet thermal oxidation process was done at 1100 ºC, leading to a 200 nm thick SiO_2 layer. This field oxide was patterned by photolithography and wet etching. Prior to the HfO_2 deposition, a cleaning in H_2O_2/H_2SO_4 and dip in HF(5%) were done. The 20 nm-thick HfO_2 layers were deposited by atomic layer deposition (ALD) at 225 ºC using TDMAH and H_2O as oxidant precursors and N_2 as carrier and purge gas. The top 200 nm-thick Ni electrode was deposited by magnetron sputtering. The resulting structures are square cells of 5x5 μm^2.

Electrical measurements of MOS structures in the pristine state were carried out putting the sample in a light-tight, electrically shielded box. In order to record electrical parameters at temperatures from liquid nitrogen temperature (≈ 77 K), samples were cooled in an Oxford DM1710 cryostat. An Oxford ITC 502 temperature controller was used to keep the temperature constant while electrical measurements. I-V curves were measured using the HP-4155B semiconductor parameter analyzer. C-V and G-V measurement setup involved a Keithley 4200SCS semiconductor analyzer. The experimental set-up of the conductance transient technique consisted of an HP 3310A function generator to apply the bias pulses, an EG&G 5206 two-phase lock-in analyzer to measure the conductance, and a HP 54501A digital oscilloscope to record the complete conductance transients. Interface trap density (D_{it}) was measured by DLTS. These measurements were performed using a Boonton 72B capacitance meter, an HP 54501A digital oscilloscope to record the capacitance transients, and an HP 8112A pulse generator to bias the samples from inversion to accumulation. Finally, an Agilent N6700B bias source, a Keithley 6517A electrometer, and a Boonton 72B capacitance meter were used for recording V_{FB} transients.

After the study of pristine samples, the MOS devices were electroformed by DC reverse bias sweeping from 0 to 13 V with a current compliance of 0.1 mA. Then, successive low-resistance state (LRS) to high-resistance state (HRS) I-V cycles were recorded from 77 to 473 K, using an HP4155B semiconductor parameter analyzer in the voltage sweep mode with current compliance of 0.1 mA for the HRS and 100 mA for the LRS.

Results and Discussion

Fig. 1 shows 1 MHz C-V and G-V curves measured at room temperature. Hysteresis in C-V vanishes when temperature diminishes, thus indicating that border traps density is very low. This was confirmed by means of conductance transient analysis, which resulted in negligible values for border traps density. On the contrary, the stretch-out of C-V curves and the height of the conductance peaks indicate that there is a moderate amount of density of states in the interface, D_{it}. DLTS measurements demonstrated a quite homogeneous energetic distribution of D_{it}, with values of around $1x10^{12}$ cm^{-2} eV^{-1} (see Fig.2). Although this density value is usual in high-k dielectrics as HfO_2 (10), it could be problematic in the transistor applications field due to the effects of interfacial states on the lowering of the channel mobility. However, for memory applications this value is not a major concern.

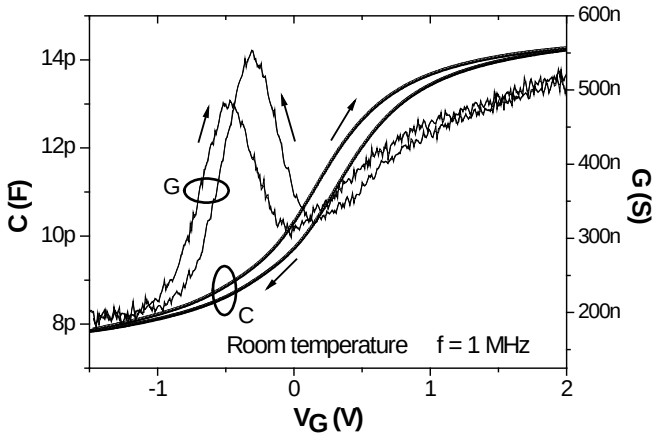

Figure 1. 1 MHz- C-V and G-V curves measured at room temperature.

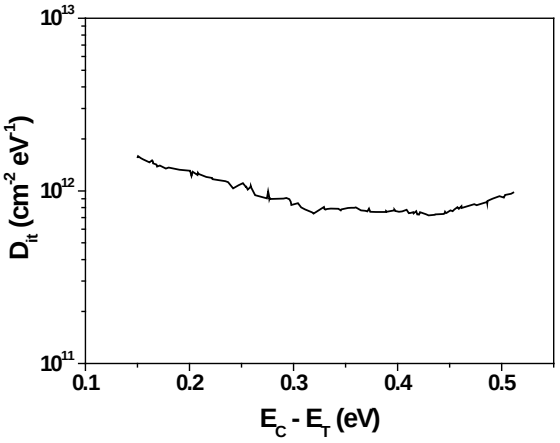

Figure 2. Interfacial state density measured by DLTS.

As for leakage current densities, they are quite acceptable, with values of around 3 - 4 x 10^{-7} A cm^{-2} in the accumulation regime (up to 2 - 3 V), and almost negligible in the depletion regime. I-V data fit well to the Poole-Frenkel model especially in the high electric field (E) range (Fig. 3):

$$I = I_0 \, exp\left(\frac{\beta_{PF} E^{1/2}}{KT}\right) E \qquad [1]$$

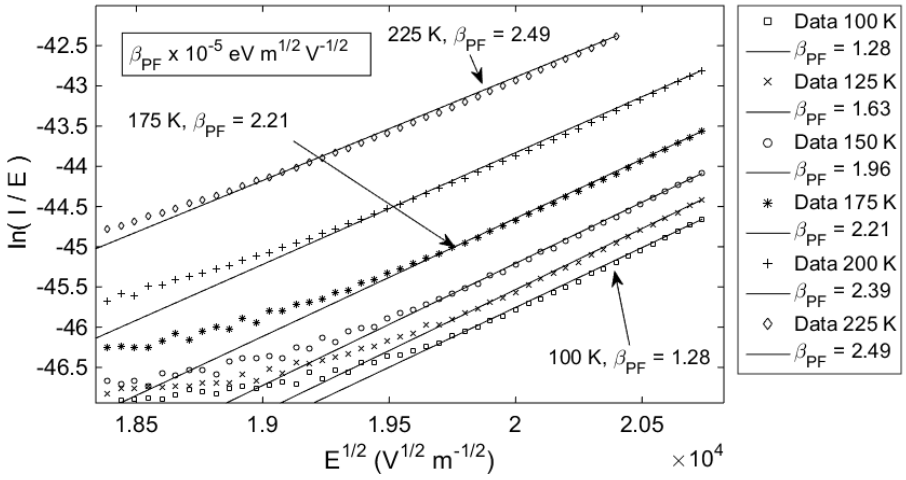

Figure 3. Poole-Frenkel plot at several temperatures. Experimental (dots) and fitting curves (solid line) are shown.

This is in good agreement with previously reported results (11, 12), and indicates that the main conduction is bulk limited, associated with the field-enhanced thermal excitation of charge carriers from traps. The theoretical value of field-lowering coefficient, β_{PF}, obtained from the permittivity value of HfO_2 at optical frequencies is around 4 x 10^{-5} eV $m^{1/2}V^{-1/2}$, taking into account that the refractive index for HfO_2 ranges from 1.7 to 1.9. The experimental values are reasonably in agreement with the theoretical one. The small discrepancy can be related to the physical structure of the films that differs from the theoretical case. Additionally, the conduction behavior could be influenced by other conduction mechanisms, which may contribute to the current, although this is mainly dominated by Poole-Frenkel emission. In Fig. 4 the obtained Arrhenius plots from the experimental results for several bias voltages are shown. In the 150-300 K temperature range the relationship between ln(I) and $1/K_BT$, with K_B the Boltzmann constant, is clearly lineal, as expected for the Poole-Frenkel emission, which is associated with the field-enhanced thermal excitation of charge carriers from traps.

As shown, the slopes of the fitting lines do not vary significantly with the applied voltage, indicating that the conduction takes place through a thermally activated process having a single activation energy, ΔE_σ, which follows the relation:

$$I = I_0 \, exp\left(-\frac{\Delta E_\sigma}{KT}\right) E \qquad [2]$$

The activation energy value obtained, around 80 meV, is similar to those previously reported for HfO_2 (13). As the temperature decreases below 155 K the current becomes temperature independent. This can be attributed either to the presence of the competing emission mechanisms or to the device self-heating (14).

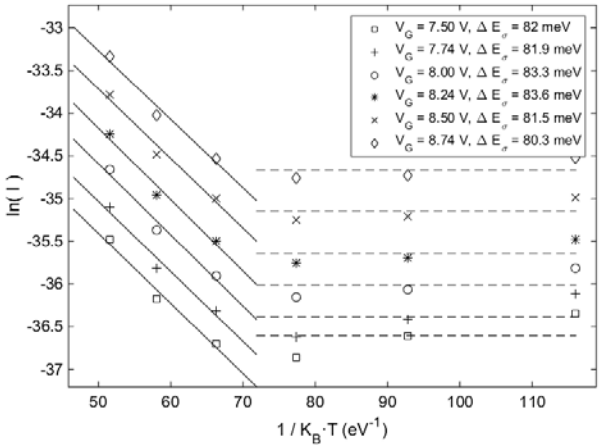

Figure 4. Arrhenius plot from I-V measurements and the obtained activation energy of conduction process through the dielectric.

Flat-band voltage transients were recorded at different temperatures (Fig.5). As flat-band transients were recorded under conditions without external stress, they are originated by phonon-assisted tunneling between localized states (15). Phonons produce the ionization of traps existing in the bandgap of the insulator.

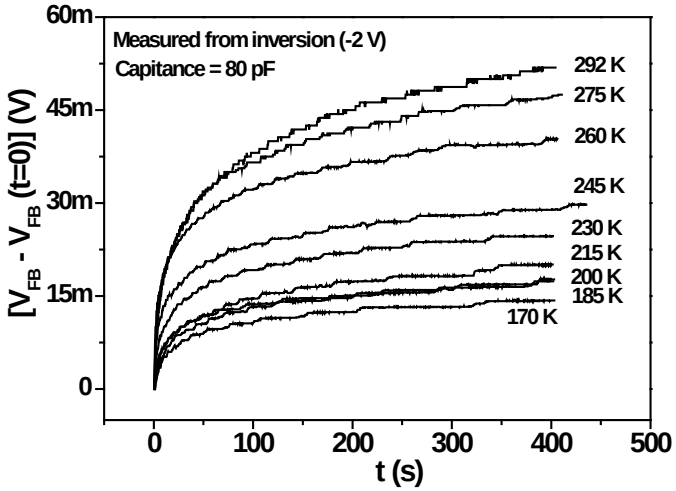

Figure 5. Flat-band transients measured at different temperatures.

Electrons and /or holes generated in this way move from trap to trap until they reach a defect location and neutralize the charge state of this defect. Indeed, the flat-band transients amplitudes follow an Arrhenius plot (Fig. 6) with an activation energy of around 50 meV, in the range of the soft-optical phonon energies (W_{PH}) usually reported for the high-k dielectrics (16). Charge trapping and detrapping inside the dielectric can cause device instability and some performance degradation.

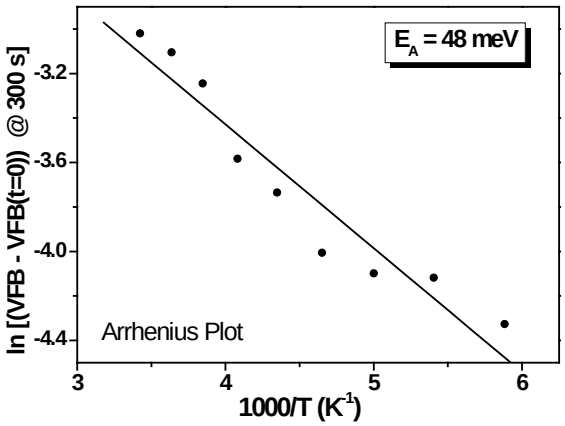

Figure 6. Arrhenius plot and the obtained activation energy of the soft-optical phonons in the dielectric.

After the study of pristine samples, the MOS devices were electroformed by DC reverse bias sweeping from 0 to 13 V with a current compliance of 0.1 mA. Electroforming causes a current-limited oxide breakdown, and a metallic filament is created (17). So, devices are taken to the low resistance state (LRS). A cycle is completed when the CF is partially broken by applying a reset voltage and samples switch to the high resistance state (HRS). In Fig. 7 the electroforming and first RS cycles at room temperature are depicted.

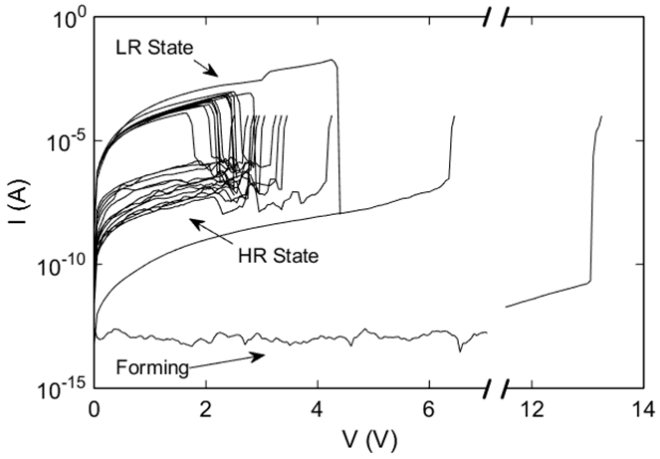

Figure 7. Electroforming and the first R-S cycles showing high and low resistive states.

After electroforming, successive LRS–HRS cycles were recorded from 77 to 473 K (Fig. 8). Transitions between both resistance states are electric field and temperature dependent.

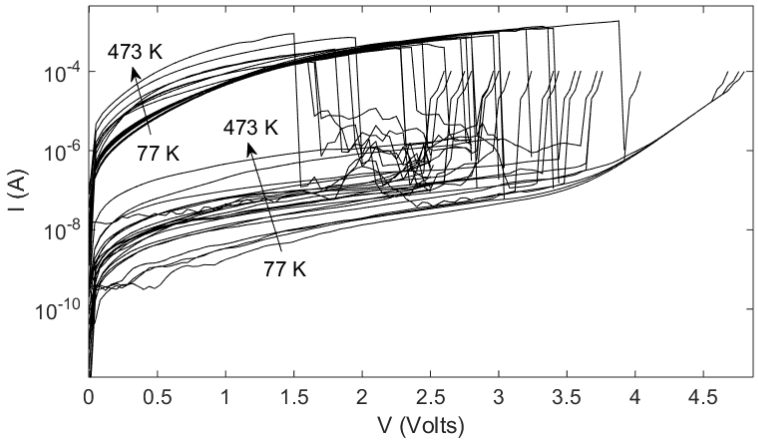

Figure 8. Low and high-resistance state I-V curves measured in the range 77-473 K.

Each LRS curve fits very well to its next HRS curve at the reset voltage, as it is shown in Fig. 9 for four randomly chosen cycles. Hence, there is a clear correlation between the current value measured just when switching from low to high resistance occurred at the previous reset voltage value, $I_{LRS}(N-1)$ at $V_{reset}(N-1)$, and the value of the OFF state current, $I_{HRS}(N)$, at the same voltage where previous reset switching occurred ($V_{reset}(N-1)$).

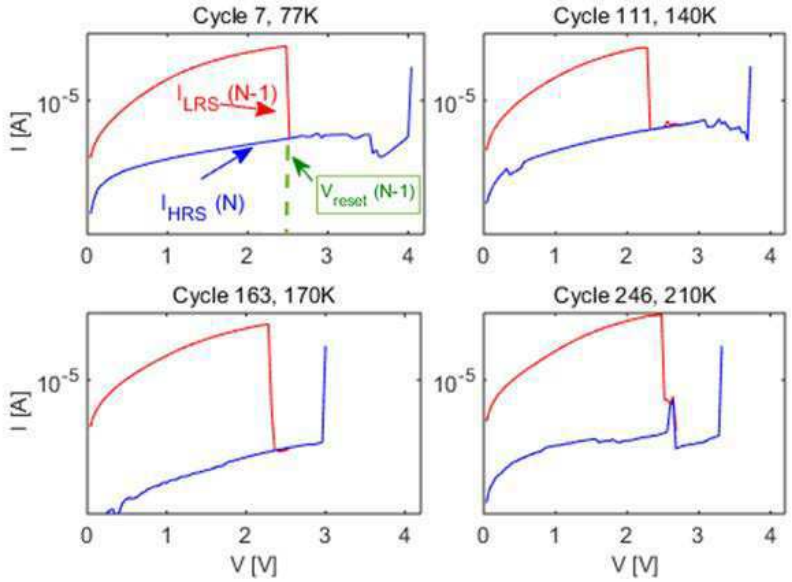

Figure 9. Low resistance I-V curve and its consecutive high-resistance curve at several temperatures.

Conclusions

$Ni/HfO_2/Si$ ReRAM devices exhibit adequate electrical properties and perform correctly at temperatures ranging from cryogenic to high temperatures. From electrical measurements, moderate interfacial states and slow traps densities in the dielectric were

detected, with low leakage currents. The conduction behavior was dominated by Poole-Frenkel emission, so the gate current in these samples is due to thermally activated process. In addition, resistive switching phenomena has been observed in a wide range of temperatures with well-defined resistance states even at temperatures as low as 77 K . As this structure can be directly implemented in advanced CMOS logic technology without employing any exotic material, it can result very attractive for embedded nonvolatile memories.

Acknowledgments

This work was partially funded by the Spanish Ministry of Economy and Competitiveness through projects TEC2014-52152-C3-1-R, TEC2014-52152-C3-3-R, TEC2012-32305, and TEC2014-54906-JIN, with support of Feder funds.

References

1. S. M. Yu, X. M. Guan, and H. S. P. Wong, *Appl. Phys. Lett*. **99**, 063507 (2011).
2. D. S. Jeong, R. Thomas, R. S. Katiyar, J. F. Scott, H. Kohlstedt, A. Petraru, and C. S. Hwang, *Reports on Progress in Physics,* **75**, 076502 (2012).
3. K.-L. Lin, T.-H. Hou, Y.-J. Lee, J.-W. Chang, J.-H. Lin, J. Shieh,C.-T. Chou, T.-F. Lei, W.-H. Chang, W.-Y. Jang, and C.-H. Lin, *Jpn. J. Appl. Phys.* **52**, pp. 031801-1–031801-5, (2013).
4. T. Suntola, *Mater. Sci. Rep*. **4**, 261 (1989).
5. M. Ritala and M. Leskelä, in *Handbook of Thin Film Materials*, Deposition and Processing of Thin Film Materials **Vol. 1**, edited by H. S. Nalwa, Academic, San Diego, p. 104 (2002).
6. D. Fang, W. Chen, L. Gao, W. Yu, and S. Yu, *IEEE Electron Dev. Lett*. **36**, 567 (2015).
7. U. Russo, D. Ielmini, C. Cagli, and A. L. Lacaita, *IEEE Trans. Electron Devices*, **56**(2), 193 (2009).
8. A. Rodríguez, M. B. González, E. Miranda, F. Campabadal, and J. Suñé, *Mic. Eng*. **147**, 75-78 (2015).
9. M. B. González, J.M. Rafí, O. Beldarrain, M. Zabala, M.C. Acero, F. Campabadal, *IEEE Trans. Device Mater. Reliab*. **14**, 769, (2014).
10. G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
11. C.Walczyk, D. Walczyk, T. Schroeder, et al, *IEEE Trans on Electron Dev*. **58**, 3124 (2011).
12. S. Dueñas, H. Castán, H. García, et al, *J. Vac. Sci. Technol. B*, **27**, 389 (2009).
13. S. Dueñas, H. Castán, H. García, et al, *Semicond. Sci. Technol.* **22**, 1344 (2007).
14. O. Mitrofanov, and M. Manfra, *J. Appl. Phys.* **95**, 6414 (2004).
15. S. Duenas, H. Castán, H. García et al. *J. of Electrochem. Soc*. 1**55**(1), G241 (2008).
16. M.V. Fischeti, D. A. Neumayer, and E. A. Cartier, *IEEE Trans. Dev. Mater. Rel* **5**(1), 45 (2005).
17. C. Nauenheim, C. Kuegeler, A. Ruediger, and R. Waser, *Appl. Phys. Lett*. **96**, 122902 (2010).