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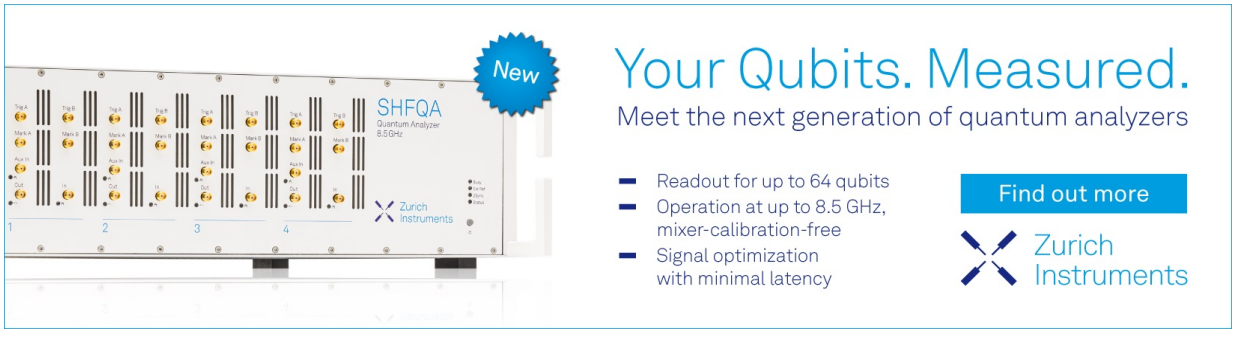

Analysis and control of the intermediate memory states of RRAM devices by means of admittance parameters

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A thorough study of the admittance of TiN/Ti/HfO_2/W bipolar resistive memories [resistance random access memory (RRAM)] was carried out under different bias conditions and in a wide range of ac signal frequencies. We demonstrate that a continuum of intermediate states can be obtained by applying appropriate dc bias waveforms. Cumulative writing and erasing admittance cycles were performed by applying triangular voltage waveform of increasing amplitude. The influence of the initial conditions on the variation of the real (conductance) and imaginary (susceptance) components of the admittance is described. An accurate control of the memory state is achieved both in terms of the conductance and the susceptance by means of an adequate selection of the voltage values previously applied. A method to obtain three-dimensional voltage-conductance-susceptance state-plots is described in detail. Memory maps of admittance parameters as a function of the programming voltage are made by sensing the memory state at 0 V, without static power consumption. The multilevel nature of RRAM devices and their suitability for neuromorphic computation are demonstrated. *Published by AIP Publishing.* https://doi.org/10.1063/1.5024836

INTRODUCTION

Resistance random access memories (RRAMs) are being intensively studied due to their promising applicabilities in the digital storage, analog computing, or neuromorphic device fields.[1–3] Their relevant properties come from its non-volatile and reversible resistance change behavior within a simple device structure. RRAM cells switch between two clearly separated states, the high resistance state (HRS or OFF) and the low resistance state (LRS or ON). The set and reset transitions drive the device from OFF to ON and from ON to OFF, respectively, by the application of electrical pulses or voltage sweeps. Most binary metal oxide-based structures evidence the formation and partial disruption of a conductive filament (CF) as the key mechanism for resistance switching.[4–7] The conduction is due to the formation of a few nanometer-sized filamentary conductive paths through the oxide spanning between two electrodes, therefore, the HRS and LRS resistances are independent of the electrode areas. The migration of oxygen ions assisted by the temperature and the electric field plays an important role in the resistive switching behavior of a great deal of metal-oxide-based-RRAM devices.[8–10] When applying a bias voltage, oxygen cations migrate from the oxide to the positively biased electrode, and the oxygen deficient zone facilitates the filament creation. In the subsequent reset operation, oxygen atoms are re-injected into the oxide, so the CF breaks down. The size of the CF is controlled by means of the current limitation imposed by a given compliance current, which avoids destructive breakdown.[9] Many works have been devoted to shed light on the physical nature of CFs, which still remains controversial. Besides the most direct applications relying on a binary mode of operation, it has been demonstrated that these devices can also be used as truly analog memory elements. The formation of a tiny multifilament network or the thickening of a single filament allows one to explain the existence of intermediate resistance states as the result of the rupture, creation, or change of some of these filaments. Subjecting the device to a train of input programming pulses in alternating polarities gives rise to gradual resistive state transitions; therefore, analog information can be stored.[11] A big effort is currently being invested in optimizing both materials and programming techniques to design devices able to represent artificial synapses. Reference 12 reports the artificial synapses in neuromorphic circuits by using a state-of-the-art HfO_2-based RRAM, capable of learning, updating, and recognizing real-world visual and auditory patterns. This realization takes advantage of the fact that the resistance after set transition is controlled by the size of the CF, which in turn is controlled by the compliance current.[13] A similar dependence on the initial state was observed in biological systems, where a synapse conductance change cannot exceed minimum and maximum values.[14]

So far, the RRAM switching dynamics has been studied in terms of gradual resistance changes.[15,16] The effect of a competition between opposite tendencies of filament dissolution and formation at opposite metal/HfO_2 interfaces might play a role in the observed dynamics.[16] Just a few recent works reported devices able to gradually increase and decrease their resistance when proper electrical signals are applied. For example, the work described in Ref. 17 was devoted to achieving the analog resistance transitions driven

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by a train of identical programming pulses in filamentary-type memristive systems. Reference 18 reported a detailed investigation of the gradual resistive switching effect in TiN/HfO_2/TiN stacks, whose resistance was found to strongly depend on the oxygen vacancy distribution. Similarly, in Refs. 19 and 20, the controllable multilevel ability of HfO_x-based RRAM devices in terms of their resistance was demonstrated. Other recent works on gradual resistance change can be found in the literature.[21–26]

Few researchers have paid attention to the concurrent capacitance changes during the switching process.[27–30] In fact, the ac electrical characteristics of resistive switching mechanisms have not been studied in great detail yet. In Ref. 31, impedance spectroscopy measurements have been used to provide additional insights into the fundamental mechanisms of SiO_x-based resistive memories. Also, admittance memory cycles provided relevant information about the role of the two different metallic species in the Ta_2O_5-ZrO_2-based RAM devices behavior.[32] In a previous work, we have demonstrated the controlled gradual transition for both set and reset dynamics of HfO_2-based RRAM devices in terms of ac parameters.[33] Here, we present an in-depth analysis of the control of admittance intermediate states. Similarly to the current, both real (conductance) and imaginary (susceptance) components of the admittance of our samples show set and reset loops with excellent repetitiveness. Moreover, we demonstrate that the states at which a RRAM device can operate form a continuum defined by the values of bias voltage, conductance, and susceptance. Each state can be achieved by means of an adequate control of the voltage sequence previously applied.

EXPERIMENTAL

The devices under investigation are TiN/Ti/20 nm-HfO_2/W RRAMs. HfO_2 films were deposited by atomic layer deposition (ALD) at 225 °C using tetrakis(dimethylamido) hafnium and H_2O as oxidant precursors and N_2 as carrier and purge gas. The top and bottom electrodes were deposited by magnetron sputtering. The resulting structures were square cells of $5 \times 5\,\mu m^2$.

Electrical measurements were carried out by means of a semiconductor analyzer (Keithley 4200SCS), with samples put in a light-tight and electrically shielded box. The dc voltage was applied to the top electrode (TiN/Ti), with the bottom one (W) being grounded. In order to carry out the admittance parameters recording, a small signal of 30 mV rms was overlapped to the dc bias voltage. A parallel admittance model was selected which directly provides the real component value of the admittance (conductance, G) and the imaginary one (susceptance, B). The frequency varied between 20 kHz and 10 MHz. To avoid the effect of parasitic elements (series resistance or inductance due to wiring, needles, etc.), the capacitance-voltage unit (CVU) of the 4200-SCS system was configured in a four-probe measurement setup. At each electrode, one probe was used to apply and measure the voltage, while the other one sensed the current. Before measurements, a short/open calibration process to compensate potential artifacts of the experimental bench was performed. The accurateness of the calibration process was tested by employing a circuit consisting of a capacitance of 10 pF in parallel with a resistance of 100 Ω. Experimental errors were less than 0.1% in both terms throughout the entire frequency range.

RESULTS AND DISCUSSION

The electroforming process was carried out by applying a voltage of around 4 V to the pristine sample. After that, the CFs were formed and the switching process was activated. It is stated that in this kind of samples, the electric field yields oxygen vacancy clusters, which make up the CFs. In this context, we use the term oxygen vacancy as an oxide molecule in which one oxygen atom is missing. The specific value of the current compliance used during the electroforming process, 50 mA, sets the number and the size of CFs and, hence, the window opening and the effective values of the low and high resistance states. The low resistance state (ON state) was achieved by applying a voltage bias of +1.2 V, whereas the high resistance state (OFF state) was reached when applying a negative voltage of −1.6 V (see Fig. 1). Bipolar resistive-switching cycles showed excellent repetitiveness and a window between ON and OFF states of around 10 mA at −0.1 V. Each cycle was carried out by using double linear voltage ramps as follows: a positive set voltage to drive the sample to the ON state (0 V → +1.2 V → 0 V) was applied; after that, a negative reset voltage to drive the sample to the OFF state was applied (0 V → −1.6 V → 0 V). In Fig. 1, we plot loops obtained at two very different ramp speeds of 5 and 150 mV/ms. It can be observed that the loops remain unaltered in this range.

In Ref. 33, well-defined admittance loops between 0 and a positive voltage varying from +0.1 to +1.2 V (ON state) or between 0 and a negative voltage varying from −0.1 to −1.6 V (OFF state) were reported in the range 20–500 kHz. Full reset cycles departing from different initial set conditions and vice versa were recorded, so that the initial state of each loop changed, whereas the back-to-zero trajectories remained identical. This way, a set of minor switching loops associated

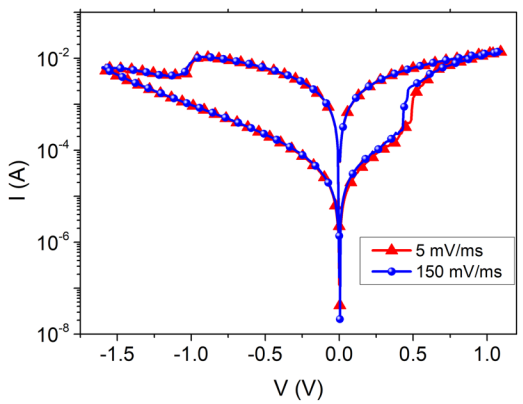

FIG. 1. Current-voltage loops of a TiN/Ti/HfO_2/W bipolar RRAM at two different voltage ramp rates: 5 and 150 mV/s. Cycles were obtained by using double linear voltage ramps: a positive set voltage to drive the sample to the ON state (0 V → +1.2 V → 0 V) was applied; after that, a negative reset voltage to drive the sample to the OFF state was applied (0 V → −1.6 V → 0 V).

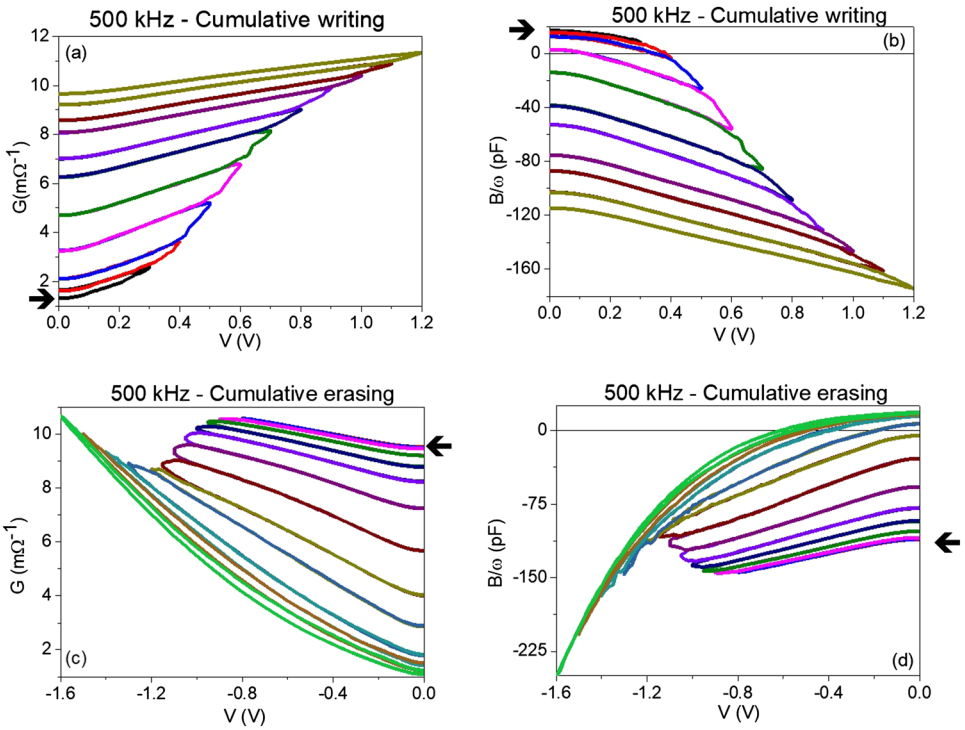

FIG. 2. Conductance and susceptance components of admittance measured at 500 kHz during cumulative writing [(a) and (b)] and erasing [(c) and (d)] operations. For cumulative writing, the sample was driven to an initial OFF state by applying a voltage of −1.6 V during 10 ms. After that, each loop of the admittance signal was obtained by applying triangular shaped bias voltage waveforms (0 V → $V_{writing}$ → 0 V), with increasing $V_{writing}$ from one loop to the next one. For cumulative erasing, the sample was driven to an initial ON state by applying a voltage of +1.2 V during 10 ms. After that, each loop of the admittance signal was obtained by applying triangular shaped bias voltage waveforms (0 V → $-V_{erasing}$ → 0 V), with increasing $V_{erasing}$ from one loop to the next one. In all cases, voltage steps of 10 mV each 10 ms were applied.

with partial transitions between the ON and the OFF states were depicted. Here, we demonstrate that it is also possible to accurately control the admittance parameters of RRAM devices during cumulative writing and erasing operations. To carry out a progressive writing process, we proceeded as follows: After taking the sample to an initial OFF state (0 V → −1.6 V → 0 V), each loop of the admittance signal was obtained by applying triangular shaped bias voltage waveforms (0 V → $V_{writing}$ → 0 V), with increasing $V_{writing}$ from one loop to the next one. Figures 2(a) and 2(b) show, respectively, the real (G) and imaginary (B/ω) components of admittance measured at 500 kHz during a cumulative writing operation. The initial state is indicated with the symbol →. This state corresponds to a full reset with a low value of the conductance and a positive value of the susceptance, which is practically equal to the geometrical capacitance of the pristine samples. It is worth pointing out that when the voltage increases from 0 V to $V_{writing}$ in one cycle, the trajectories are identical to the back-to-zero ones corresponding to the previous cycle. This means that the device remembers its state, and so each new state starts from the previous one, in a cumulative way. In other words, the maximum value of the bias voltage applied in a cycle determines the back-to-zero trajectories of the real and imaginary components of the admittance.

In a similar fashion, a progressive erasing process was carried out. The sample was first driven to the ON state (0 V → +1.2 V → 0 V), which drove the device to an initial state of full set (high conductance and negative susceptance). Then, subsequent bias voltage waveforms consisting of 0 V → V_{erase} → 0 V double ramps were applied. The value of $|V_{erase}|$ was then increased from cycle to cycle. Figures 2(c) and 2(d) show, respectively, the real (G) and imaginary (B/ω) components of the admittance measured at 500 kHz during a cumulative wiping out operation. The initial state is indicated with the symbol →. The voltage changes from 0 V to V_{erase} in one cycle, and the trajectories are identical to the back-to-zero ones found at the previous cycle. As observed in the cumulative writing process, the device remembers its state, so each new state starts from the previous one in a cumulative way. In summary, for both writing and erasing operations, excellent control and repetitiveness are achieved. Similar results are obtained in the whole range of experimental frequencies. It is worth noting in Figs. 2(b) and 2(d) that susceptance values are negative in the ON state. This indicates the existence of an inductive-like component.[33,34] Once the CFs are created after the initial forming step, the device can be modeled as a capacitance in parallel with a resistance in series with an inductance.[30,33,34]

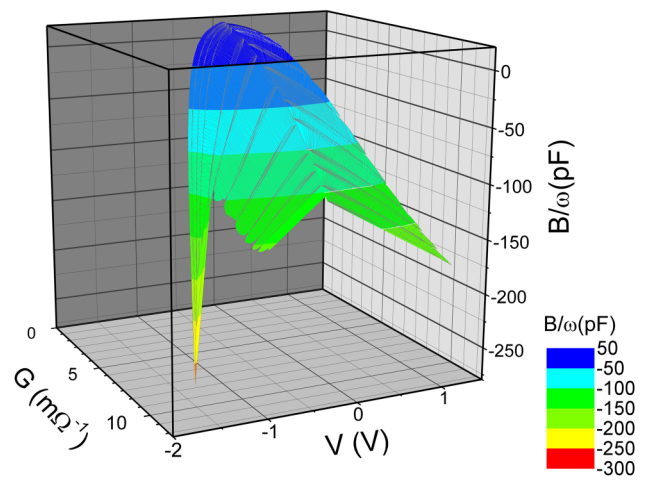

FIG. 3. Three-dimensional plot of all accessible voltage, conductance, and susceptance states of a TiN/Ti/HfO_2/W bipolar RRAM. This memory map has been obtained from the results plotted in Fig. 2.

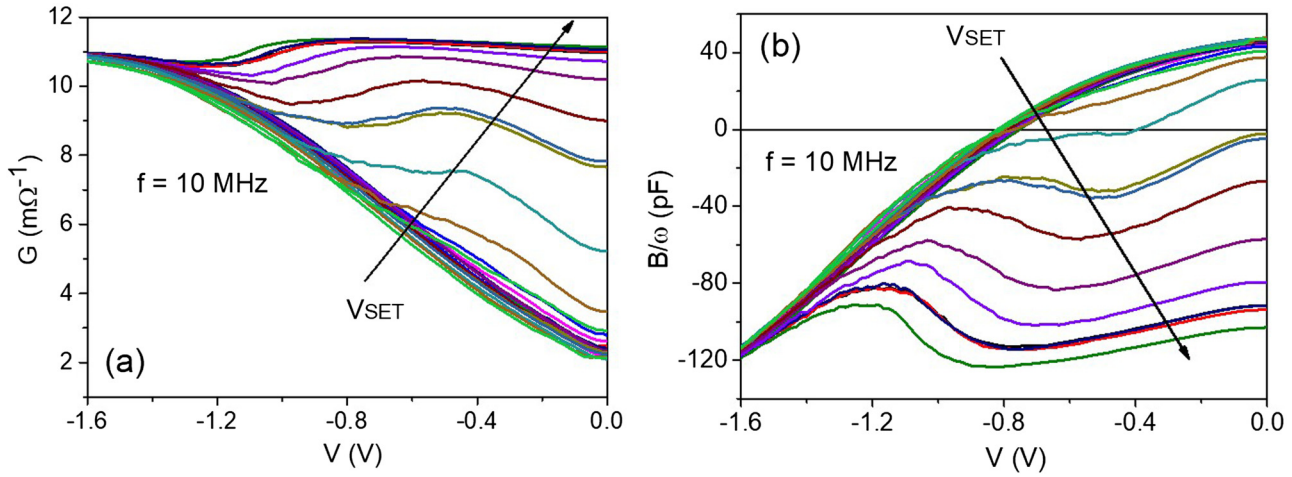

FIG. 4. Full reset loops of conductance (a) and susceptance (b) at 10 MHz after different partial set initial conditions. Each loop was obtained by applying a full reset sequence: V = 0 V → V = −1.6 V → V = 0 V with voltage steps of 10 mV each 10 ms. Before recording each loop, different values of V_{set} were applied during 10 ms. V_{set} was varied from 0.3 to 1.2 V in 0.1 V steps.

The erase process needs values of at least −0.9 V to begin. For lower values of $|V_{erase}|$, the sample remains at the low resistance state and no loops are observed. Therefore, the reset process, consisting of the dilution of CFs, needs that the applied voltage overcome a certain threshold value. The process mainly occurs at the voltages ranging from −1 to −1.2 V, and the back-to-zero trajectories only depend on the maximum applied voltage value. On the contrary, the writing process takes place in almost the entire voltage range: [0.3, 1.2] V. Therefore, it is possible to obtain different values of the real and imaginary parts of the admittance of the RRAM devices in a very well controlled manner. These values are a function of the recent history of the sample biasing. In terms of applicability, this allows to accurately modulate the in-phase and quadrature components of the ac current of RRAM by applying properly defined bias voltage sequences.

From the experimental results of Fig. 2, a three-dimensional plot of all accessible states to the RRAM devices used in this study has been built (Fig. 3). The plotted surface represents the available values of dc voltage, conductance, and susceptance of the device under study. The colors are an eye-guide to distinguish the susceptance value range. Other values outside this surface cannot be reached. Each point in this plot contains information about the values of the set and reset voltages previously applied to the cell, i.e., each point treasures two past events. The memory map shown here has been reproduced from device to device with no remarkable changes. Finally, the memory states form a continuum and can be used for analog applications such as neuronal networks, approximate computing, etc. As for the effect of technological parameters, we have not observed noticeable changes in the memory map when varying the device area or the film thickness. This fact probes whether the area of the conductive filaments has nanometric dimensions and whether the changes from the ON to the OFF state involve very narrow regions of the conductive filament itself.

The good behavior and control remain even at frequency values of 10 MHz, as it is shown in Fig. 4 for reset loops. In this case, we carried out full reset cycles departing from different initial set conditions. Each loop was obtained by applying a full reset sequence: V = 0 V → V = −1.6 V → V = 0 V, just after different values of positive set voltages, V_{SET}. The value of V_{SET} determines the initial values of the conductance and susceptance of each cycle. As V_{SET} increases, the set process becomes more effective, yielding higher values of the conductance and more negative values of the susceptance at the beginning of each new cycle. Because full reset is achieved in all cases, the back-to-zero trajectories are identical for all curves.

In Fig. 5, return-to-zero (RTZ) pulsed voltages instead of ramp voltages are applied. To control the set process, square pulses (0 V during 2.5 s, V_{SET} V during 2.5 s) with V_{SET}: 0.1, 0.2, 0.3,…,1.1 V were applied. We have chosen pulse duration of 2.5 s to ensure that partial set or reset saturates for each applied voltage value. At room temperature, dependencies are only observed for very short pulsed times in the range of milliseconds. After each set pulse, G and B/ω values are recorded at 0 V. In a similar fashion, to control the reset process, square pulses (0 V during 2.5 s, V_{RESET} V during 2.5 s) with V_{RESET}: −0.1, −0.2, −0.3, …, −1.3 V were applied. The envelope points of the curves on the left panels [Figs. 5(a) and 5(c)] are the admittance parameters measured when each voltage pulse is applied, whereas the points located at the V = 0 axis correspond to the admittance values measured at 0 V, between two consecutive voltage pulses. In the right panels [Figs. 5(b) and 5(d)], the values measured at 0 V as a function of the previous pulse voltage value (programming voltage) are plotted. We label these plots as zero-voltage memory maps. Clear differences between the set and reset processes are observed, with the reset transition being much more abrupt than the set one. The intermediate states can be controlled in the whole range of positive $V_{program}$ values between 0 and +1.1 V. However, in the reset process, the control of intermediate states is restricted to $V_{program}$ values in the range [−0.9, −1-1] V. Hence, the set and reset processes are asymmetrical to some extent. In fact, a positive voltage must be applied to the top electrode to form the CFs. In this way, oxygen anions are

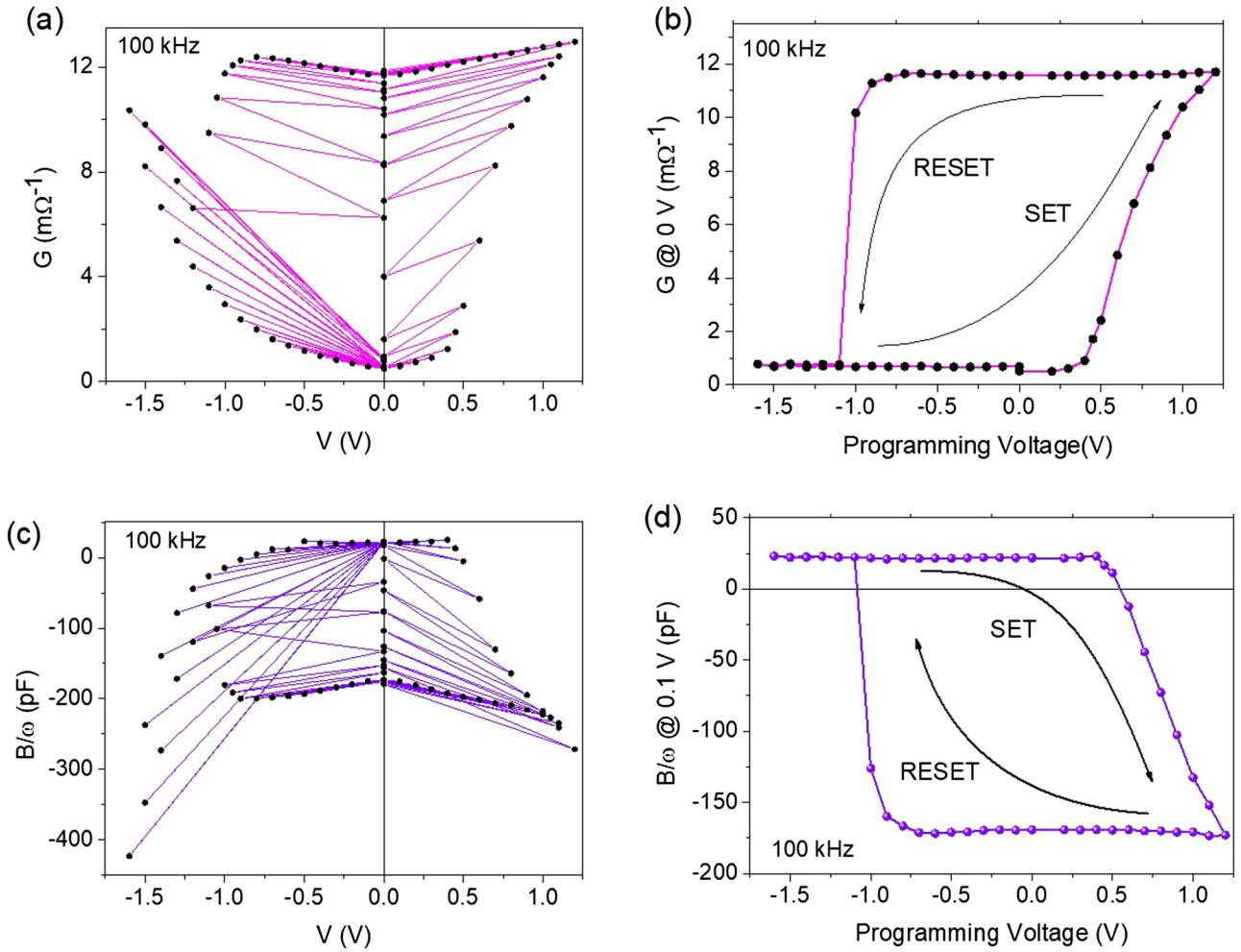

FIG. 5. Left panels are the experimental values of conductance (a) and susceptance (c) for RTZ pulsed voltages. Right panels are the zero-voltage memory maps: values of conductance (b) and susceptance (d) measured at 0 V as a function of the previous pulse voltage value (programming voltage). Square pulses (0 V during 2.5 s, programming voltage during 2.5 s). Programming voltage was varied in 0.1 V steps, first increasing from 0 to a maximum value 1.1 V and then decreasing up to a minimum value of −1.6 V and finally returning to 0 V. After each set pulse, G and B/ω values are recorded at 0 V.

gradually attracted from the dielectric layer to the top electrode, creating a conductive path of oxygen vacancies between the top and bottom electrodes. On the other hand, in the reset transition, when a negative enough voltage is applied to the top electrode, oxygen anions previously cumulated there are suddenly repelled to come back to their positions into the dielectric layer, and so the oxygen-vacancies-built-CFs are quickly broken. To sum up, when

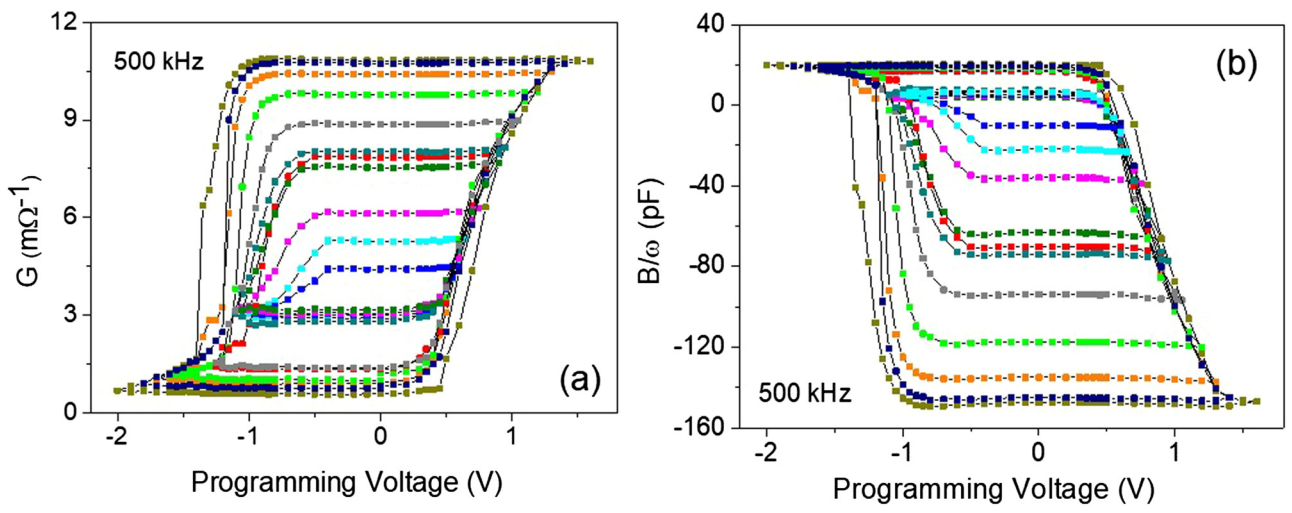

FIG. 6. Intermediate zero-voltage memory maps obtained in an analogous way as in Fig. 5 but changing the maximum positive and negative values of the programming voltage in order to obtain intermediate set and reset states.

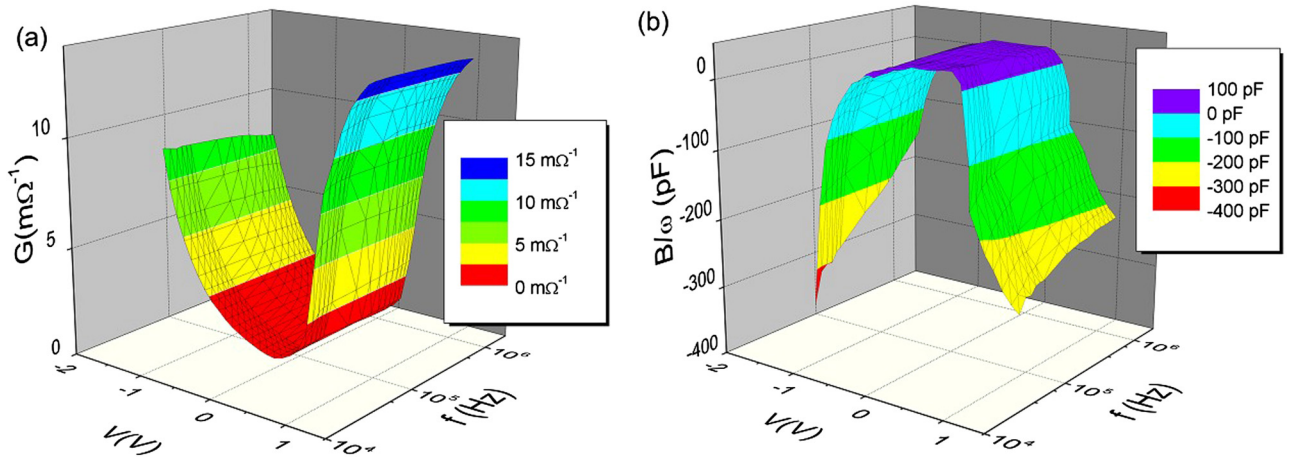

FIG. 7. Surface plots showing the voltage and frequency dependencies of conductance (a) and susceptance (b) obtained after total reset at frequencies varying between 10 kHz and 2 MHz. These plots were obtained by first driving the samples to full reset (−1.6 V) and then increasing the voltage up to +1.2 V in steps of 10 mV each 10 ms.

the dilution process begins, the current paths suddenly disappear, whereas their reconstruction takes place in a gradual manner.

Intermediate states can also be displayed in good resolution memory maps, as it is shown in Fig. 6 for 500 kHz. Similar results are obtained in the whole range of experimental frequencies. The intermediate loops are built by changing the height of the maximum positive and negative voltage pulses so that the set and reset processes are not complete. In other words, internal loops represent the memory state when it is partially read and/or written. Interestingly, the reset process in the inner loops is more gradual and departs at lower voltages than in the external ones. Chemical reactions involved in the filament dilution seem to be enhanced when the current level increases, so they would become faster.

The negative value of the imaginary part of the admittance, usually known as negative capacitance (NC), has been observed in a variety of electronic devices. The microscopic origin of this behavior is, in general, not well established for each particular case. However, in a very interesting paper, Ershov *et al.*[35] established a general principle behind the NC phenomena to all cases: the origin of the NC is related to the non-monotonic or positive-valued behavior of the time-derivative of transient current upon application of a voltage step. They probe the validity of this principle in the case of quantum well infrared photodetectors (QWIP) which exhibit big values of negative capacitance. In these devices, NC is due to the non-equilibrium transient currents caused by the injection properties of the contact barrier and the inertia of the recharging process on quantum wells (QW). Conductive filaments in the bipolar RRAM studied in this work consist of oxygen vacancy clusters which form conductive paths connecting the top and bottom electrodes of the MIM devices. Oxygen vacancies are electron traps and can be seen as quantum wells in which electron capture and emission occur. These mechanisms yield to inertial recharging

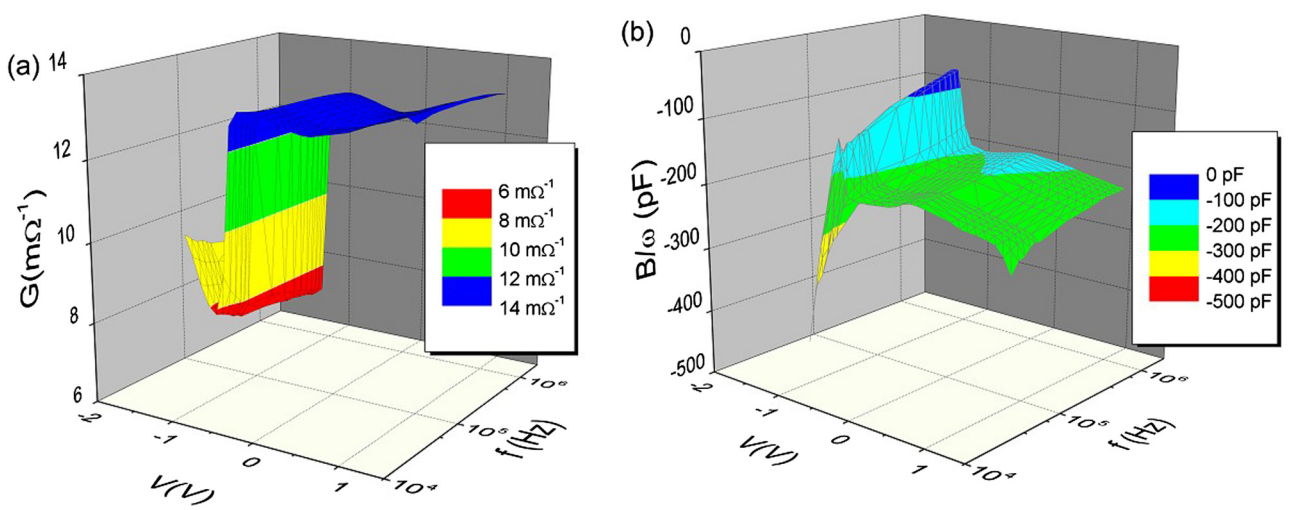

FIG. 8. Surface plots showing the voltage and frequency dependencies of conductance (a) and susceptance (b) obtained after total set at frequencies varying between 10 kHz and 2 MHz. These plots were obtained by first driving the samples to total set (+1.2 V) and then decreasing the voltage to −1.6 V in steps of 10 mV each 10 ms.

process, similar to the ones described in Ref. 35, which induce negative values of the reactive component of the conduction current that achieves values larger than the displacement term.

To obtain a more complete perspective of the admittance behavior of RRAM, we have obtained three dimensional spectra of conductance and susceptance as a function of voltage and frequency in the range 10 kHz to 200 MHz. According to the literature, in this frequency, range dipolar relaxation processes are dominant in the response of the dielectric to the electric field. We have constructed these spectra for the cases in which total reset (Fig. 7) or total set (Fig. 8) were established before varying the voltage from −1.6 to +1.2 V at each frequency. It is important to point here that whereas in Fig. 6, we plot the G and B/ω values at 0 V as a function of the previous programming voltage, in Figs. 7 and 8, the plotted data are those measured at the bias voltage V itself. In both figures, we can see that the conductance term is practically independent of the frequency and only depends on the voltage applied. As for the susceptance term (B/ω), it can be seen that it does not depend on the frequency for low voltages. In contrast, important variations of B/ω occur for high positive and negative voltages, where the dc current levels are more important: the negative capacitance decreases with frequency. Moreover, the absolute value of the negative capacitance is higher for these higher current regimes. Therefore, there is a clear correlation between negative capacitance behavior and conduction regimes, thus confirming the theory of Ref. 35.

CONCLUSIONS

The conductance and susceptance of TiN/Ti/20 nm-HfO_2/W devices showing bipolar resistive switching behavior have been studied in depth. This study reveals that very good repetitiveness and excellent control of intermediate states during cumulative writing and erasing processes are achieved. This can be performed in a wide range of frequencies. A continuum of intermediate states is obtained by applying an adequate voltage sequence. Conductance and susceptance at each state are a function of the set and/or reset voltage values previously applied. Three dimensional plots of the accessible states to the memory cells were built from the experimental results. Pulsed measurements provided memory maps by testing the device at V = 0 V, without static power consumption. The intermediate states in this kind of representation appear as the transition path between two clearly distinguished values, corresponding to the ON and OFF states, which remain essentially constant. Relevant information about the inherent physical phenomena of set and reset transitions can be obtained by analyzing the rise and fall of edge shapes, both for the nominal and intermediate memory states. Another important advantage of carrying on the RRAM device study in terms of admittance parameter is that some information can be extracted from the sign of the in-quadrature component. In fact, negative values of the susceptance point to an inductive-like behavior of conductive filaments, which in turn is related to the physical nature of the underlying processes. Conductive filaments consist of oxygen vacancy clusters which behave like quantum wells. The inertia of the emission and capture process occurring at the oxygen vacancies is on the basis of the microscopic nature of the negative values of the imaginary part of the admittance.

ACKNOWLEDGMENTS

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