Rapid Thermal Process Driven Intra-Die Device Variations

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Intra-die device variation due to pattern layout effects associated with the development of ultra-fast annealing processes is one of the major scaling challenges for advanced CMOS devices. In this paper, we show that an excellent and universal correlation can be established between on-die device variation and a new reflectance characterization technique with sufficient resolution, and this approach can be extended to virtually any structure pattern. In addition, we conducted simulation of thermal annealing effect on 2D doping profile by considering effects of temperature sensitivity, reflectivity, active dopant fraction, and the results show that the observed on-die variation was caused mainly by using a rapid thermal annealing (RTA) process rather than by flash annealing (FLA). We further concluded that pattern-induced device variation is mainly due to the redistribution of the dopants, instead of from a dopant activation. To mitigate the pattern loading effect from thermal annealing, we employed a light absorbing layer to eliminate the within-die reflectivity variation, and successfully reduced electrical on-die variation by 50%.

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Rapid advancements in accelerated computing platforms such as in CPUs, GPUs, FPGAs, and heterogeneous chip platforms that support AI acceleration and high-speed networks, have pushed chip integration to an unprecedented level, leading to greater die area to meet application requirements[1]. It is well known that for a given process technology, thermal process-related variation issues get worse as die size increases. Larger die size reduces overall wafer yield compared to smaller size die and variation issues are closely related to thermal process[2,3]. When the die size is scaled up to a centimeter level, suppressing the within-die variability caused by thermal annealing becomes a challenge for fabricating CMOS transistors.

Rapid annealing in the semiconductor industry can be divided into the following categories depending on the thermal energy source and annealing dwell time: tungsten halogen lamps in rapid thermal annealing (RTA), Xenon arc lamps in flash lamp annealing (FLA)[4,5], diode lasers in dynamic surface annealing (DSA)[6], and excimer laser in nanosecond annealing (NSA)[7,8]. These different rapid annealing processes can achieve annealing dwell times in seconds, milliseconds, microseconds, and nanoseconds, respectively. The development of thermal budget reduction technique aims to maximize dopant activation while maintaining a diffusion-less dopant distribution[9,10]. However, since peak wafer temperatures are typically much lower than heat source temperatures, wafers will not be in thermal equilibrium with the radiant heat source which makes the nature of the wafer's heating cycle dependent on its optical properties[11-13]. When the variation within a die occurs on a length scale larger than the lateral thermal diffusion length in the silicon, this could lead to spatial temperature non-uniformity and could result in an intra-die electrical variation. The spatial non-uniformity caused by rapid annealing suggests that a larger die area usually suffers more from a pattern density effect[14-15].

Early theoretical or experimental research work related to pattern effects was mainly limited to a specific pattern layout, and it was difficult to apply it to a variety of pattern layouts. It is well known that

pattern-dependent heating within a die is related to the patterning topography, which leads to changes in local optical properties, resulting in differences in energy absorption and thermal emission[11,13]. Pattern structures in modern CMOS device architectures arises from features such as polysilicon gate and fin channel architectures, that exhibit trench structures with different aspect ratios[16,17]. It is difficult to use theoretical approaches for modelling effects, because they can usually only be applied to specific pattern structures[18]. Other experimental research uses special pattern designs[19,20] to measure and model pattern effects but the results are specific to a particular layout. Therefore, it is imperative to develop a general physical methodology to estimate the expected on-die device variations for any given layout design. In our quest to develop a universal application, we used optical experimental methods to detect the effective emissivity without being restricted by any pattern structures. The two-dimensional reflectivity characterization shown in Fig. 1(a) provides the spatial resolution required to capture and predict pattern effects caused by radiation heating annealing. Furthermore, we propose to introduce the addition of a light absorbing layer to solve the pattern variability effect problem and at the same time to verify the reliability and correctness of the proposed reflectivity measurement methodology. Our results show that electrical on-die variation can be significantly improved if a light absorbing layer is incorporated before annealing because it can counteract reflectivity variations. We used high-density two-dimensional reflectivity measurements to verify the results.

The quantification of on-die device variation is the primary challenge in studying the patterning effects caused by source-drain thermal annealing done by a combination of RTA and FLA. To characterize the variation of on-die devices, we rely on a simple ring oscillator (RO) circuit layout using an odd number of inverters sequentially cascaded in a feedback loop evenly distributed on the die. Since the output frequency of a ring oscillator consisting of CMOS inverters is sensitive to process variations inherent in the die[21-23], testing each RO frequency in sequence provides a succinct signature of the RO's circuit speed wherever the RO is distributed on the die. The test frequency of RO represents the net sum of all process

variations, whatever their sources are random or systematic, and can be expressed as $f_{test}=1/(n \times 2T)$, where f_{test} is the test frequency, T is the average transistor gate delay time characterizing RO circuit speed, n is an odd number and is the number of stages of the ring oscillator[24]. To obtain the circuit speed of RO_i (i=1 - N) at all different locations within the die, we used the scan chain circuit design[24,25] shown in Figure 1(b), so that the RO located on the die can be sequentially triggered once by the scan clock during sampling, and the individual output frequency of the RO is then measured by a frequency counter and recorded in memory. This enables any local RO circuit speed information to be available within the die, allowing on-die device variation to be calculated. Fig 2(a) shows an example where a pattern effect was considered and where there was an electrical on-die variation in a CMOS circuit. In this example, 600 special CMOS sub-circuits were designed and evenly distributed in a custom-made chip to evaluate the influence of a pattern effect on the distribution of the circuit performance within the die. In our layout with a chip area of 2.5cm x 2.4cm size, the observed on-die variation was as much as 17%. It was observed that for different patterns, the different pattern densities induced different degrees of on-die variations. As shown in Fig 2(a) the concentric and progressive device performance changes indicate that this could be the result of thermal inhomogeneities caused by a pattern effect. Since the non-uniformity is driven by optical effects, a reflectivity mapping approach was proposed to outline the possible correlation with temperature inhomogeneities and to explain the electrical variation within the die. We can adopt this to optimize the layout design in advance so as to reduce the pattern effect or use it to evaluate any possible process solutions to solve observed on-die variations.

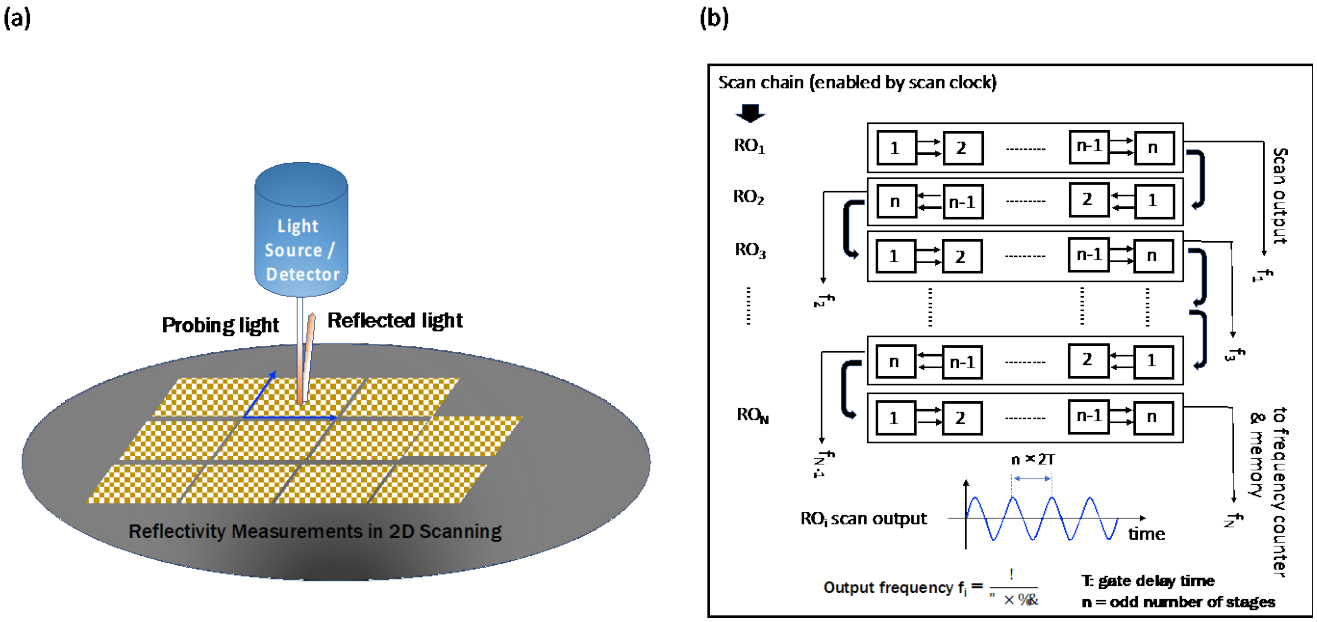

Fig. 1(a). Optical set-up for 2D reflectivity scan measurement where the light source is incident on the die surface area and reflected to the detector module (the 3μm light spot size followed the 2-dimensional scan path). The 600 sub-circuits were distributed throughout the die area and used to determine electrical on-die variations. Fig. 2(b). Electrical set-up for sequential characterization of the speed of all RO circuits in the die, the RO circuits evenly distributed in the die are designed with scan chains to sequentially enable one RO at a time during the sampling period, during which the RO frequency from the scan output is measured and stored in the memory system using a frequency counter. From the stored RO frequency, on-die variation information of circuit speed can be calculated.

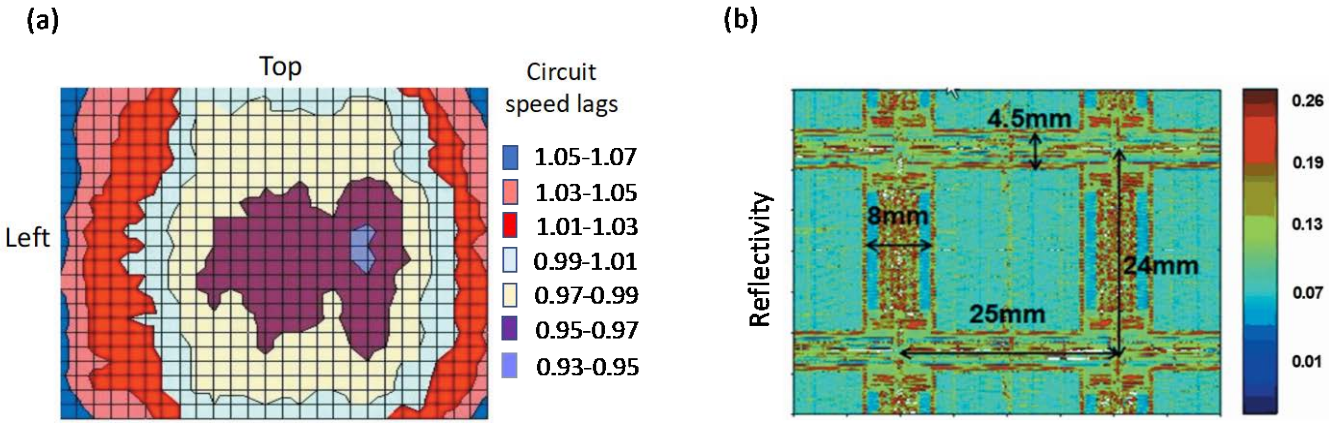

Fig. 2(a). Circuit speed on-die variation map. The larger speed lag index represents a slower circuit speed. This map reveals a somewhat concentric non-uniformity profile where the zones at the left and right die edges show steep changes in the speed lag index. Fig. 2(b). 2D reflectivity mapping of the entire dice. A higher reflectivity (~0.22) can be seen at the left edge region of the chip while a lower reflectivity (~0.08) can be seen at the center region of the chip.

High density wafer surface reflectivity mapping can be used to directly identify patterned features which can then be used to predict non-uniform temperature distributions during RTA or FLA annealing. In many cases, localized temperature inhomogeneities tend to be associated with corresponding reflectivity variations[26] due to pattern topography and optical properties of thin film stacks on the wafer surface. Therefore, once the local reflectivity variation can be measured and determined, it is possible to evaluate the pattern loading effect for any wafer pattern. To achieve this goal, the optical measurement set-up needs to provide spatial resolution and sensitivity to resolve relevant local reflectivity changes. The spatial resolution must be smaller than the lateral thermal diffusion length in silicon, which is typically in an order of 100μm for FLA annealing and around 1mm for RTA annealing[19,27]. Ideally, the measurement light source spectrum should match the heat source spectrum so that the wavelength-dependent optical effects, such as refraction, diffraction and interference can be accurately captured. The tungsten-halogen lamps used in RTA annealing produces a continuous spectrum of light where the wavelength ranges from near-ultraviolet (~300nm) to mid-infrared (~4um), while the arc lamps used in the FLA annealing typically produce a spectrum from 250 to 750nm[28]. In practice, it can be difficult to find a probing light source which perfectly matches the heating light source. In our experimental work, a broadband 250-850nm light source was selected as the probing light source to measure the wafer surface reflectivity at room temperature. A xenon arc lamp was preferred because it contains not only many ultraviolet bands but also a large band of visible light and some infrared bands. This spectrum covers most wavelengths used in modern state-of-the-art annealing techniques such as RTA (visible and IR), FLA (250-750nm), DSA (810nm), or NSA (308nm or 532nm). In reflectivity optics with monochromatic gratings, it can select a desired single wavelength from a broadband spectral light source to simulate the reflectivity behavior of DSA and NSA laser annealing. According to Wien's law, a black-body radiation curve for different temperatures has peaks at different wavelengths which are inversely proportional to temperature. The peak temperature of the W-halogen radiation used for annealing is higher than 3200 K as its maximum emission

occurs at a wavelength close to the visible range. Depending on the CMOS technology node, the patterned device wafer may have pre-amorphized ion implantation completed in the source-drain regions or it may have deposited doped-epitaxial source-drain prior to completing the dopant activation anneal. In either case, the light energy absorption bands are mainly located between 300nm, and 750nm[29-30]. Furthermore, without dopant-activated annealing[31], the Si substrate cannot provide free carrier concentrations above 2×10^{20} cm^{-3}. According to Lojek[32], the reflectivity exhibits a strong spectral wavelength dependence only when the free carrier concentration in Si is as high as 1×10^{21} cm^{-3}. In our case, the theoretical spectral dependence of reflectivity is expected to be limited as the free carrier concentration is well below this level. Therefore, an arc lamp is a reasonable compromise that can be used as a probing beam source to approximate the absorption and reflection from pattern structure when whatever RTA, FLA, DSA, and NSA annealing is used. The strong intensity advantage of xenon arc lamps also allows the measurement spot to be focused at a μm length scale. The spot size of the detection beam was chosen to be 3μm, which is significantly smaller than the characteristic thermal diffusion length of the RTA and millisecond annealing in silicon. This ensured that any critical local non-uniformity will be captured by the probing light. Finally, the step distance (40 μm) between the two detection points was set to be larger than the spot size but smaller than the characteristic thermal diffusion length. These settings provided enough spatial resolution to study pattern effects during the annealing processes.

Line scan measurements and 2D mapping were performed over a unit die on a wafer with die dimension of 2cm x 2cm. Identical scans were repeated over multiple dies on the wafer at different locations and we found no significant differences in the line scan results. Within each die, 2D scans were performed to characterize the within-die reflectivity variations. Fig. 2(b) shows a 2D profile map across a full die. In the 2D profile map, a steep reflectivity changes were observed around the right and left edge portions of the die, while no significant reflectivity variations were observed in the center zone of the die. We also validated a single wavelength (508 nm) but showed no significant difference on the 2D map.

Based on the 2D scan results, the die reflectivity map was divided into two zones. The inner zone was of a 19.5mm x17mm size with low reflectivity around 0.08, while the outer zone which surrounded the inner zone possessed a higher reflectivity of around 0.22. Both the inner zone and outer zone were larger than the characteristic thermal diffusion length in silicon for RTA annealing and much larger than that for FLA annealing. As a result, the temperature differences due to the pattern effect could not be smoothed out through thermal diffusion. The outer zone had a lower temperature than the inner zone due to higher reflectivity in the outer zone and a thermal gradient was found between the inner zone and outer zone. The 2D reflectivity map showed good correlation with the electrical on-die variations. Because RTA annealing and FLA annealing are used together to provide the desired dopant activation and dopant distribution at the source-drain junction formation, we need to understand whether RTA or FLA dominates the pattern-induced non-uniformity effects.

We used the information from the 2D reflectivity map, to estimate the temperature effect caused by the change in the reflectivity of the substrate during FLA annealing. Referring to the work of Habuka et al[33], every 0.1 change in reflectivity results in a 100°C change in temperature. Therefore, in our example, the observed change in chip reflectivity of 0.14 resulted in a change in FLA temperature of approximately 140°C. To assess the possible impact of this temperature change on device performance, we used kinetic Monte Carlo (KMC) simulations and the model adopted by Aboy et al.[34] to simulate boron diffusion and activation in pre-amorphized FINFETs. The fin structure and the simulation box showing the 3D dimensions of the fin are depicted in Figure. 3. The ion implantation conditions used in simulation were 10 keV Ge 1 x 10^{14} cm^{-2} followed by 1 keV B 7.5 x 10^{15} cm^{-2}. As shown in Figure 4(a), the variation in active boron fraction is less than 3% even over a wide temperature range from 1100 to 1250 °C across a target temperature of 1150 °C. Dopant activation, which is almost insensitive to the annealing temperature, is strongly related to the actual temperature at which solid-phase epitaxy regrowth (SPER) occurs[35]. In our work, all simulations start at the same activation level as SPER has occurred before the temperature

peak has been reached. The additional thermal budged in the 1100-1250°C range FLASH anneal does not have much effect on activation[36]. Additionally, while FLA annealing is known as a diffusion-less thermal annealing, we performed simulations of a 2D dopant distribution under a FinFET transistor structure to verify how the dopant distribution in the gate-source/drain overlap region varied with the annealing temperature. The results in Fig. 4(b)-(d) show an insignificant change in the dopant profile of the gate-source/drain overlap over the annealing temperature from 1100°C to 1250°C. Obviously, neither dopant activation nor dopant distribution in FLA annealing can be used to explain the large variation in the circuit performance we observed. To find the root cause, we considered a possible effect from RTA spike annealing, as it was also used in conjunction with FLA annealing for the source and drain dopant activation.

When compared to FLA annealing which utilizes a fast ramp up and cool down with a millisecond dwell time to boost dopant activation, RTA spike annealing is used to provide the desired dopant profile and moderate dopant activation by using a longer dwell time at peak temperature. The RTA step, which maintains the peak temperature for around 1.5 seconds, creates a doping diffusion profile with sufficient source-drain overlap with the transistor channel. We performed similar 2D boron dopant distribution simulations for the same FinFET structure but at different RTA spike annealing temperatures. As shown in Fig. 5, at 910°C, the gate-source/drain overlap was negligible, but as the temperature increased to 970°C, more overlap was observed. It is widely accepted that an optimal gate-source/drain overlap has a decisive influence on the driving current of CMOS transistors[37-39], as the sensitivity of extremely scaled CMOS devices can reach a sub-nanometer level[37]. Therefore, pattern effects caused by RTA annealing are more likely the cause of observed on-die electrical variations in CMOS devices.

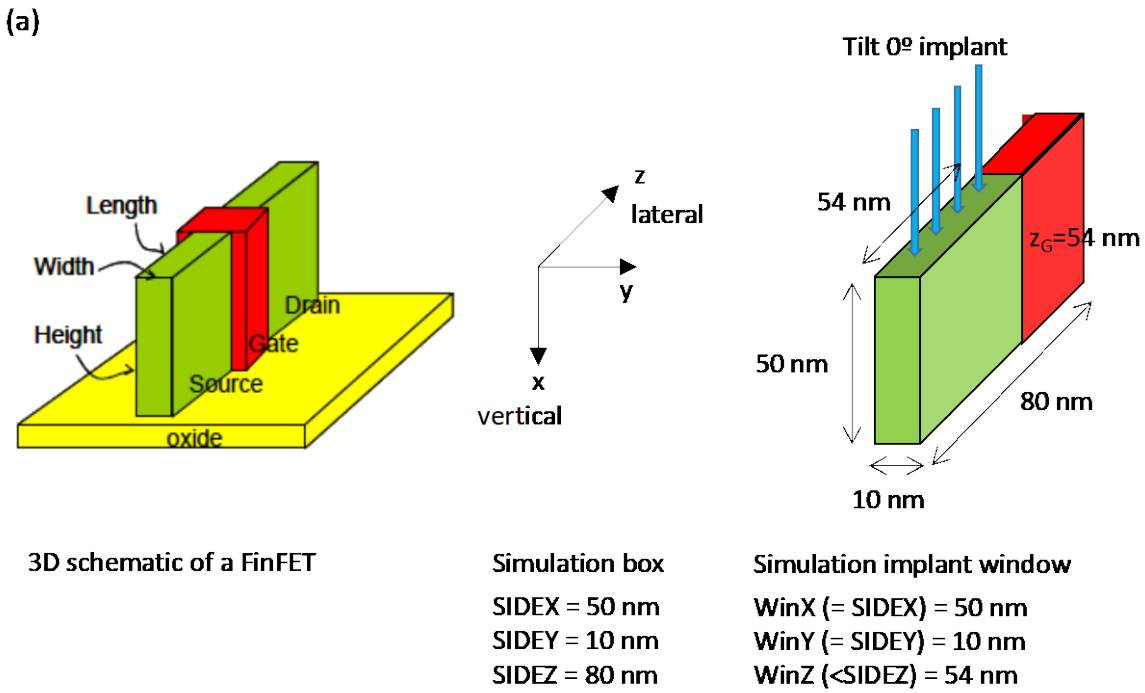

Figure. 3.(a). 3D schematic of a FinFET. Figure 3. (b) Simulation box showing the 3D dimensions of the Fin architecture used in the KMC simulation, which was used to study the dopant profile after ion implantation and annealing of FLA and RTA at different temperatures.

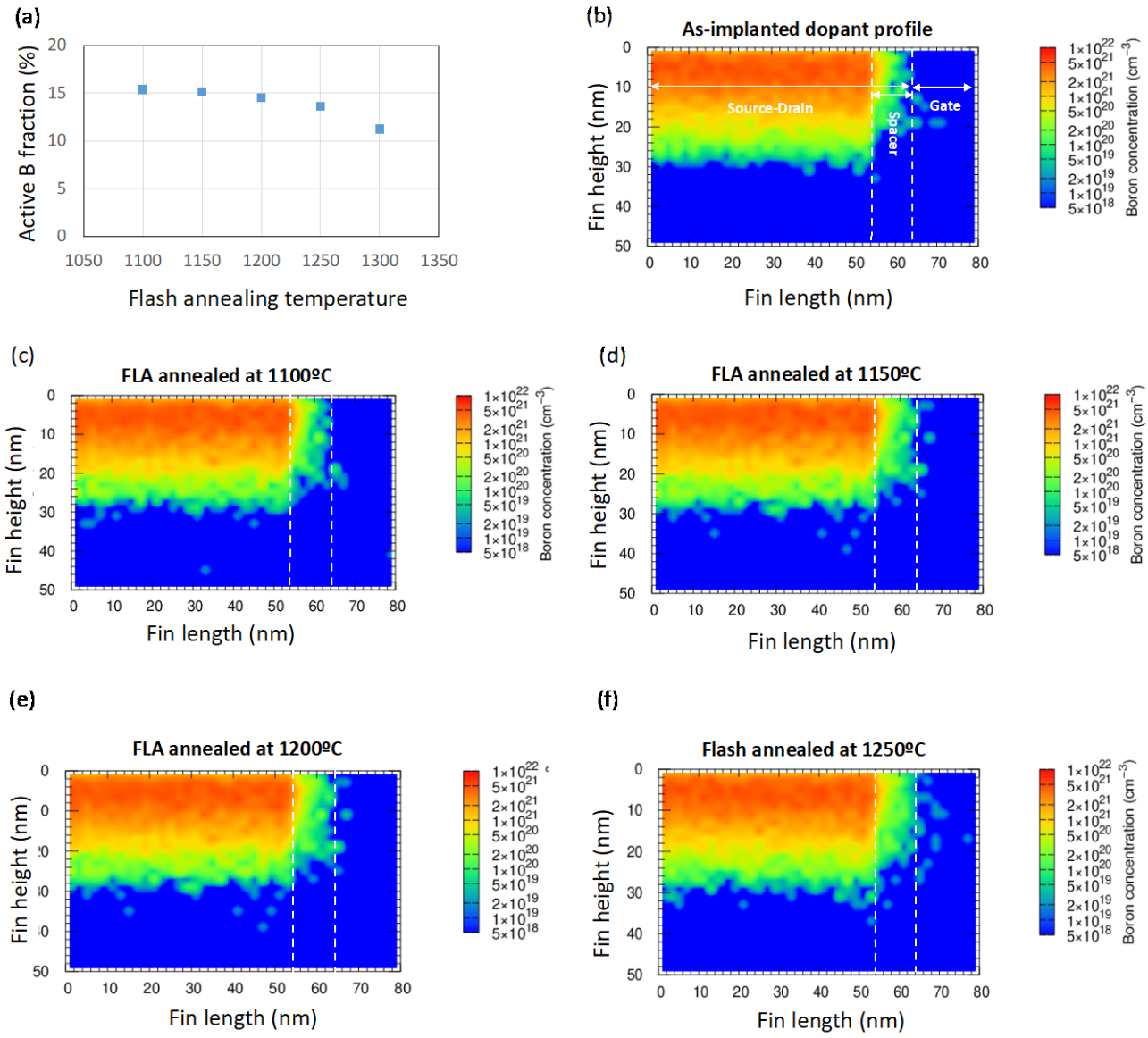

Fig. 4.(a). Sensitivity of the boron active fraction to FLA temperature. A 14% change in reflectivity results in a temperature change of 140°C, which does not significantly alter the active boron fraction over the annealing temperature range of 1100-1250°C. Fig. 4. (b) - (f). Simulation of 2D dopant distribution in FinFET source and drain before and after FLA annealing. The dopant profile of the ion implantation was produced by the silicon amorphization implantation of germanium at 10keV and 10^{14} cm^{-2}, followed by 1keV and 7.5 x 10^{15} cm^{-2} boron implants. The gate-source/drain underlap did not change significantly over a wide FLA activation temperature range from 1100°C to 1250°C.

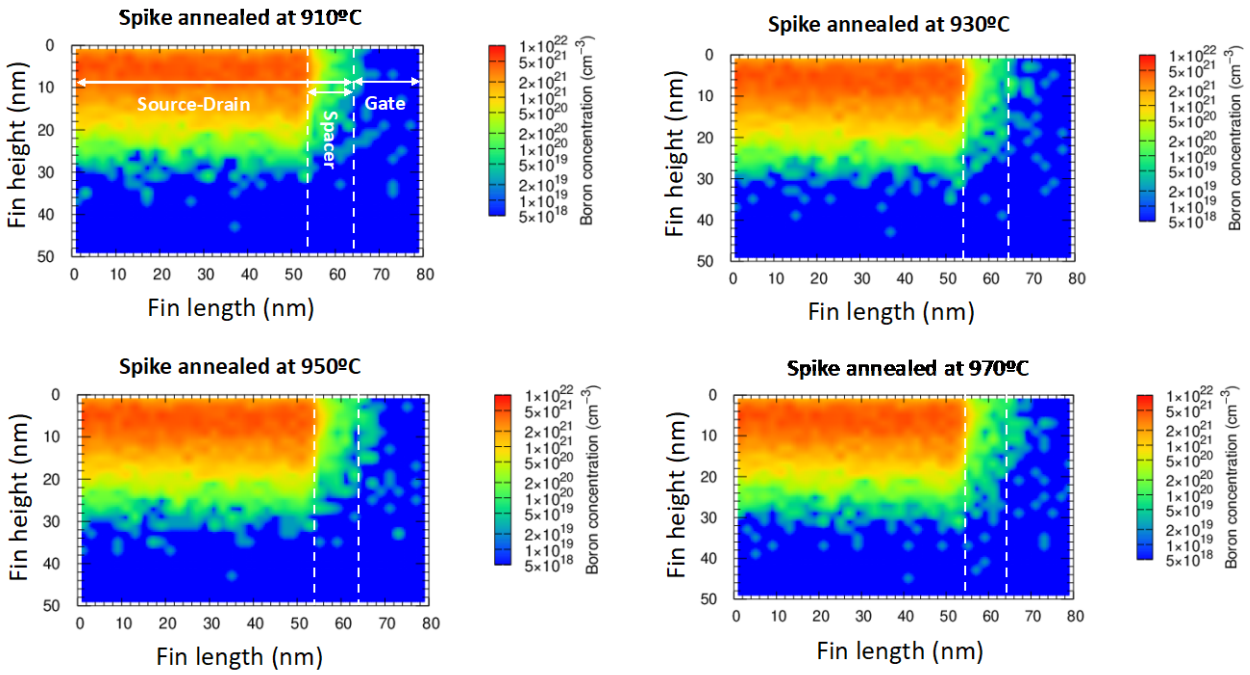

Fig. 5. Simulation of 2D dopant distribution in a FinFET source and drain by ion implantation and annealing. Implantation was done using pre-amorphized implantation at 10keV, 10^{14} cm^{-2}, followed by boron implantation at 1keV and 7.5 x $10^{15}cm^{-2}$. Dopant activation was performed by spike annealing at various temperatures from 910°C to 970°C. Dopant profile in the gate-source/drain overlap region increased with RTA spike annealing temperature and showed a significant overlap at temperatures above 950°C. An optimal overlap between the gate source/drain was critical for the transistor current drive.

To confirm the influence of a reflectivity variation on temperature uniformity during RTA annealing, we deposited an anti-reflective (AR) absorber layer on the substrate to obtain uniform heat absorption. The AR layer is an amorphous carbon layer deposited by plasma enhanced chemical vapor deposition (PECVD) containing a gas mixture of carbon source propylene C_3H_6 and carrier gas[40]. The PECVD RF plasma source was operated at the following processing conditions: 400° C. 10 Torr, 1000 watts RF power at 13.56 MHz, 380 sccm C_3H_6. As an anti-reflection coating, this layer scheme is designed to effectively absorb the incident electromagnetic radiation generated by the annealing tool. To solve the pattern effect issue, the basic requirement of the absorption layer was that its reflectivity was no longer affected by the background reflection of the substrate. The AR absorption layer of 100nm to 250nm thickness was deposited on the silicon substrate to help select the optimum thickness so that the reflectivity was no longer sensitive to the layer thickness. As shown in Fig. 6(a), when the thickness of the AR layer covering Si is greater than 200 nm, the reflectivity of Si decreases effectively and stays around 0.1. To apply this method

to patterned wafers, the extra thickness of the gap-filling must be considered, and after comprehensive consideration, the thickness of the AR layer was finally increased to 400nm. The deposition thickness and gap fill performance were verified by transmission electron microscopy. Prior to RTA annealing for the source-drain junction formation, the on-die reflectivity evaluation was performed on the wafers with and without the AR layer. We used line scan reflectivity to scan along the area of the maximum reflectivity change close to the die-to-die boundary to verify the effectiveness of the absorber. It can be seen from the comparison of reflectivity line scans in Figs. 6(a) and (b) that the 400nm AR layer deposited on the patterned wafer effectively suppressed local reflectivity changes. As a result, the device circuit speed variation within a die was reduced from 16% to about 9%, which was a nearly 50% improvement. As indicated earlier, the local reflectivity variation region in the original patterned wafer was about 4mm around the edge of the die. It matched the circuit speed lag map with a concentric shape as seen in Fig. 7(a), from a value of 0.85 in the inner zone to 1.1 in the outer zone. A large speed lag means a slower circuit response which agreed with our temperature map predictions. In contrast, the wafer with the additional AR layer did not show the concentric shape of Fig. 7(b) as there was no circuit speed lag, which confirmed that the AR layer effectively eliminated any die variation. The successful application of the AR layer shows that a 2D reflectance map is a reliable and universal methodology that can be used to pre-evaluate on-die variation caused by any pattern effect of any circuit layout. Furthermore, our experimental results confirm that the RTA annealing, which dominates dopant distribution in junction formation, is the main factor in the effect of patterning on device uniformity after thermal annealing.

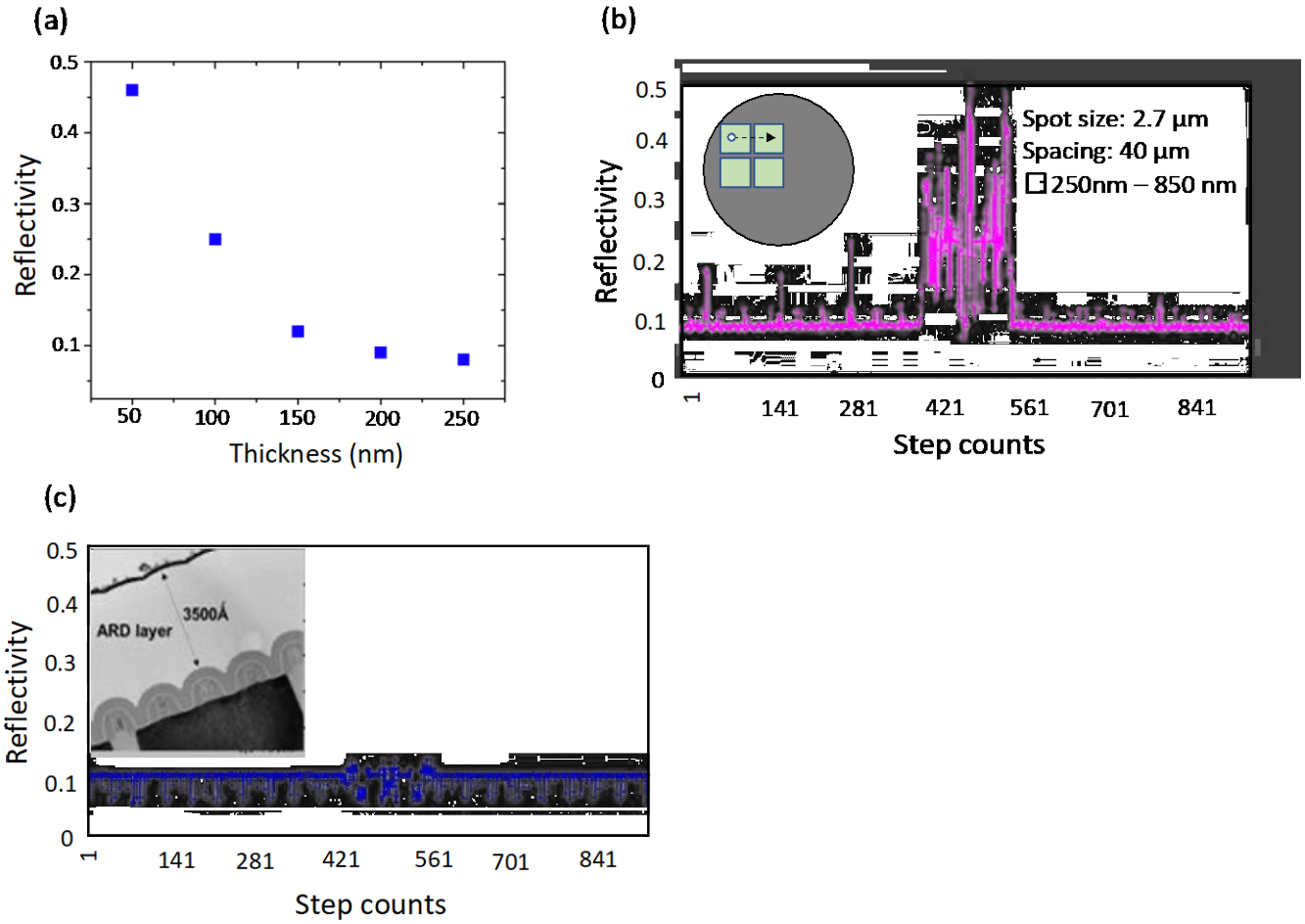

Figure. 6(a) The reflectivity of the bare silicon substrate exhibits AR layer thickness dependence, and the reflectivity saturates to 0.1 when the thickness exceeds 200 nm. Fig. 6(b). Reflectivity line scan map across the die prior to absorber deposition on a reference wafer. The reflectivity variation mainly comes from the die edge and scribe line. Fig. 6(c). Reflectivity line scan after a 400nm AR layer was deposited on the patterned wafer. The coating effectively suppressed the local reflectivity variation.

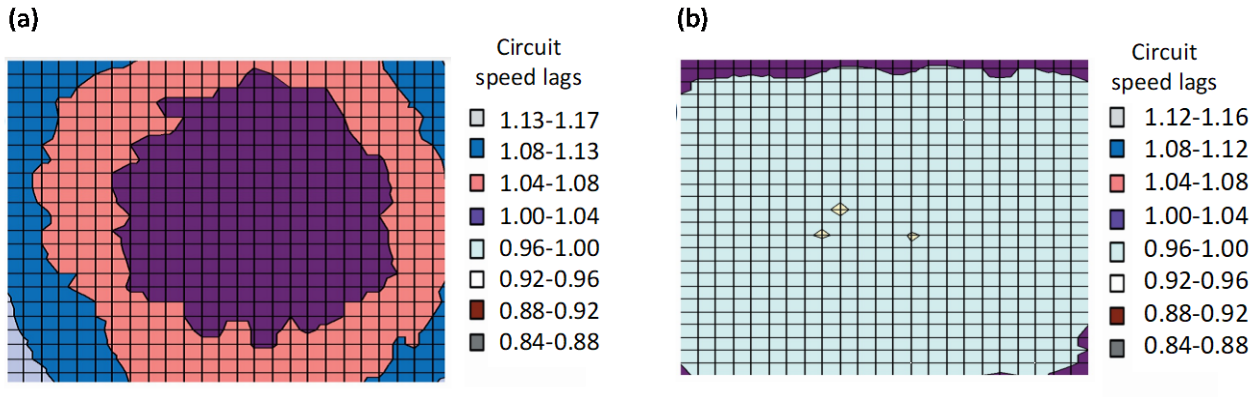

Fig. 7 (a). Reference pattern wafer without AR layer deposition prior to RTA spike annealing showed a concentric shape in the on-die variation profile. Variation was as high as 16.7%. The on-die variation map was based on calculation from 600 sub-circuits; the color/number code represents circuit speed lags; a

higher number means a slower speed. Fig. 7 (b). Device results from a patterned wafer with a 4kA AR layer deposition prior to RTA spike annealing. The concentric shape on the die variation profile was eliminated. The variation was significantly reduced from 16.7 to 7.9%.

Our study shows that the on-die pattern loading effect can be quantified by the reflectivity and the corresponding temperature variation in RTA and FLA annealing. Its impact on electrical performance would depending on the annealing temperature and the temperature sensitivity of dopant activation and distribution. For example, source-drain annealing performed by a combination of RTA and FLA showed that electrical performance is dominated by the pattern loading effect from RTA. However, this does not exclude presence of pattern loading effect from FLA and its contribution to die variation. In applications with lower FLA anneal temperatures required for highly scaled CMOS devices, one can expect greater impact on device variation due to greater temperature sensitivity[36].

In conclusion, using an evenly distributed sub-circuit layout we characterized the electrical on-die variation for a given CMOS circuit layout and investigated its correlation to pattern loading effects from annealing. Furthermore, we demonstrated the use of reflectivity characterization technology based on a xenon arc lamp at a micron-level spot size to examine the CMOS pattern before rapid annealing. This opens up the possibility of a universal methodology to evaluate emissivity-driven pattern effects of any given pattern structure. This approach allows pattern effects to be minimized during the design phase. In addition, to eliminate design constraints, we show that an absorption layer film can be used to significantly improve the pattern effect by as much as 50% and reduce the on-die electrical variation from 16.7% to 7.9%. Going forward, continued CMOS scaling will continue to demand annealing solutions with lower thermal budget. This involves developing shorter dwell times and higher energy density anneals such as DSA and, more recently, nanosecond annealing (NSA). However, these newly developed annealing methods are expected to exacerbate pattern loading effects[7]. Our study of reflectivity characterization techniques and absorber layer process solutions would produce useful insights to alleviate such challenges.

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