Fabrication, characterization and modeling of TiN/Ti/HfO_2/W memristors: programming based on an external capacitor discharge

F. Jiménez-Molinos
Departamento de Electrónica y Tecnología de Computadores
Universidad de Granada
Granada, Spain
https://orcid.org/0000-0002-8866-7568

S. Dueñas
Departamento de Electrónica
Universidad de Valladolid
Valladolid, Spain
https://orcid.org/0000-0002-2328-1752

F. Campabadal
Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC)
Bellaterra, Spain
https://orcid.org/0000-0001-7758-4567

H. García
Departamento de Electrónica
Universidad de Valladolid
Valladolid, Spain
http://orcid.org/0000-0003-1329-8806

H. Castán
Departamento de Electrónica
Universidad de Valladolid
Valladolid, Spain
https://orcid.org/0000-0002-3874-721X

J.B. Roldán
Departamento de Electrónica y Tecnología de Computadores
Universidad de Granada
Granada, Spain
https://orcid.org/0000-0003-1662-6457

M.B. González
Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC)
Bellaterra, Spain
https://orcid.org/0000-0001-6792-4556

E. Miranda
Departament d'Enginyeria Electrònica. Universitat Autònoma de Barcelona
Bellaterra, Spain
https://orcid.org/0000-0003-0470-5318

2021 13th Spanish Conference on Electron Devices (CDE) | 978-1-6654-4452-1/21/$31.00 ©2021 IEEE | DOI: 10.1109/CDE52135.2021.9455756

***Abstract*—Hafnium oxide based memristors were fabricated and multilevel programming driven by a capacitor discharge current through the device was performed. Furthermore, the dynamic memdiode model was used for modeling and analyzing the experimental data.**

Keywords—memristor, resistive-switching device, set/reset processes, capacitor.

I. Introduction

Memristors based on the resistive switching phenomenon, such as bipolar HfO_2 valence change memories (VCMs), are currently drawing attention as key devices for the implementation of neuromorphic circuits [1], such as hardware artificial neural networks [2]. For that task, each synaptic weight or matrix coefficient in a vector-matrix multiplication operation is represented by a memristor device inside a crossbar configuration [3]. Therefore, the device conductance needs to be tuned to reproduce the corresponding coefficient. Due to device variability, analog or continuous setting of the conductance is not a feasible option and, instead, multilevel operation is generally employed [4, 5].

In order to obtain these discrete set of conductance values, several programming schemes based on voltage ramps [6] or pulsed voltage operation were proposed [6-9]; even the compliance current control has been employed for this purpose [10]. Furthermore, current pulses have also been proposed for a better control of the synaptic potentiation (set) [11]. In the latter case, hardware limitations hinder the use of short current pulses and transitions are obtained with just one applied pulse, which prevents cumulative effects linked to the application of pulse series. To overcome this issue, in this work we introduce a new approach based on the control of the set and reset processes by the injection of a limited amount of charge through the use of a capacitor discharge. To do so, we use memristors based on a TiN/Ti/HfO_2/W stack, see section II. The experimental data obtained with this new technique have been simulated and analyzed using the dynamic memdiode model [13] (section III). Finally the main conclusions are drawn in section IV.

II. Device Fabrication and Measurement

Resistive switching devices based on TiN/Ti/HfO_2/W structures were fabricated and employed for the experiment. The 10 nm-thick HfO_2 layer was grown by atomic layer deposition at 225°C using TDMAH and H_2O as precursors, and the top and bottom metal electrodes were deposited by magnetron sputtering. The bottom electrode consists of a 50 nm-W layer deposited on a 20 nm-Ti adhesion layer on a highly doped n-type silicon wafer. The top electrode is a 200 nm-TiN on a 10 nm-Ti layer acting as oxygen getter material. Electrical contact to the bottom electrode is made through the Al-metallized back of the silicon wafer. The resulting structures are square cells of 5×5 μm^2. A schematic cross-section of the device structure is given in Figure 1.

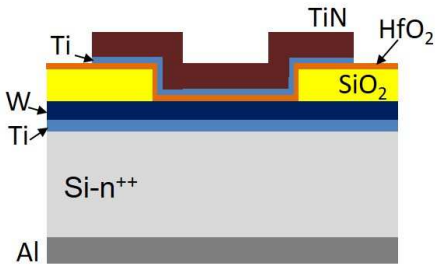

Fig. 1. Device cross-section schematics.

The TiN/Ti/HfO_2/W stack has been previously studied in depth at the simulation and experimental level. It was found that they show bipolar filamentary conduction characterized by the creation (set process) and rupture (reset process) of metallic-like conductive filaments formed by percolation paths made of oxygen vacancies that short the electrodes changing the device conductance [12].

An HP 4155B Semiconductor Parameter Analyzer was used to perform the current-voltage (*I-V*) measurements. Figure 2 shows the electrical characterization setup used to perform the measurements based on a capacitor discharge. Two relays (ϕ_1 and ϕ_2) control the capacitor charge and discharge. First, ϕ_1 is *off* and ϕ_2 is *on*, so the capacitor is charged with a V_C voltage using a Keithley 617 electrometer. When the capacitor has been charged, ϕ_2 is turned *off* and immediately ϕ_1 is turned *on:* the capacitor is now discharged through one of the resistive switching devices described above. After the capacitor is discharged, ϕ_1 is turned *off* and the device conductivity is obtained with the HP 4155B, which measures the current which flows through the device when +0.1 V is applied to the top electrode.

III. Device Modelling and Results

In order to study and characterize the resistive switching device programming experiments by transient SPICE simulation, the dynamic memdiode model has been implemented [13]. In this general memristor model, the current is given by Equation 1.

$$I = I(V_m, h) \tag{1}$$

where V_m is the applied voltage on the device and h is the state variable, whose value is assumed to be in between 0 and 1. The maximum device conductance is obtained when $h = 1$ (for a VCM device this situation could be physically interpreted as a minimum gap distance between the conductive filament tip and one of the electrodes, after a set process). On the contrary, the minimum device conductance is obtained if h equals 0 (maximum gap distance between the conductive filament tip and the electrode, after a reset process). More details about the model and the equation for the time-dependent rate of change of the state variable, *dh/dt*, can be found in Reference [14].

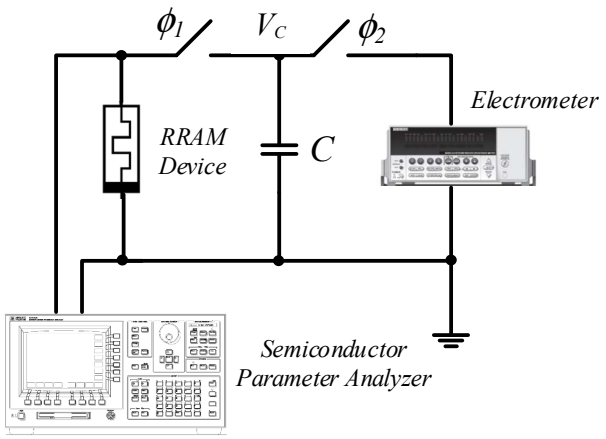

Fig. 2. Measurement setup.

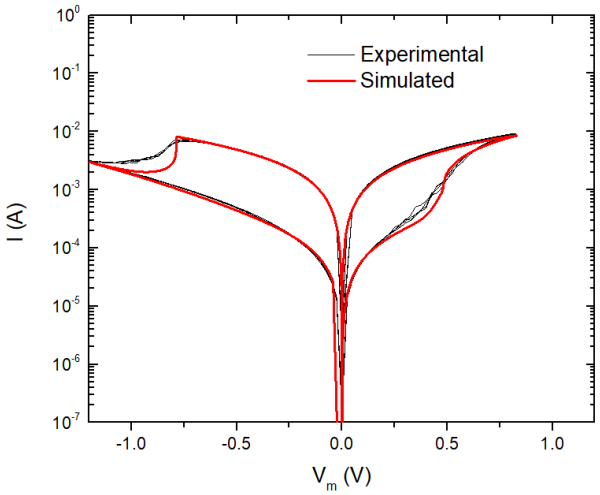

Fig. 3. Experimental (black) and modeled (red) I-V curves under ramped voltage for the devices under study.

The experimental *I-V* characteristics were measured under ramped voltage signals and the results have been employed to obtain the model parameters (following the procedure in [13]). Figure 3 shows experimental *I-V* curves and the reasonably good fit achieved using the memristor model. The inherent cycle-to-cycle variability of these devices could also be modeled, although we have not considered this issue here [6, 10, 12]. The set of model parameters obtained from the fitting of the experimental I-V curves, has been used in all the simulations performed in the present work.

Figure 4 shows the device final conductance (the read voltage is 0.1 V) after set programming using different capacitors previously charged with 1nC, as a function of the initial capacitor voltage (V_{C0}). Before the experiment, all the devices were driven to the high resistance state. Note that different conductance levels are obtained. As can be seen, the higher the initial voltage (the lower the capacitance), the higher the final device conductance. The simulation results are also given in Figure 4, showing a good agreement with the experimental values.

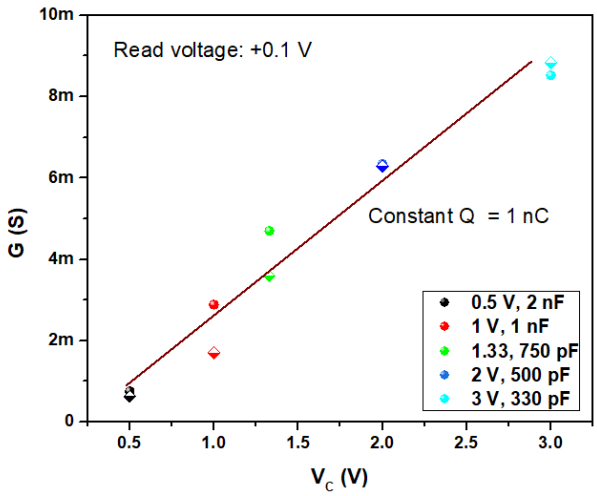

Fig. 4. Resultant conductance at 0.1 V after the device programming based on the capacitor discharge (set process) versus initial capacitor voltage (V_{C0}). Different capacitors previously charged with 1nC were employed. Solid circles: experimental data; diamonds: simulated results. The solid line represents the linear fitting of the experimental data.

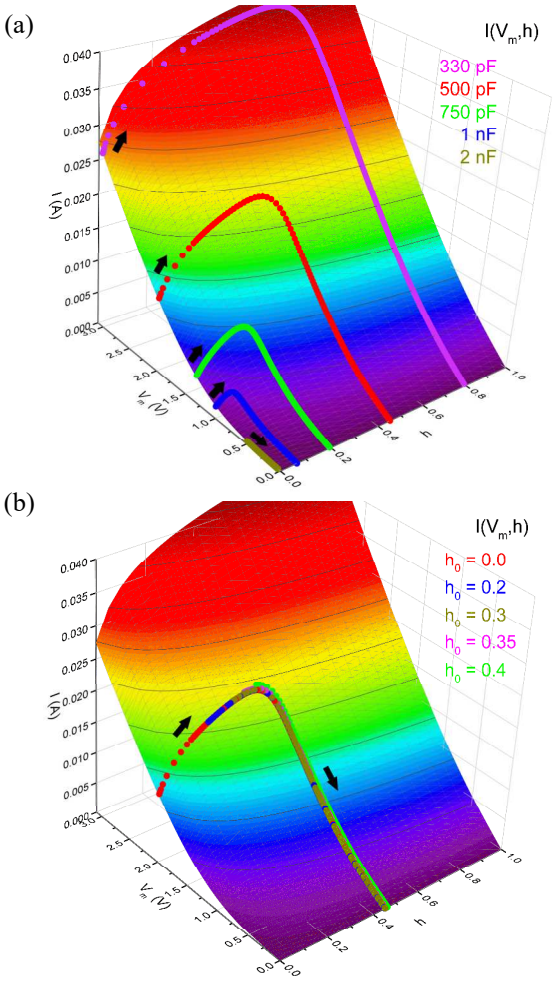

Fig. 5. a) Modeled device current characteristics $I(V_m, h)$ shown in 3D surfaces. Simulated trajectories during the same programming events as those in Fig. 4 are shown. b) Simulated trajectories departing from different memristor initial states (h_0) are shown (they correspond to the case of C = 500 pF). Colors on the surface illustrate equal current points (same horizontal plane).

As previously mentioned, according to the memdiode model, the device current is a function of the applied voltage, V_m, and the state variable, h. Therefore, in order to analyze the results and visualize the device evolution during the programming event driven by the capacitor discharge, the $I(V_m, h)$ surface is plotted in Figure 5 and the trajectories drawn on such surface during the transient simulations corresponding to Figure 4 are also shown in Figure 5a.

Note that the voltage remains almost constant while the state variable h evolves. However, as the set process progresses and the device demands more current, the capacitor acts also as a current limiting device and the memristor resistive switching evolution is stopped. In fact, Figure 5b shows that the final device state, h, does not depend on the initial one (if the latter is lower than the final value reached departing from h=0), but the current and device evolution are limited at the same point. These simulations have been obtained for the case of C = 500 pF.

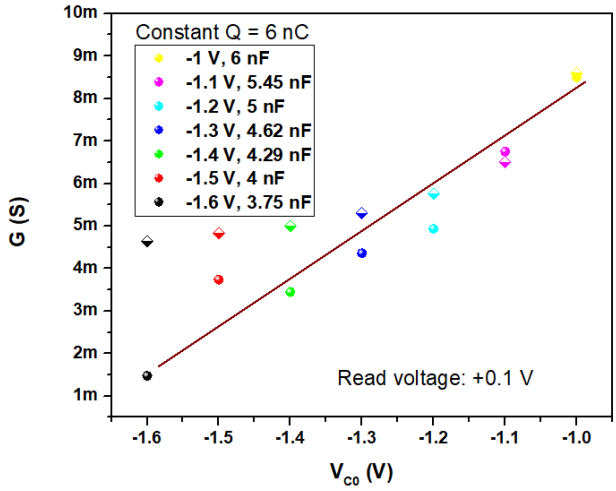

Fig. 6. Conductance at 0.1 V after a reset process versus initial capacitor voltage (V_{C0}) for different capacitors previously charged with 6nC. Solid circles: experimental data; diamonds: simulated results. The solid line represents the linear fitting of the experimental data.

Reset processes have also been experimentally performed and modeled. Different capacitors were charged with 6nC and connected to the memristor afterwards (Figure 2). After programming, the conductance was measured at 0.1V. The experimental and simulated results are plotted in Fig. 6. As can be seen, the higher the initial capacitor voltage, the lower the final conductance value (the reset process runs further). Although good agreement exists between experimental and simulated data, some difference is obtained for the highest capacitor voltage. In fact, the simulated conductance tends to saturate at the highest voltages. This effect is clear in Figure 7, where the simulated trajectories on the $I(V_m, h)$ surface are shown.

As a final remark, note that the model [13] successfully reproduces the device behaviour for different operation regimes: ramped voltage excitations (Fig. 3) or transient response during the capacitor discharge process (Figs. 4 and 6).

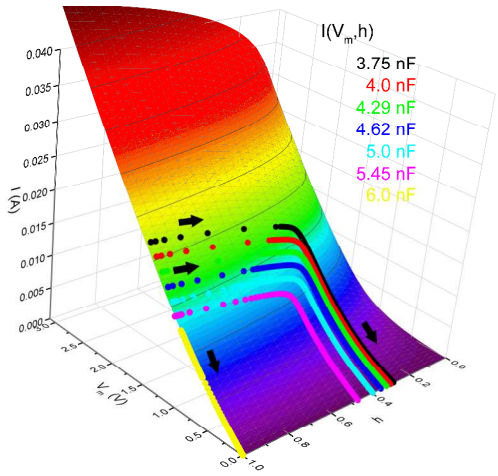

Fig. 7. Simulated trajectories on the modeled $I(V_m,h)$ surface during the same reset processes as those in Fig. 6.

IV. Conclussions

$TiN/Ti/HfO_2/W$ memristors devices were fabricated and employed in order to explore multilevel set and reset programming driven by a previously charged capacitor. The devices were modeled by means of the memdiode model, so that the device resistive switching evolution during the programming events could be sketched by transient simulation with SPICE. The same set of model parameters was used for the fitting of the *I-V* curve under ramped voltage, for the simulation of the transient set/reset processes by means of the capacitor discharge and for the calculation of the final device conductance, showing good agreement with the experimental results.

Acknowledgment

The authors thank the support of the Spanish Ministry of Science, Innovation and Universities and the FEDER program through projects TEC2017-84321-C4-1-R, TEC2017-84321-C4-2-R, TEC2017-84321-C4-3-R, TEC2017-84321-C4-4-R.

References

[1] S. Yu, "Neuro-inspired computing using resistive switching devices", Springer, Switzerland, 2017.

[2] P. Yao, H. Wu, B. Gao, J. Tang, Q. Zhang, W. Zhang, J.J. Yang and H. Qian,, "Fully hardware-implemented memristor convolutional neural network", Nature, vol. 577, p. 641, 2020.

[3] G. Milano, G. Pedretti, M. Fretto, L. Boarino, F. Benfenati, D. Ielmini, I. Valov and C. Ricciardi, "Brain-Inspired Structural Plasticity through Rewewighting and Rewiring in Multi-Terminal Self-Organizing Memristive Nanowire Networks", Adv. Intell. Syst. vol. 2, 2000096, 2020.

[4] E. Pérez-Bosch, R. Romero-Zaliz, E. Pérez, M. Kalishettyhalli, J. Reuben, M. A. Schubert, F. Jiménez-Molinos, J. B. Roldán, C. Wenger, "Toward reliable compact modeling of multilevel 1T-1R RRAM devices for neuromorphic systems", Electronics, 10, 645, 2021

[5] R. Romero-Zaliz, E. Perez, F. Jiménez-Molinos, C. Wenger, J.B. Roldán, "Study of quantized hardware deep neural networks based on resistive switching devices, conventional versus convolutional approaches", Electronics, 10, 346, 2021.

[6] S. Poblador, M.B. González and F. Campabadal, "Investigation of the multilevel capability of $TiN/Ti/HfO_2/W$ resistive switching devices by sweep and pulse programming", Micr.Eng. vol. 187-188, p. 148, 2018.

[7] H. García, O.G. Ossorio, S. Dueñas and H. Castán, "Controlling the intermediate conductance states in RRAM devices for synaptic applications", Micr. Eng. vol. 215, p. 110984, 2019.

[8] J. Park, M. Kwak,, K. Moon, J. Woo, D. Lee and H. Hwang, "TiO_x-Based RRAM Synapse With 64-Levels of Conductance and Symmetric Conductance Change by Adopting a Hybrid Pulse Scheme for Neuromorphic Computing", IEEE EDL, vol. 37, p. 1559, 2016.

[9] E. Pérez, C. Zambelli, M.K. Mahadevaiah, P. Olivo and C. Wenger, "Toward Reliable Multi-Level Operation in RRAM Arrays: Improving Post-Algorithm Stability and Assessing Endurance/Data Retention", IEEE JEDS, vol. 7, p. 740, 2019.

[10] G. González-Cordero, M. Pedro, J. Martin-Martinez, M.B. González, F. Jiménez-Molinos, F. Campabadal, N. Nafría, J.B. Roldán, "Analysis of resistive switching processes in TiN/Ti/HfO2/W devices to mimic electronic synapses in neuromorphic circuits", S. S. Elec., 157, 25-33, 2019.

[11] H. García, S. Dueñas, O.G. Ossorio and H. Castán, "Current Pulses to Control the Conductance in RRAM Devices", IEEE JEDS vol. 8, p. 291, 2020.

[12] S. Aldana, P. García-Fernández, R. Romero-Zaliz, M.B. González, F. Jiménez-Molinos, F. Gómez-Campos, F. Campabadal, J.B. Roldán, "Resistive Switching in HfO_2 based valence change memories, a comprehensive 3D kinetic Monte Carlo approach", Journal of Physics D: Applied Physics, vol. 53, 225106, 2020.

[13] E. Miranda and J. Suñé, "Fundamentals and SPICE Implementation of the Dynamic Memdiode Model for Bipolar Resistive Switching Devices", TechRxiv preprint, 2020.

[14] E. Miranda and J. Suñé, "Memristive State Equation for Bipolar Resistive Switching Devices Based on a Dynamic Balance Model and Its Equivalent Circuit Representation", IEEE T. Nanotech., vol. 19, p. 837, 2020.