Technology Development for Exploring Novel Concepts in Semiconductor Qubits

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***Abstract*—The use of semiconductor technologies for the development of qubits is having a strong development. This paper reports the development of technological solutions to enable the experimentation on semiconductor qubits. Two technological approaches are followed: spin qubits in quantum dots and Majorana qubits for topological quantum computing. This is complemented by research on advanced characterization of the fabricated qubit nanostructures.**

Keywords*— Nanoelectronics, quantum technologies, qubits, nanowires, low-dimensional structures, advanced characterization

I. Introduction

Quantum computing (QC) offers the potential to carry out exponentially more efficient algorithms than classical computing for a variety of problem classes. The devices for QC require very precise fine-tuned characteristics to avoid decoherence. Among them, semiconductor devices are experiencing a huge interest [1], as they show outstanding properties as high-quality qubits, and leverage the capabilities of the semiconductor technology. We are developing technological solutions to enable the experimentation of novel concepts for semiconductor qubits, focusing on technologies for spins in quantum dots (QD) [2] and for Majorana zero modes [3,4], supported by a platform for advanced physical characterization that is developed in parallel. This work presents the recent results of this development.

II. Process Development for Spin Qubits

We follow two manufacturing directions for semi-conductor spin qubits. The first one is based on Si nanowires (NW), where the confinement is provided in two dimensions by the NW itself, while gate electrodes around the NW create a confining potential along it. Fig. 1 shows an image of a NW pattern on a silicon on insulator (SOI) substrate.

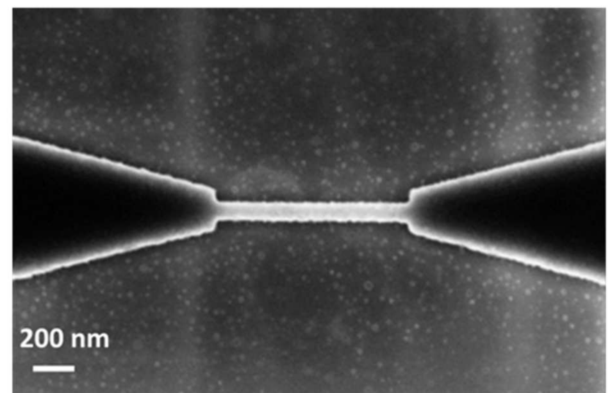

Fig. 1. SEM image of an electron beam lithography (EBL) resist pattern for the fabrication of a Si NW on a SOI substrate.

A novel fabrication route has been developed consisting of mix and match electron beam and optical lithography where the resist is exposed sequentially before a common development step. This allows the fabrication of devices at the wafer level. The emphasis in this development has been the control of the lateral doping profile in the NW, to define a lightly doped region on the central area where the QD is built while allowing lateral source/drain reservoirs to provide charge carriers to it.

The second approach is based on defining multiple gates on planar MOS structures to generate electrostatic QDs, as shown in Fig. 2. The fabrication involves a relatively complex process, with definition of field oxide, active areas, doped source/drain, gate oxide and three metal levels (for lower electrodes, transverse top electrode and contact metal). A cross section of the device is shown in Fig. 2(a). Devices in intermediate states of fabrication have been characterized by various methods. The source and drain doped areas have been studied by Kelvin probe force microscopy (KPFM), which allows mapping the work function of the measured sample.

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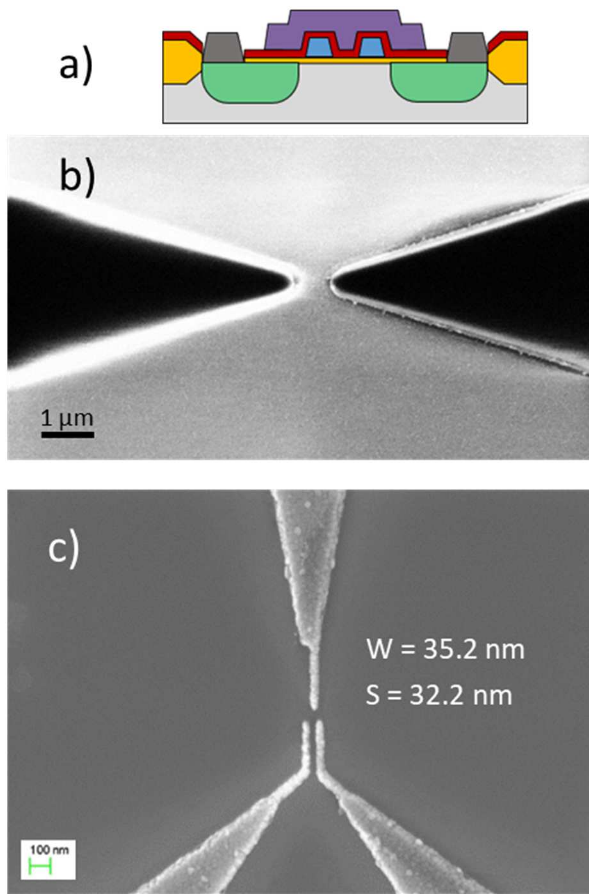

Fig. 2. a) Schematic cross section of a multiple-gate device to define a single electrostatic QD. The blue, dark grey and violet areas are conductors; red and yellow are insulators; in green the N^+-doped source and drain (S/D). b) SEM image of an optical (i-line) lithography pattern for the S/D areas. c) SEM image of Al test gates fabricated by EBL. W is the measured gate width and S the measured gate separation.

This is shown in Fig. 3. The image has been processed with the Gwyddion software [5]. To analyse the behaviour of the areas where the QD have to be defined, transistor test structures have been fabricated with an aluminium gate. An AFM image is shown as an inset in Fig. 4(a).

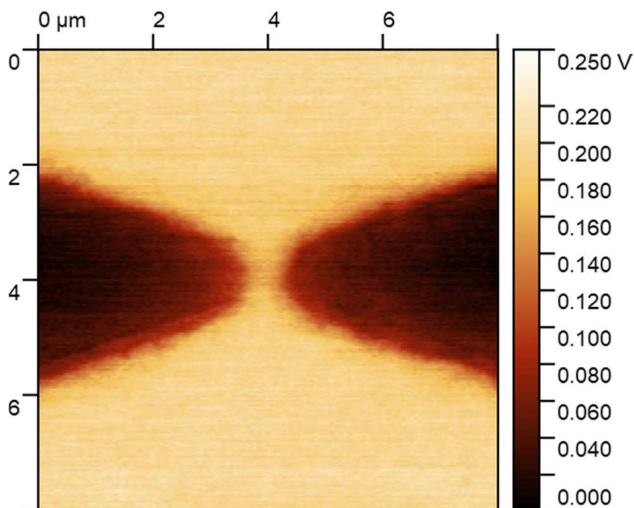

Fig. 3. Kelvin Probe Force Microscopy (AM lift mode) image of the S/D areas. We measure a contact potential difference of 170 mV between the ion-implanted and intrinsic regions of the device.

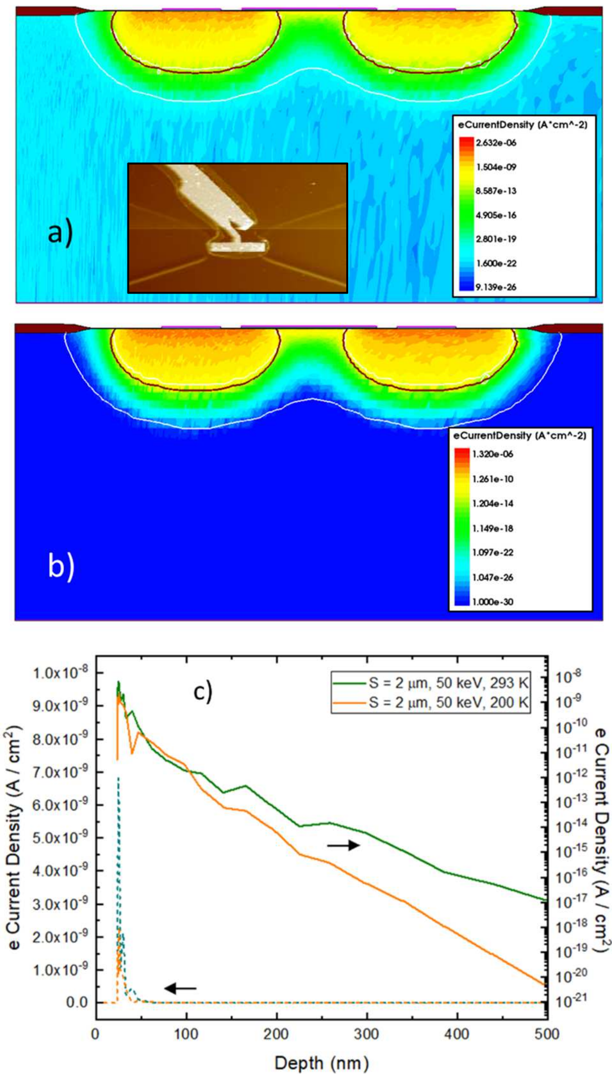

Fig. 4. FET test structure with 2 µm S/D nominal separation, with a phosphorus S/D implantation (dose: $4.2 \cdot 10^{15}$ cm^{-2}; energy: 50keV) and an annealing at 850 C. Inset in a): AFM image of the device with an Al metal gate. a) Simulation of the electron current density at 293 K (cross section). b) Simulation of the electron current density at 200 K (cross section). c) Electron current density as a function of the depth at the channel, for the simulations in a) and b). In all cases V_{DS}= 10 mV, V_{GS}= 0V.

For a 2 µm nominal S/D separation in these FET test structures, a parasitic current of around 0.1 µA appears that cannot be controlled by the gate voltages, due to punch-through by the overlapping source and drain depletion widths. To have a quantitative understanding of this effect, process and device simulations have been performed with Sentaurus TCAD software from Synopsys, Inc. The results for the parasitic currents are shown in Figs.4(a) and 4(c).

The QD qubit devices should, however, be operated at low temperatures. The device simulation shows that there is a clear reduction of the parasitic current if the FET is operated at 200 K, as shown in Figs. 4(b) and 4(c), and the current should be further reduced at even lower temperatures. To avoid the effects of punch-through, the next generation of devices will be fabricated with a higher S/D separation.

III. Process Development for Hybrid Semiconductor/Superconductor Qubits

Narrow bandgap III-V semiconductor NW with strong spin-orbit coupling, e.g. InAs, InSb, combined with a superconducting material offer great prospects for the realization of topologically protected, fault-tolerant qubits. With the aim of having a scalable process to fabricate networks of interconnected III-V/Al NW hybrids that will allow for the manipulation and transfer of quantum information, we have developed a method based on atomic hydrogen-assisted molecular beam epitaxy (H-MBE) using nanoscale selective area growth on SiO_2/Si(001) substrates, previously patterned by electron beam lithography (EBL). The method includes ex-situ UV-O_3 and in-situ atomic H irradiation steps, followed by As pre-deposition and one-step growth of the III-V compound at high V/III flux ratios. Under these conditions, selective growth of InAs NW via 2D nucleation and coalescence on the unmasked Si substrate is demonstrated, as depicted in the HRSEM images shown in Fig. 5. In addition, VLS growth of self-standing InAs nanowires on Si(111) substrates is also being investigated as a platform to perform quantum transport measurements in this material. Self-catalyzed nanowires that are single phase (ZB) and ≈8 μm long have been grown in the 500-550ºC temperature range with V/III ratios below 18. Another approach being explored is Au-catalyzed growth at lower temperatures, i.e. 400ºC, which has rendered faceted nanowires bounded by (110) nanofacets with high diameter uniformity and lengths up to 3μm, as shown in Fig. 6(a). Furthermore, selective area growth has been applied to demonstrate 1D and 2D arrays of defect-free and coherent InAs/GaAs quantum dots monolithically integrated on nanopatterned Si substrates having various geometries, i.e. grids, pyramids [6]. Fig. 6(b) depicts an individual quantum dot selectively nucleated on an inverted GaAs-coated Si pyramid, as part of a 2D array of these InAs nanostructures.

IV. Advanced Characterization

Optical characterization using micro-Raman spectroscopy yields valuable information on the material properties all along the technological processes followed to the qubit preparation, e.g., stress induced by the gates, crystal disorder induced by dry etching, and local doping assessment. This

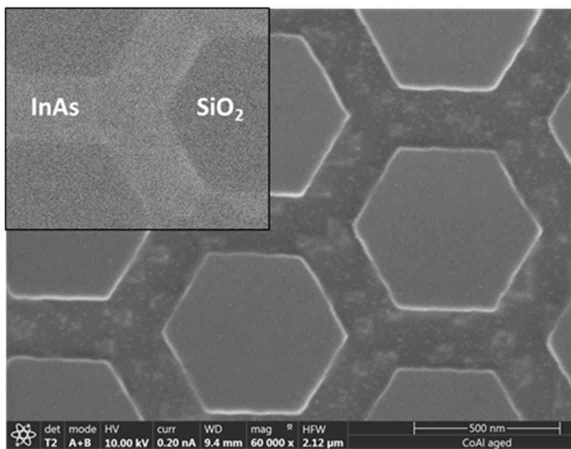

Fig. 5. HRSEM topography image showing selective 2D nucleation of InAs on the SiO_2-masked Si(001) substrate. Inset: Backscattered electron image (z-contrast) illustrating InAs nanowire growth on the unmasked Si areas.

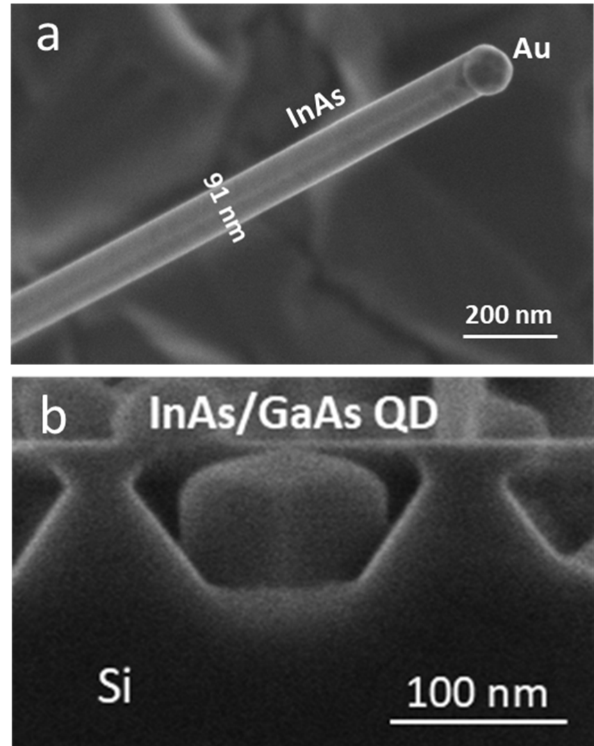

Fig. 6. High-resolution scanning electron micrograph showing (a) self-standing InAs nanowire grown by MBE using the VLS technique on a Si(111) substrate and (b) cross-section image of an InAs/GaAs quantum dot nucleated by selective area growth on a nanopatterned Si/SiO_2 substrate.

allows us to discern the critical steps in materials and device processing towards functional qubits. Figure 7(a) displays as an example the optical image of a B-doped Si structure made by dry etching on a SOI wafer. It includes a Si NW 1200 nm long and 60 nm diameter, and two contact pads, a triangular shaped one and a rounded one. Micro-Raman imaging in the region of interest was taken with a laser excitation of 532 nm wavelength and 4.5 mW power, using a HORIBA Soleil spectrometer with a 200 μm pin hole, a 2400 l/mm grating 500 nm blazed, and a CCD detector. The spectra display the typical Si Raman mode at 520 cm^{-1}, both on the contacts, on the NW, and at the etched SOI substrate. 2D hyperspectral images were acquired with 100 nm step size focusing the laser on each XY map point. The spectra were fitted by asymmetric Lorentzian functions, revealing subtle but significant changes in the Raman parameters, namely, asymmetry parameter, linewidth, Raman shift, and Raman intensity. Special attention is paid to the asymmetry of the phonon line shape. The Raman parameter images extracted from the hyperspectral image are also shown in Fig. 7. It is worth mentioning that changes in all parameters allow us to distinguish the uppermost 30 nm thick B-doped Si layer from the bottom Si/SiO_2 substrate. The Raman spectra of the contact pads show a lower intensity, slightly larger values of the asymmetry parameter, and a considerable broadening, as compared to the etched substrate. Furthermore, the etching edges of the B-doped Si layer, in both the contact pads and the NW exhibit a significant increase of both asymmetry and linewidth, accompanied by a subtle increase in phonon peak frequency, revealing a local compressive strain [7]. A careful analysis of the Raman spectra at these boundary points reveals a broadening of the phonon peak towards its low frequency side, congruent with the presence of disorder induced by the etching process [8].

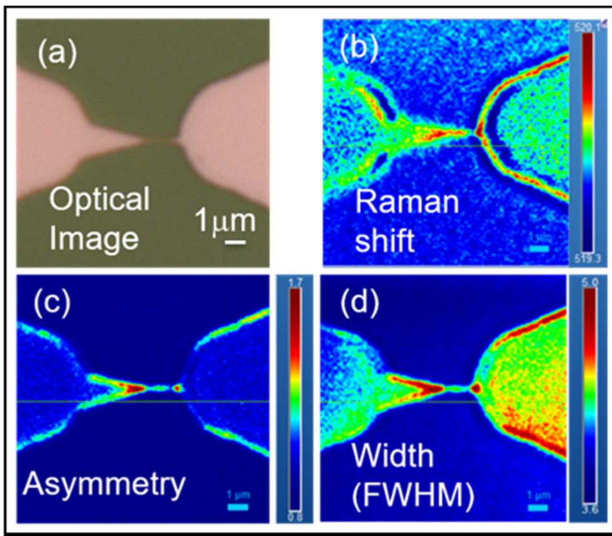

Fig. 7. (a) Optical microscopy image of the contact pads and Si NW region of a Silicon-on-insulator (SOI) bottom-up structure for development of Si qubits. Color maps of (b) Raman shift, (c) asymmetry parameter, and (d) full width at half maximum (FWHM) of asymmetric Lorentzian fit to the micro-Raman hyperspectral image taken with a step of 100 nm. The small but significant changes in the Raman shift indicate strain and disorder. The asymmetric parameter and the FWHM distributions are related to crystalline disorder. The main changes in the Raman features are observed in the dry etched edges, which reveals that the dry etching is not a neutral process, as it can produce structural changes in Silicon.

Figure 8 displays two Raman spectra corresponding to the contact edges and the etched Si/SiO_2 substrate, showing this asymmetric broadening. We attribute the changes in the Raman parameters at these contact edges to the dry etching process. Micro-Raman imaging is demonstrated here to be a powerful characterization technique of the effects of dry etching processing on the fabrication of semiconductor NW based qubits.

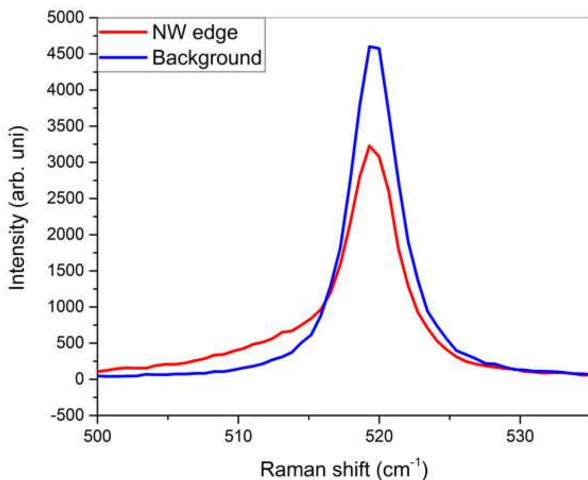

Fig. 8. Raman spectra obtained from the etched Si/SiO_2 background (blue line) and from the contact edge joining the NW, displaying the largest asymmetry in the phonon line shape (red line). The shoulder shown at the lower frequency side is attributed to accidental crystalline disorder stemming from the dry etching process.

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